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Cloud Nyamhere, A Scheinemann, A Schenk, A Scheit, François Olivie, et al.. A comprehensive study of the impact of dislocation loops on leakage currents in Si shallow junction devices. Journal of Applied Physics, 2015, 118, pp.184501. 10.1063/1.4935293 . hal-01921377

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Citation: Journal of Applied Physics **118**, 184501 (2015); doi: 10.1063/1.4935293
View online: http://dx.doi.org/10.1063/1.4935293
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/118/18?ver=pdfcov
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# A comprehensive study of the impact of dislocation loops on leakage currents in Si shallow junction devices

C. Nyamhere,[1,2,3,a)] A. Scheinemann,[4] A. Schenk,[4] A. Scheit,[5] F. Olivie,[1,2] and F. Cristiano[1,2]
[1]*CNRS, LAAS, 7 avenue du colonel Roche, F-31400 Toulouse, France*
[2]*Univ de Toulouse, LAAS, F-31400 Toulouse, France*
[3]*Midlands State University, P. Bag 9055, Gweru, Zimbabwe*
[4]*ETH Zürich, Gloriastr. 35, 8092 Zurich, Switzerland*
[5]*IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany*

(Received 23 July 2015; accepted 20 October 2015; published online 9 November 2015)

In this work, the electrical properties of dislocation loops and their role in the generation of leakage currents in p-n or Schottky junctions were investigated both experimentally and through simulations. Deep Level Transient Spectroscopy (DLTS) reveals that the implantation of silicon with $2 \times 10^{15}$ Ge $cm^{-2}$ and annealing between 1000 °C and 1100 °C introduced two broad electron levels $E_C - 0.38$ eV and $E_C - 0.29$ eV in n-type samples and a single broad hole trap $E_V + 0.25$ eV in the p-type samples. These trap levels are related to the extended defects (dislocation loops) formed during annealing. Dislocation loops are responsible for the significant increase of leakage currents which are attributed to the same energy levels. The comparison between structural defect parameters and electrical defect concentrations indicates that atoms located on the loop perimeter are the likely sources of the measured DLTS signals. The combined use of defect models and recently developed DLTS simulation allows reducing the number of assumptions and fitting parameters needed for the simulation of leakage currents, therefore improving their predictability. It is found that simulations based on the coupled-defect-levels model reproduce well the measured leakage current values and their field dependence behaviour, indicating that leakage currents can be successfully simulated on the exclusive basis of the experimentally observed energy levels. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4935293]

## I. INTRODUCTION

Ion implantation is widely used for the formation of doped regions in several different semiconductor devices.[1–3] One of the main consequences of this doping method is the formation of extended defects (EDs) during the annealing step required to recover implant damage. Defects are at the origin of several deleterious effects that need to be minimised to improve the device performances. For instance, source/drain junction leakage in metal-oxide-semiconductor (MOS) devices is particularly sensitive to implantation-induced extended defects. These defects may not be fully removed after state-of-the-art low-thermal budget annealing processes, which today include spike rapid thermal anneal (RTA), flash lamp or laser annealing. In particular, leakage current is critical and undesirable in modern MOS devices as they drain power supply resources in integrated circuits and systems.[2,4] Also, in advanced solar cell structures, secondary defects formed during annealing may cause an increased Shockley-Read-Hall recombination of minority carriers, reducing the overall conversion efficiency of the device. For boron implantation, defects such as dislocation loops (DLs) and boron-interstitial clusters have been identified as possible causes of high recombination.[3,5,6] Finally, in CMOS-based imagers, the neighbour pixel isolation, necessary to avoid pixel-to-pixel crosstalk issues,[7] can be achieved by ion implantation,[8,9] where again defects can act as generation/recombination centres. Thus, identifying and characterizing the electrical impact of implantation-induced defects are critical elements in the optimisation of several semiconductor device fabrication processes.

Extended knowledge is available on the origin of implantation-induced defects, including their structure and impact on dopant diffusion/activation anomalies.[10] Several studies exist in which the electrical behaviour of dislocation loops has been investigated by deep level transient spectroscopy (DLTS)[11,12] or where their impact on leakage currents has been qualitatively shown in terms of their position within the space charge region (SCR).[13,14] However, a "comprehensive" study of this issue, including the correlation of the defect parameters (density, size, nature) to the DLTS signal (peak, energy levels) and to the measured leakage currents is not yet available. Moreover, it is important to be able to simulate the electrical behaviour of the defects in TCAD, due to the strategic importance of predictive simulations in the design of future devices.

In this work, the full "chain value" (from the structural and electrical properties of dislocation loops to their role in the generation of leakage currents in p-n or Schottky junctions) is investigated both experimentally and through simulations. In Section II, the experimental investigations will be described in detail. In Section III, the combination of defect models and recently developed DLTS simulations will be

a)Author to whom correspondence should be addressed. Electronic mail: cnyamhere@gmail.com. Tel.: +263 54 260464. Fax: +263 54 260753.

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TABLE I. Sample details and implantation conditions (species, dose, energy, annealing temperature, and pn junction depth).

| Substrate | Implant ions | Dose ($cm^{-2}$) | Energy (keV) | {$T_{anneal}$ (°C)}[a] | $X_j$ (nm) |
|---|---|---|---|---|---|
| n-type | … | … | … | … | 200 |
| | Ge | $2 \times 10^{15}$ | 560 | 1000 °C_15 s | |
| | Ge | $2 \times 10^{15}$ | 560 | 1100 °C_300 s | |
| p-type | Ge | $2 \times 10^{15}$ | 560 | 1000 °C_15 s | 150 |
| | Ge | $2 \times 10^{15}$ | 560 | 1100 °C_300 s | |
| p-type | Ge | $5 \times 10^{14}$ | 560 | 1050 °C_15 s | Schottky diodes |
| | Ge | $2 \times 10^{15}$ | 560 | 1000 °C_15 s | |

[a]Post-implantation anneal for defect formation.

used to perform leakage current simulations using the state of the art industrial simulation solution by SYNOPSYS and discuss different simulation approaches.

## II. EXPERIMENTAL INVESTIGATION

### A. Experimental details

Phosphorus and boron-doped (001) bulk silicon samples, doped to $4.5 \times 10^{15}$ or $1.0 \times 10^{16}\,cm^{-3}$, respectively, have been implanted with 560 keV $Ge^+$ to a dose of $5 \times 10^{14}\,cm^{-2}$ or $2 \times 10^{15}\,cm^{-2}$ at room temperature followed by post-implantation annealing. All the ion implantations were performed with a tilt of 7° and a twist of 22°. The implantation, annealing and diode fabrication were performed at IHP-Microelectronics, Germany. The ion implantation conditions, listed in Table I, were specifically chosen in order to form a layer of end-of-range (EOR) defects at a depth of ~600 nm below the surface as shown in Fig. 1. In particular, the annealing temperatures ($T \geq 1000\,°C$) resulted in the formation of faulted circular dislocation loops, lying on {111} planes, with a Burgers vector of $a/3\ \langle 111 \rangle$.[10] In this paper, they will be referred to as "dislocation loops."

To enable the probing of the EOR defects, electrical characteristics and their impact on leakage currents on the same space charge region structure, a Schottky diode or a pn junction may be used as a test device. Both structures were fabricated in this work.

Following the Ge implants and annealing for defect formation, the pn junction devices were formed by implanting either 2 keV $B^+$ $5 \times 10^{14}\,cm^{-2}$ or 5 keV $P^+$ $2 \times 10^{14}\,cm^{-2}$ in the n or p-type Si substrate, respectively. The dopant activation was achieved by a 950 °C post implant spike anneal. TiN was used as the metal contact, an oxide layer as a spacer and CoSi for the silicide. The resulting pn junctions were located at ~200 nm and ~150 nm from the surface for $p^+n$ and $n^+p$ junctions, respectively. The junction depths were deduced from SIMs measurements. The junction location in both substrates ensured that the EOR defects were located at least 200 nm below the zero bias depletion region therefore allowing the EOR to be placed in the space charge region when the diode is reverse biased.

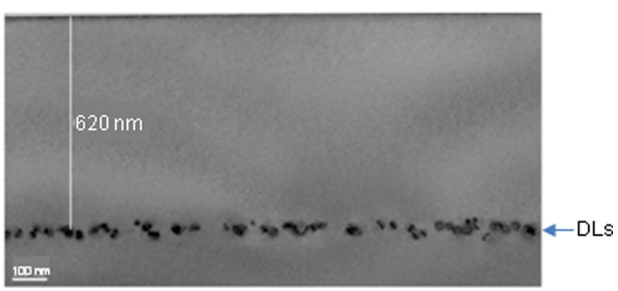


FIG. 1. TEM cross-section image showing dislocation loops introduced in Si after implantation with $2 \times 10^{15}$ Ge $cm^{-2}$ and annealed at 1000 °C for 15 s.

In the case of the p-type Schottky diodes and after the Ge implants and annealing for defect formation, a 100 nm titanium (Ti) layer was evaporated onto the front side of the sample. Standard lithography and etching was then used to define circular Schottky contacts. Silver paste was used as the backside ohmic contact.

Current-voltage (IV) measurements were used to monitor the diode qualities and leakage currents, whereas the capacitance-voltage (CV) measurements were used to extract the sample free carrier concentrations in the sample. The electronic properties of deep levels introduced after the ion implantation and post-implant annealing were characterized by DLTS. The "*signatures*" of the observed deep levels (i.e., activation energy for electron emission, $E_T$, and the apparent capture cross section, $\sigma_a$) were determined from Arrhenius plots of $ln(T^2/e)$ vs. 1000/T. Here, $e$ represents the charge carrier emission rate, and $T$ is the measurement temperature in Kelvin. TEM measurements have been used to monitor the extended defect structures.

### B. Results

#### 1. Electrical characterization of dislocation loops

*a. Electron traps.* Fig. 2 shows the DLTS spectra of electron traps in n-type Si for (a) reference (un-implanted) sample and after ion implantation of n-type Si with $2 \times 10^{15}$ Ge $cm^{-2}$ and after post-implant anneals at (b) 1100 °C for 300 s and (c) 1000 °C for 15 s. The DLTS spectra in Fig. 2(c) show a dominant and broad peak attributed to an electron trap with activation energy of 0.38 eV below the conduction band. The DLTS signal of this level clearly decreases upon increasing the thermal budget to 1100 °C as shown in Fig. 2(b) and a lower temperature peak at E(0.29) is also more pronounced after using the higher thermal budget.

The activation energy and "apparent" electron capture cross-section of the defects were extracted from the Arrhenius plots shown in Fig. 3. Ayres *et al.*[12] observed a similar dominant electron trap, with activation energy of

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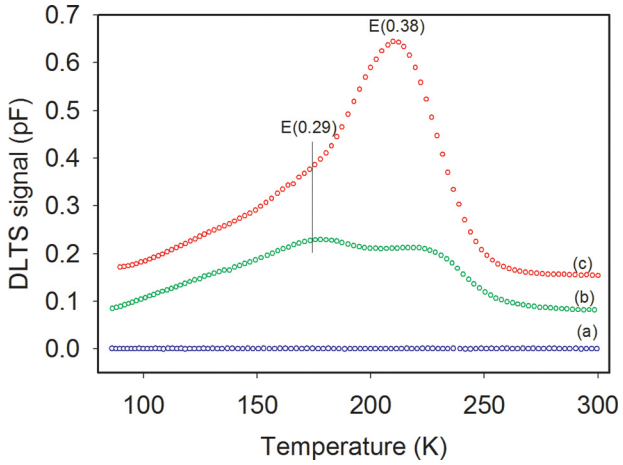


FIG. 2. DLTS spectra in n-type Si for the (a) reference sample and after implantation to a dose of $2 \times 10^{15}$ Ge cm$^2$ and annealing at (b) 1100 °C for 300 s and (c) 1000 °C for 15 s.

about 0.38 eV, after implantation of silicon with Ge amorphising implants and annealing at 900 °C and they associated this level to the dislocations loops.

To shed more light on the nature of these implantation defects, the energy band model[15] has been fitted to the experimental DLTS spectra. The computation of the DLTS spectrum for the sample annealed at 1000 °C or 1100 °C with the energy band model shown in Fig. 4 reveals that the dominant electron trap E(0.38) has a broadening factor of S = 23 meV for both samples. The energy band model mentioned here assumes that the deep levels that produce the broad peaks are not associated to a single level with an activation $E_o$ but to a narrow band of levels that form Gaussian distribution having $E_o$ as the mean value and with a broadening described by an S factor. Ayres and Brotherton[11] obtained an energy spread, S, of about 27 meV for their electron trap level with activation energy of 0.38 eV in silicon samples with dislocation loops formed after amorphising Ge implants and annealed at 900 °C. A lower temperature shoulder also observed by Ayres and Brotherton in Ref. 11 is clearly visible in Fig. 4. In addition, the measurement of the electron capture

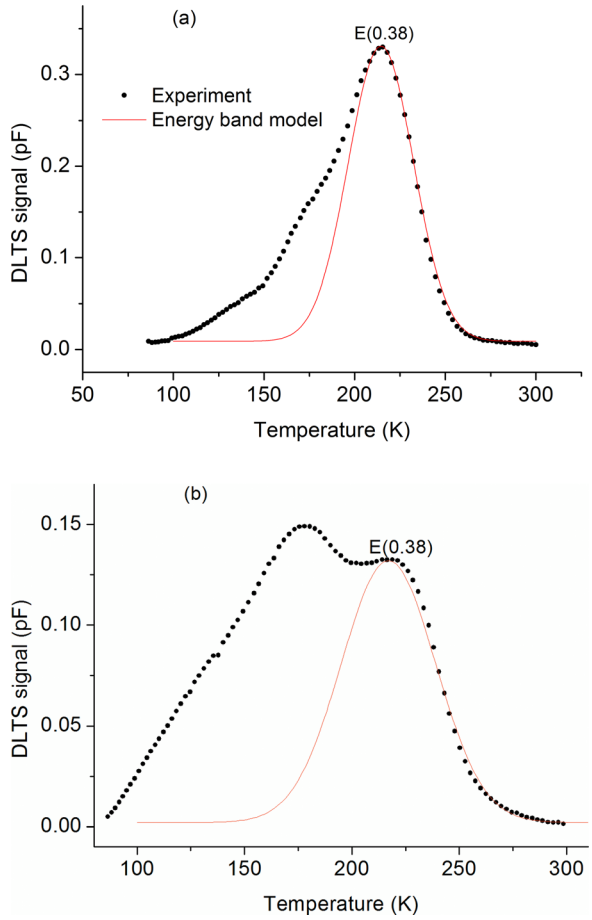


FIG. 4. DLTS spectra of electron traps in the sample implanted with $2 \times 10^{15}$ Ge cm$^{-2}$ and annealed at (a) 1000 °C for 15 s and (b) 1100 °C for 300 s. The experimental data are shown in solid circles, whereas the fit by the energy band model is indicated by solid lines.

kinetics[16] relative to the E(0.38) level, shown in Fig. 5, reveals a logarithmic characteristic for a filling pulse between $10^{-5}$ and $10^{-2}$ s, while the deviation from linearity for pulses larger than 10 ms is a measurement artefact introduced by capacitance meter overload at such high filling pulse widths. Similar charge capture behaviour was obtained

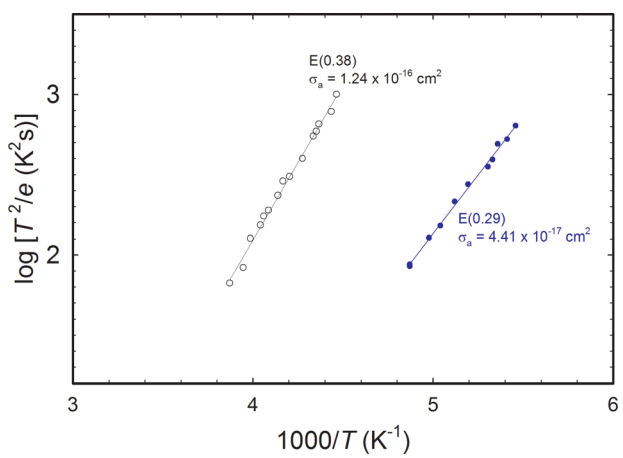


FIG. 3. Arrhenius plots for the defects introduced by implantation of $2 \times 10^{15}$ Ge cm$^{-2}$ into n-type Si from which activation energies and "apparent" electron capture cross sections were extracted.

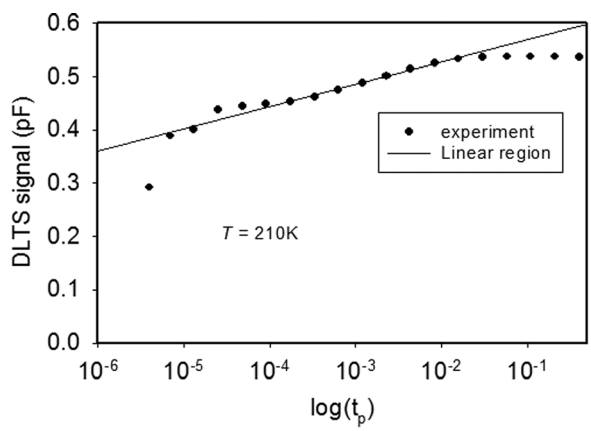


FIG. 5. Electron capture kinetics for the level E(0.38) for the sample annealed at 1000 °C for 15 s showing a logarithmic characteristic normally associated with extended defects. Similar characteristics were obtained for the sample annealed at 1100 °C.

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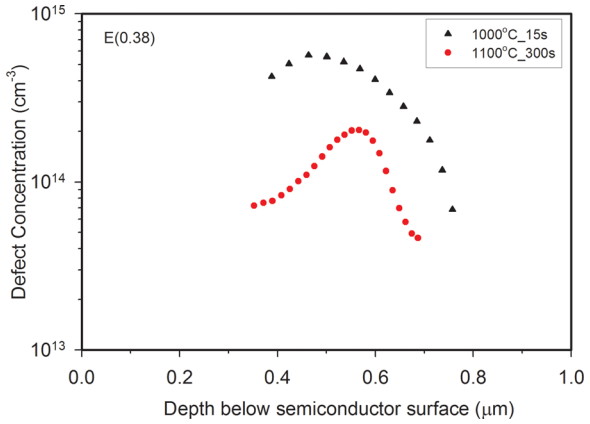


FIG. 6. Defect depth profiles for the electron trap E(0.38) in samples implanted with a dose of $2 \times 10^{15}$ Ge cm$^{-2}$ and post-implant annealed at (i) 1000 °C (triangles) and (ii) 1100 °C circles. The profiles were recorded using a fixed bias-variable pulse.[17]

for the 1100 °C sample. Therefore, the combination of energy band broadening factor, the logarithmic defect capture kinetics and the defect formation annealing temperatures (1000 °C or 1100 °C) all prove that the DLTS signal is directly related to the dislocation loops.

The correlation between the DLTS signal and the implantation-induced dislocation loops is further supported by the DLTS defect concentration profile[17] as a function of depth shown in Fig. 6. For both samples annealed at 1000 °C and 1100 °C the DLTS defect concentration profile peaks around the expected EOR defect region, i.e., ∼600 nm from the semiconductor surface. The slight peak shift from the expected EOR position could be due to the experimental error introduced by the uncertainty of the depletion width transition region.[13] Furthermore, the decrease in the peak concentration as the annealing temperature increases from 1000 °C to 1100 °C is about a factor of 2, correlating well with the decrease in DLs density as the annealing temperature is increased. This correlation will be further discussed in Section II B 1 c.

*b. Hole traps.* Fig. 7 shows the DLTS spectra of hole traps (Schottky diodes) in p-type Si for (a) reference (unimplanted) sample and after ion implantation with (b) $5 \times 10^{14}$ Ge cm$^{-2}$ and annealed at 1050 °C for 15 s and (c) $2 \times 10^{15}$ Ge cm$^{-2}$ and annealed at 1000 °C for 15 s. It must be mentioned here that it was not possible to measure the DLTS spectra in the n$^+$p diodes annealed at 1100 °C due to the high leakage currents in these diodes (see Table I for sample details). The DLTS spectra in Fig. 7 show a dominant and broad signal peak that is attributed to a hole trap with activation energy of 0.25 eV above the valence band for all samples.

Ayres and Brotherton[11] observed two hole traps, with activation energies 0.26 eV and 0.47 eV above the valence band after Ge amorphising implants and annealing at 900 °C, in which the 0.26 eV level is the most dominant peak (∼4× higher amplitude than the 0.47 eV level). The level at 0.26 eV is most likely similar to the level H(0.25) we have observed in our samples whereas the deeper level was not observed in our samples. This may simply be due to the fact that its concentration falls below our system detection limit since we have used higher annealing temperatures (>1000 °C) compared to the one (900 °C) used in Ref. 11.

Fig. 8 shows a comparison of the measured DLTS signal and the computed DLTS signal after assuming a narrow band of energy levels with a broadening factor S. It is clear from the curve that the simulation does not fit well on the lower temperature side, probably due to the presence of a shallower peak or due to additional effects that will be discussed in Section III. The defect broadening factor extracted after the model fitting (for samples b and c in Fig. 7) is S = 23 meV. This result is similar to the value obtained for the E(0.38) electron trap discussed in Section II B 1 a. The capture kinetics of the hole trap H(0.25) shows similar characteristics to the one found for the E(0.38) electron trap discussed in Section II B 1 a. The capture kinetics for H(0.25) is logarithmic for a filling pulse between $10^{-5}$ and $10^{-2}$ s (dashed line in Fig. 9), which is typically associated with extended defects.[18]

*c. Discussion.* The amorphising implantation of Si with $2 \times 10^{15}$ Ge cm$^{-2}$ and annealing at 1000 °C, 1050 °C, or

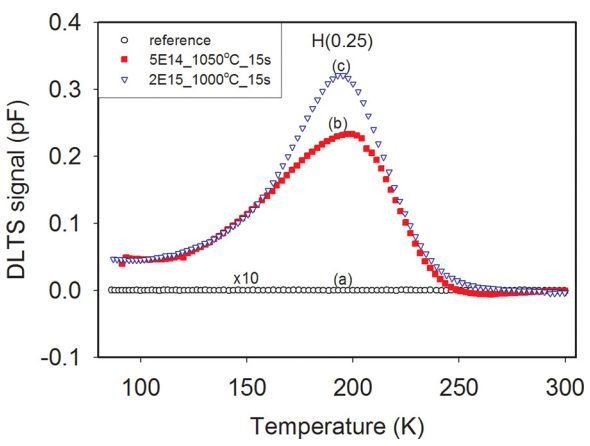


FIG. 7. DLTS spectra in p-type Si (Schottky diode) for the (a) reference sample and after ion implantation with (b) $5 \times 10^{14}$ Ge cm$^{-2}$ and annealed at 1050 °C for 15 s and (c) $2 \times 10^{15}$ Ge cm$^{-2}$ and annealed at 1000 °C for 15 s.

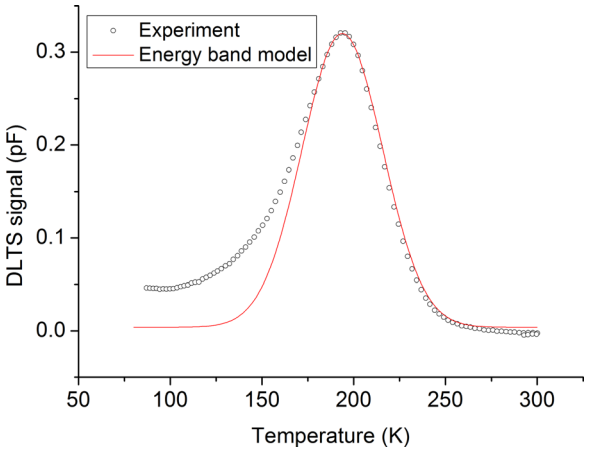


FIG. 8. DLTS spectra of hole traps in the p-type Si sample implanted with $2 \times 10^{15}$ Ge cm$^{-2}$ and annealed at 1000 °C for 15 s (i) experiment data (solid circles), and fit with (ii) band model (solid line).

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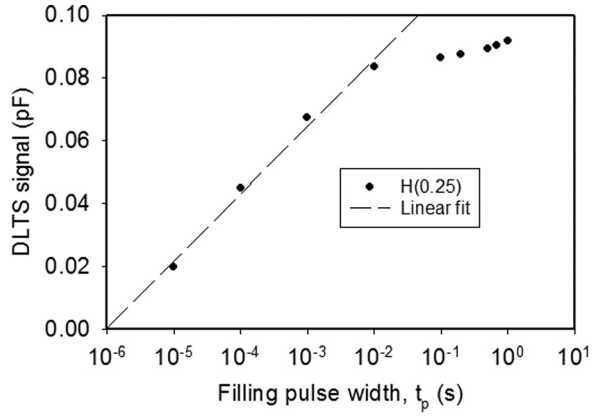


FIG. 9. Hole capture kinetics for the level H(0.25) in the sample annealed at 1000 °C for 15 s.

1100 °C resulted in the formation of dislocation loops shown in the TEM images in Fig. 10 for the lowest and highest investigated temperatures. When the annealing temperature is increased from 1000 °C to 1100 °C the defect size increases and the concentration decreases as expected. DLTS measurements in these samples have revealed broad signal peaks related to the electron traps E(0.38) and E(0.29) and a single hole trap H(0.25).

The extended nature of the trap levels E(0.38) and H(0.25) has been confirmed by peak broadness and logarithmic behaviour of the capture kinetics (within the filling pulse range $10^{-5}$ s $-10^{-2}$ s), all indicating that the DLTS signal is directly related to the dislocation loops.

In order to better identify the possible "structural" origin of the observed electrical defects, we investigate in Figs. 11 and 12 the correlation between the DLTS defect concentrations obtained in the p-type and n-type samples, respectively, and three different physical parameters describing the dislocation loops population, as extracted from TEM analysis (coloured symbols). The first is the dislocation loops areal density, i.e., the "number of defects" ($D_{Loop}$, red circles), which can be directly measured from TEM plan-view micrographs. From $D_{Loop}$ and the measured values of the loop size, and knowing the atomic structure of the defects[10] (precipitates of Si interstitial atoms in the form of {111} faulted loops in our case), it is then possible to calculate two additional parameters, namely, the areal density of all the Si interstitial atoms contained in the loops ($C_{Loop}$, green squares) and the areal density of those Si interstitial atoms being

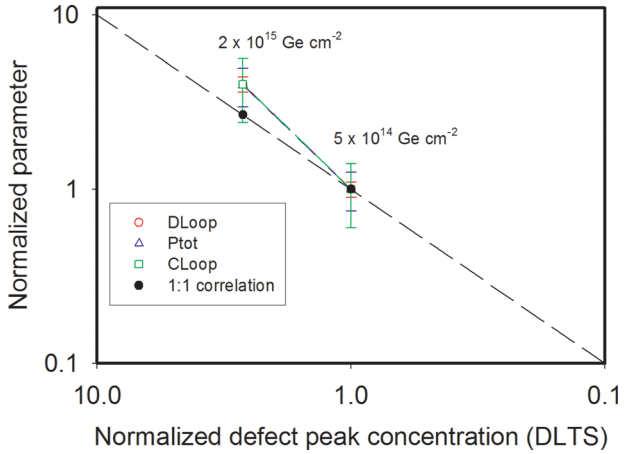


FIG. 11. Normalised defect properties ($D_{tot}$, $C_{tot}$, or $P_{tot}$) as a function of defect peak concentration extracted from DLTS for the hole trap H(0.25) in the samples implanted with $5 \times 10^{14}$ Ge $cm^{-2}$ or $2 \times 10^{15}$ Ge $cm^{-2}$ annealed at 1050 °C or 1000 °C, respectively.

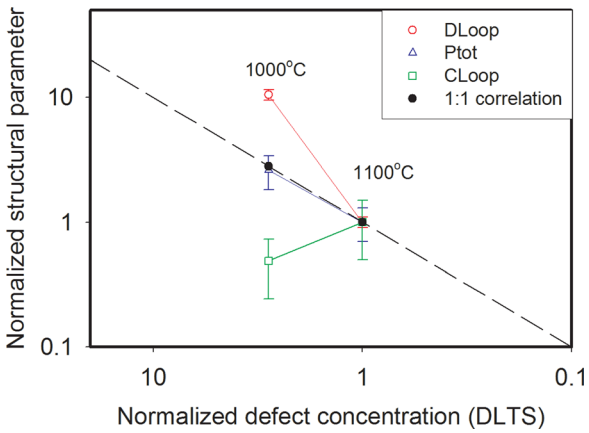


FIG. 12. Normalised defect properties ($D_{tot}$, $C_{tot}$, or $P_{tot}$) as a function of defect peak concentration extracted from DLTS for the electron trap E(0.38) in samples implanted with $2 \times 10^{15}$ Ge $cm^{-2}$ annealed at 1000 °C or 1100 °C.

located on the perimeter of the loops ($P_{tot}$, blue triangles). Because of the uncertainties related to the DLTS concentration values close to the surface region, we used the peak concentration value for the DLTS results (expressed in $cm^{-3}$) for the comparison, while the defect related parameters are expressed in $cm^{-2}$. For each group of samples, we therefore normalised each data set with respect to the sample containing the lowest amount of defects.

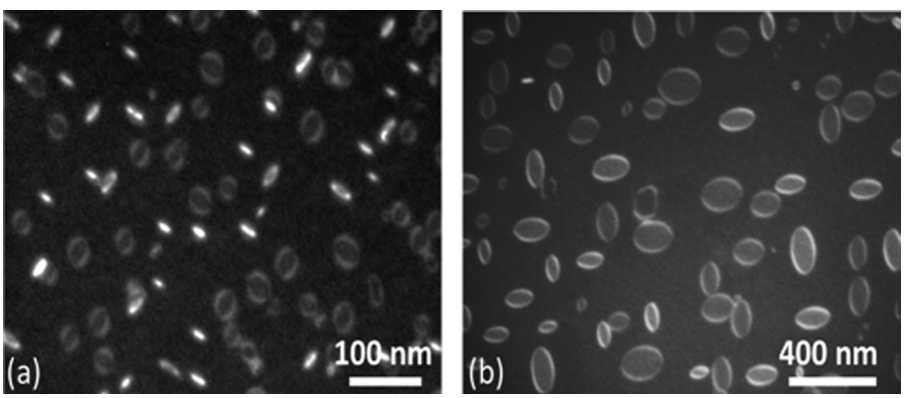


FIG. 10. TEM images for the Si samples implanted with $2 \times 10^{15}$ Ge $cm^{-2}$ and annealed at (a) 1000 °C and (b) 1100 °C.

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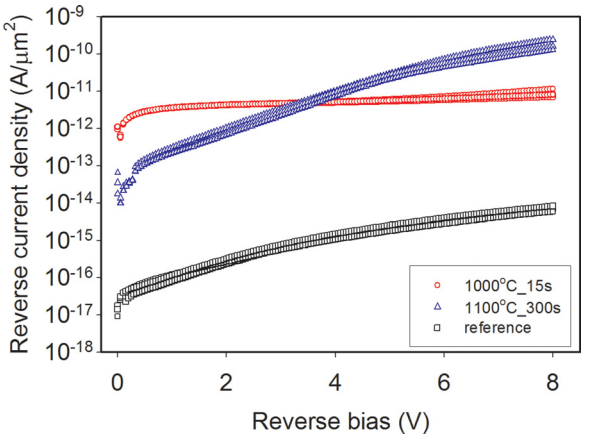


FIG. 13. Reverse leakage current versus reverse bias in the n-type reference sample and samples implanted with $2 \times 10^{15}$ Ge $cm^{-2}$ and annealed at 1000 °C or 1100 °C.

In the case of p-type samples (Fig. 11), the investigated samples strongly differ in the implant dose (by a factor of 4), with the low-dose sample annealed at a slightly higher temperature compared to the high-dose one (1050 °C vs. 1000 °C). Under such conditions, the variation of all three investigated parameters ($D_{Loop}$, $C_{Loop}$, and $P_{tot}$) correlates well (within the experimental errors) with the variation of the measured DLTS defect concentration, and no conclusion can be drawn on the structural origin of the electrical defects. In contrast, in the case of n-type samples (Fig. 12), the investigated samples received the same implant dose, and were annealed at different temperatures (1000 °C and 1100 °C). Under such conditions, the areal density of loops, $D_{Loop}$, is found to decrease more rapidly than the DLTS defect concentration when increasing the annealing temperature, while the areal density of all the Si interstitial atoms contained in the loops, $C_{Loops}$, is constant within the experimental errors (in agreement with a conservative Ostwald ripening process,[10] which is in disagreement with the decrease of the DLTS defect concentration). Finally, the variation of the areal density of Si interstitial atoms located on the perimeter of the loops, $P_{tot}$, closely follows the variation of the DLTS defect concentration, therefore suggesting that the measured DLTS signals originate from defects (i.e., deep levels) related to the atoms located on the loop perimeter.

### 2. Leakage currents in the presence of dislocation loops

In addition to the DLTS measurements discussed in Section II B 1 c, the test structures fabricated in this work were specifically designed to also allow reliable leakage current measurements in p-n or Schottky diode configurations, with the implant-induced defects being located inside the space charge region. Results from n-type and p-type diodes will be presented in the Subsections II B 2 a and II B 2 b, respectively. Additional results will be presented in Section II B 2 c from samples where the implant-induced defects are located in the neutral region below the SCR.

*a. EOR in the depletion region (n-type substrate).* The leakage current in n-type samples containing dislocation loops presented in Section II B 1 a is discussed first. The plots of the leakage current versus bias for the reference sample and samples implanted with $2 \times 10^{15}$ $cm^{-2}$ $Ge^{+}$ and annealed at 1000 °C and 1100 °C are shown in Fig. 13. A summary of the leakage current density at −0.5 V and −5 V, junction position from the surface ($X_j$), depletion width at 0 V and −0.5 V and defect density extracted from the TEM measurements are listed in Table II.

Due to the presence of defects, the leakage current density in the sample annealed at 1000 °C (recorded at reverse bias of 0.5 V) increases by 4 orders of magnitude compared to that in the reference sample. After increasing the annealing temperature from 1000 °C to 1100 °C, there is an order of magnitude decrease in the leakage current. This is consistent with the decrease in the DLTS defect concentration as the annealing temperature is increased (cf. Figs. 6 and 12). At higher electric fields (i.e., at a reverse bias of 5 V) the leakage in the 1100 °C sample becomes dominant which suggests other leakage sources. Indeed, the shallow doping profiles in Fig. 14 for the reference and samples annealed at 1000 °C and 1100 °C reveal that they are significantly modified upon annealing. In particular, the doping profile of the 1100 °C sample increases significantly towards the junction. This is a clear indication that the high leakage currents in the 1100 °C sample at elevated E-field values are dopant-related. The source of this rather strange modified dopant profile for the 1100 °C sample is not clear at the moment. Ryoo *et al.*[14] and Brotherton *et al.*[13] have shown that dislocation loops which are located on the highly doped side of the junction do not contribute to the leakage current, whereas the DLs in the neutral region contribute significantly to leakage and the greatest leakage was obtained when the defects are located in the space charge region.

In Section II B 1 c on DLTS analysis, we evidenced a possible direct relation between the concentration of electrical defects (concentration of DLTS centres) and the areal

TABLE II. Defect density and reverse current density at −0.5 V and −5 V for the $p^{+}n$ diodes (cf. Section II A, Table I for sample details). $X_j$ is the junction and A/C is the amorphous-crystalline interface from the semiconductor surface, whereas W is the depletion depth at 0 V and −0.5 V from the junction.

| Sample ID | [Anneal conditions][a] | $X_j$ (nm) | A/C (nm) | $W_{(0V\text{-bias})}$ (from $X_j$) (nm) | $W_{(-0.5V\text{-bias})}$ (from $X_j$) (nm) | [b]DLs density ($cm^{-2}$) | $I_R$ (0.5 V) ($A/\mu m^2$) | $I_R$ (5 V) ($A/\mu m^2$) |
|---|---|---|---|---|---|---|---|---|
| Reference | … | 200 | 620 | 430 | 600 | … | $4.5 \times 10^{-17}$ | $2.1 \times 10^{-15}$ |
| 1000 °C | 1000 °C/15 s | 200 | 620 | 430 | 600 | $2.9 \times 10^{10}$ | $2.9 \times 10^{-12}$ | $6.2 \times 10^{-12}$ |
| 1100 °C | 1100 °C/300 s | 200 | 620 | 430 | 600 | $2.8 \times 10^{9}$ | $1.2 \times 10^{-13}$ | $2.2 \times 10^{-11}$ |

[a]Post-implantation anneal for defect formation.
[b]Defect density extracted from TEM measurements.

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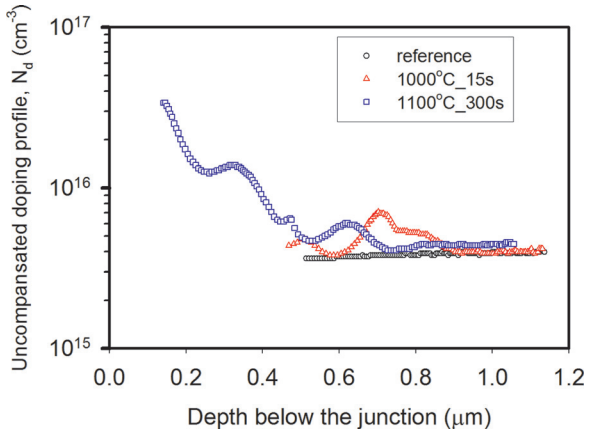


FIG. 14. Uncompensated doping profiles in the reference sample (circles-black) and samples implanted with $2 \times 10^{15}$ Ge $cm^{-2}$ and annealed at 1000 °C (triangles-red) or 1100 °C (squares-blue).

density of Si interstitial atoms located on the perimeter of the loops ($P_{tot}$, cf. Fig. 12). Here, it is not possible to directly compare leakage current values to defect population parameters, as several mechanisms may contribute to the leakage currents (including doping effect). However, the qualitative comparison of TEM data to leakage currents measured at −0.5 V, reported in Fig. 15, can be used to further support that, similarly to the DLTS signal, the leakage current is not related to $C_{Loop}$, i.e., the areal density of all the Si interstitial atoms contained in the loops. This parameter does not vary with annealing temperature (within the experimental errors), whereas the leakage current decreases by a factor of ∼20 when increasing the temperature by 100 °C.

*b. EOR in the depletion region (p-type substrate).* The leakage currents in the p-type silicon samples presented in Section II B 1 b with DLs in the depletion region are presented next. A summary of the samples considered for the leakage current investigation is presented in Table III. It must be noted that the leakage currents for these samples were recorded on Schottky diode structures.

Similarly to the n-type samples discussed in Section II B 2 a, the Shottky diodes show an increase in leakage current upon introduction of dislocation loops as depicted in Fig. 16. Again, the difference in leakage current measured in the two samples containing loops is consistent with the corresponding DLTS defect concentrations. Indeed, the sample implanted with the higher dose $2 \times 10^{15}$ Ge $cm^{-2}$ and annealed at 1000 °C exhibits a higher concentration of both structural and electrical defects (cf. Fig. 11) compared to the lower dose implanted sample ($5 \times 10^{14}$ Ge $cm^{-2}$), and hence a higher leakage current for all the investigated bias (up to −6 V). The corresponding *C-V* doping profiles for the samples are shown in Fig. 17 for comparison. The profiles are similar except for a "bump" in the sample implanted with $5 \times 10^{14}$ Ge $cm^{-2}$.

TABLE III. Reverse current density at −1 V and −5 V for the Schottky diodes (cf. Section II A, Table I for sample details).

| Ge dose ($cm^{-2}$) | [T (°C)][a] | $I_R$ (1 V) | $I_R$ (5 V) |
|---|---|---|---|
| Reference | … | $1.1 \times 10^{-15}$ | $2.6 \times 10^{-15}$ |
| $5 \times 10^{14}$ | 1050 °C/15 s | $8.8 \times 10^{-12}$ | $1.1 \times 10^{-11}$ |
| $2 \times 10^{15}$ | 1000 °C/15 s | $1.6 \times 10^{-10}$ | $3.6 \times 10^{-10}$ |

[a]Post-implantation anneal for defect formation.

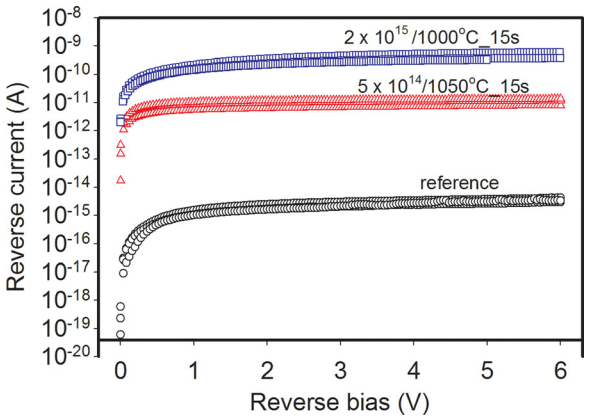


FIG. 16. Leakage current versus reverse bias in the p-type reference sample and samples implanted with $2 \times 10^{15}$ Ge $cm^{-2}$ and $5 \times 10^{14}$ Ge $cm^{-2}$.

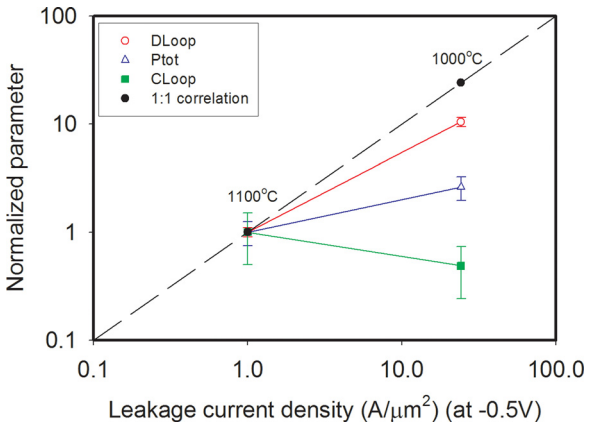


FIG. 15. Normalised defect properties ($D_{Loop}$, $C_{Loop}$, or $P_{tot}$) as a function of leakage current for the dislocation loops in the n-type Si samples annealed at 1000 °C and 1100 °C.

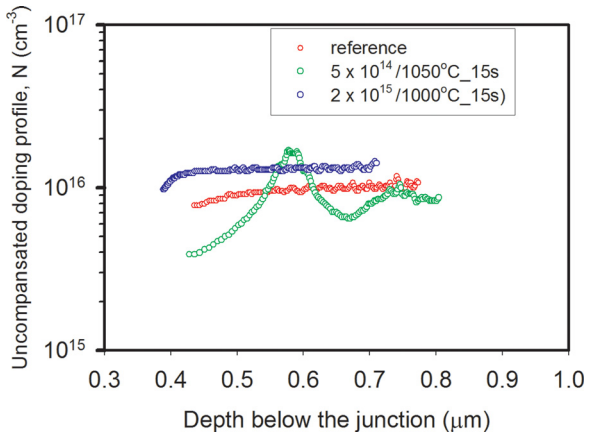


FIG. 17. Uncompensated doping profiles in the reference sample and samples implanted with $5 \times 10^{14}$ Ge $cm^{-2}$ and $2 \times 10^{15}$ Ge $cm^{-2}$ and annealed at 1000 °C.

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TABLE IV. Sample details and implantation conditions for $n^+p$ junction diodes with EOR in the neutral p-region.

| Sample ID | Implants | [T (°C)][a] | $X_j$ (nm) | B conc. at $x_j$ ($cm^{-3}$) | A/C (nm) | Defect type | [b]Total defect density ($cm^{-2}$) | $I_R$ (−0.5 V) | $I_R$ (−5 V) |
|---|---|---|---|---|---|---|---|---|---|
| A1 | … | 1100 °C/RTA | 310 | $9.0 \times 10^{17}$ | … | No defects | … | $1.7 \times 10^{-17}$ | $2.5 \times 10^{-13}$ |
| A2 | … | 1100 °C/RTA | 310 | $1.7 \times 10^{18}$ | … | No defects | … | $5.3 \times 10^{-17}$ | $1.2 \times 10^{-9}$ |
| B | Si | 1100 °C/RTA | 270 | $1.5 \times 10^{18}$ | 460 | DLs only | $3.56 \times 10^{10}$ | $3.7 \times 10^{-14}$ | $1.7 \times 10^{-10}$ |
| C | Si | 900 °C/5 s | 270 | $1.5 \times 10^{18}$ | 460 | DLs + 311 s | $1.15 \times 10^{11}$ | $3.5 \times 10^{-13}$ | $4.3 \times 10^{-10}$ |
| D | Si | 700 °C/30 s | 270 | $1.5 \times 10^{18}$ | 460 | 311 s only | $2.40 \times 10^{12}$ | $1.6 \times 10^{-12}$ | $4.8 \times 10^{-10}$ |

[a]Post-implantation anneal for defect formation.
[b]Total areal defect density (DLs + 311) extracted from TEM measurements.

*c. EOR in the neutral region (p-type substrate).* In this section, we present leakage current measurements performed on $n^+p$ diode structures, in which the implant-induced defects are located in the neutral p-region ($\sim 10^{18}\,cm^{-3}$) but close to the lower edge of the space charge region. Details of the investigated samples are given in Table IV (full description of the fabrication process is given in Ref. 19). In particular, in the diodes containing defects (samples B-D in Table IV), the metallurgical junction is located at about 270 nm below the surface and the lower edge of the space charge region is estimated at a depth of ∼330 nm at −1 V or ∼360 nm at −6 V, whereas the implant-induced defects occupy a layer extending from 410 nm to 520 nm. In such conditions, the defects are not included in the depletion region during the I-V measurements, with the possible exception of the highest measured bias (−6 V). Indeed, no DLTS signal related to the defects could be extracted in these diodes, unlike the cases described in Section II B 2 b.

The two defect-free reference diodes (A1 and A2 in Table IV) were fabricated with slightly different conditions compared to diodes B-D, leading to boron concentrations in the p-doped side of the junction either lower (A1) or higher (A2) than the diodes containing defects.

The leakage currents as a function of bias for samples (A-D) are depicted in Fig. 18. The graphs clearly show that at low fields (below 3 V) the diodes containing defects exhibit higher leakage currents compared to the reference diodes, and this is despite the fact that the defects are all located in the neutral region at such voltages. The highest leakage current is measured in diode D, which received the lowest thermal budget during the activation anneal. At higher voltages, the leakage increase in diodes containing defects is weaker, while the leakage currents from B-D diodes become similar to each other and close to one of the reference diodes (A2).

Finally, as shown in Fig. 15 for leakage currents generated by dislocation loops located inside the SCR of $p^+$-n diodes, the qualitative comparison of TEM data to the measured leakage currents is reported in Fig. 19 and clearly indicates that, although in this case the defects are located outside the space charge region (i.e., they are not expected to directly induce an increase in leakage current), the variation of the measured leakage correlates well with either the areal density of defects, $D_{Loop}$, or the areal density of the atoms located in the defects perimeter ($P_{tot}$).

*d. Discussion.* For the investigation of diodes containing implant defects (loops) within the space charge region (Sections II B 2 a and II B 2 b), the doping concentration in the low-doped side of the junction was always lower or equal to $1 \times 10^{16}$ $cm^{-3}$. In such conditions, the current-voltage (IV) measurements of the reference defect-free structures showed a low reverse leakage in all cases as expected (i.e., less than $10^{-14}$ $A/\mu m^2$, cf. Figs. 13 and 16)). When the loops are formed inside the space charge region, the increase in leakage current can therefore be directly attributed to the electrically active defect levels induced in the band gap by the loops. In samples containing loops, we found that the deepest levels are E(0.38) and H(0.25) for the electron trap and hole trap, respectively. Therefore, these levels are most

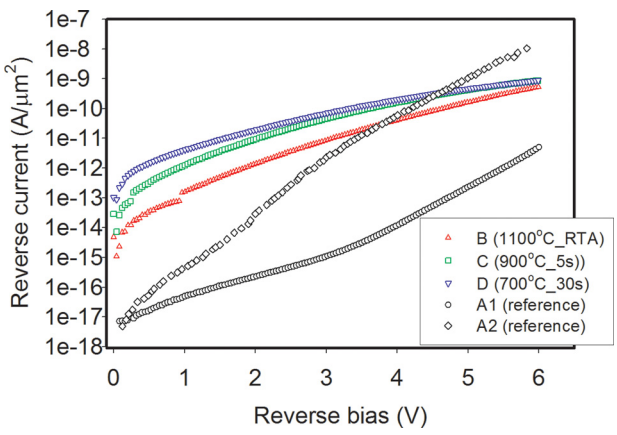


FIG. 18. Reverse leakage current in the reference samples (A1 and A2) and in samples with EOR defects and annealed at 1100 °C (B), 900 °C (C), and 700 °C (D).

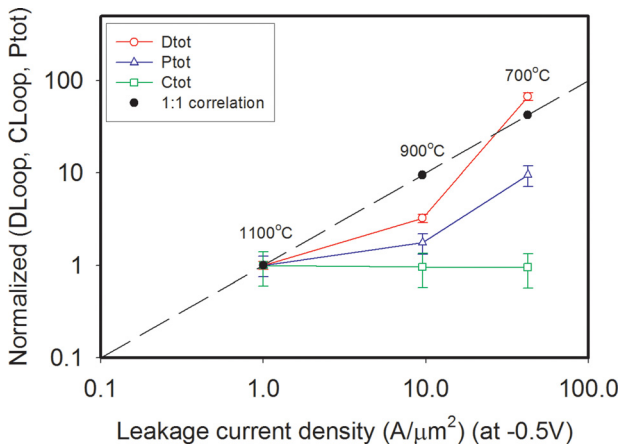


FIG. 19. Normalised defect properties ($D_{tot}$, $C_{tot}$, or $P_{tot}$) as a function of leakage current for the $n^+p$ diodes with EOR in the neutral region.

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probably related to the observed increase in leakage current. Leakage current simulations based on these energy levels will be presented and discussed in Section III.

For the investigation of diodes containing implant defects ({311}s and/or loops) in the neutral regions (Section II B 2 c), the doping concentration in the low-doped side of the junction was higher than the previous investigations (i.e., close to $1 \times 10^{18}\,cm^{-3}$). Such high doping levels are known to induce a strong increase in leakage currents.[19] Indeed, even in the absence of defects (reference samples A1 and A2, Fig. 18), leakage currents up to $1 \times 10^{-10}\,A/\mu m^2$ were recorded. Yet, when compared to diodes containing defects (curves B-D in Fig. 18) a clear increase in leakage current is observed, at least for low reverse bias (less than 3 V). At these bias values, the implant defects are still located in the neutral p-doped region (i.e., outside the SCR), as suggested by process simulations and by the absence of the DLTS signal in these structures.

Several studies have been published about the impact of the defect position on leakage currents,[13,14,19–21] where the implant defects were located either inside the space charge region or in the highly doped side of the junction. In the work of Ryoo *et al.*,[14] one of the investigated samples contained implant defects (loops) located in the neutral low-doped region of the junction at 0 V bias. However, within the voltage range investigated in that work (0–100 V), a low bias (estimated at less than 10 V by the authors) was sufficient to incorporate the loops in the depletion region. The measured leakage currents in all those works were therefore interpreted as a direct effect of the electrically active defects associated to the loops present inside the space charge region, similar to the results we found in Sections II B 2 a and II B 2 b.

In contrast, the mechanism by which a significant increase in leakage current occurs in diodes containing defects in the neutral region (such as those investigated in Section II B 2 c) and the possible role of the defects in the observed leakage increase is still unclear. Following the amorphising implant, the induced primary point defects (interstitial and vacancies) can interact with existing impurities (oxygen, carbon) or getter metal impurities introduced during diode fabrication and generate a huge variety of electrically active defects, whose associated energy levels have been deeply investigated,[22] and that can act as generation centers responsible for increased leakage currents. However, most of these defects anneal out at much lower temperatures (i.e., 450 K for the group V-vacancy "E centre")[23] than those used to form the extended defects in our structures (700 °C–1100 °C), so that such mechanism can be excluded in our case. Similarly, the defect formation anneal is performed prior to the low-temperature diode fabrication process, so that metal impurity gettering can also be excluded. Finally, a possible mechanism by which implant defects might have an indirect impact on leakage currents is based on their doping behaviour. The electronic properties of extended defects, particularly loops, have been investigated in depth,[24] and in some cases a clear donor behaviour was observed for implant-induced dislocation loops.[11] It can be speculated that the doping behaviour of the implant induced defects might result in a modification of the local doping concentration in the region containing the defects, and therefore enhance the leakage current mechanisms based on the dopant related mechanism. This would be in agreement with the absence of DLTS signals in the investigated diodes, however further work will be necessary to explore and validate such hypothesis.

## III. PHYSICAL MODELING

### A. Introduction

For the obtained results to be of noteworthy significance, especially for the application in industrial research and development (R&D) processes, the implications of the experimental results must be made available in terms of usable models. This part of the paper discusses the modelling used to describe the electrical activity of the dislocation loops (DLs). The modelling is partially based on investigations about extended dislocation defects conducted by Read.[25] The technique used to perform the DLTS simulations is explained and the simulation results are compared to the measurements presented in the first part of the paper. Furthermore, the possible approaches to use the latter findings in order to perform leakage simulations are presented and discussed.

### B. DLTS simulations

The concept used to simulate DLTS measurements has been extensively discussed in Ref. 26 and a variety of alternative approaches to compute or simulate the DLTS signal have been proposed and investigated.[27,28] A summary of the simulation approach results is given in the schematic illustration of Fig. 20. The diagram shows the simulation flow used to calculate a DLTS signal from a process-simulated device structure with non-homogeneous defect-, dopant- and charge carrier concentrations. The process simulations were carried out using *Sentaurus-Process* (S-Process)[29] and the simulation of the self-consistent, stationary electrostatics was performed with Sentaurus-Device (S-Device).[30]

This simulation strategy allows simulations for realistic use cases, which lie beyond the scope of purely analytical solutions.

The simulation of the DLTS signal (as it is shown in Fig. 21 for the $E_T = E_C - 0.35\,eV$ energy level) helps to understand important key properties of the EDs.

In contrast to the case of normal point-like and uniformly distributed defects one has to account for additional effects. For a defect concentration of $N = 10^{15}\,cm^{-3}$, the average mutual distance between two defects is on the order of 60 nm. The influence of a charged defect on the neighbouring defect can be neglected in this case. However, when considering extended defects the distance from one defect site to the neighbouring defect can be as short as 1 nm, and, therefore, Coulomb interactions between charged defect sites must be considered. The inclusion of the Coulomb interaction in the carrier capture and emission expressions ($e_n$, $e_p$, $c_n$, $c_p$) readily broadens the peak towards low temperatures. This could not be captured with the energy band model applied in Section II (cf. Figs. 4 and 8) and is a direct consequence of the lowering of the thermal energy barrier in the emission expression due to the Coulomb repulsion.

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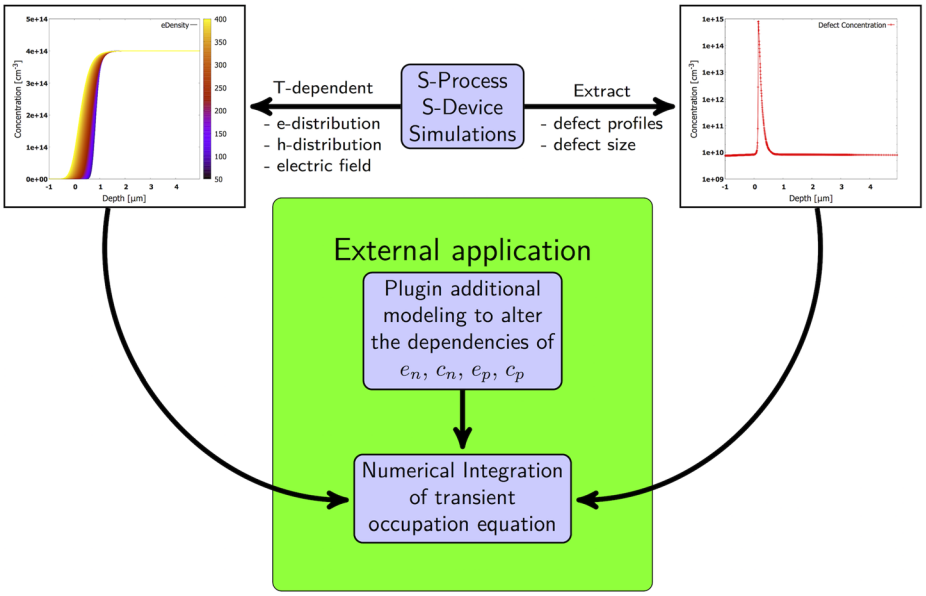


FIG. 20. A schematic illustration of the simulation process for DLTS signals. Defect profiles obtained from process simulations and free charge-carrier profiles obtained from stationary device simulations are used to simulate the transient development of the defect states. From A. Scheinemann, *Modelling of Leakage Currents Induced by Extended Defects in Extra-Functionality Devices*, Series in Microelectronics Vol. 238, p. 47. Copyright 2014 Hartung-Gorre Konstanz. Reprinted with permission from Hartung-Gorre Konstanz.

Furthermore, it is observed that the inclusion of the Coulomb repulsion alters the peak position with respect to the peak obtained when the Coulomb repulsion is neglected or if an analytical solution is used. Similar to the peak broadening discussed above, the shift of the peak also occurs towards lower temperatures.

### C. Simulation of leakage currents

With this newly developed DLTS simulation technique, it is now possible to investigate in detail the impact of extended defects on the electrical properties of pn-junctions, including the difficult challenge of finding a plausible explanation for the increased leakage currents measured in samples containing dislocation loops. To this purpose, two different strategies are proposed and discussed in Sections III C 1 and III C 2.

#### *1. Leakage through mid-gap level*

The simplest way to explain the observed leakage currents is to assume that a deep mid-gap defect level is associated to the dislocation loops, which for various possible reasons may not be resolved by the DLTS measurements (only shallower E(0.38) and H(0.25) levels were observed, cf. Section II). One of these reasons might be a possible coupling of the mid-gap level to one of the shallower levels, leading to the masking of the deeper level, as shown in Ref. 31. Obviously, if the presence of a mid-gap level is assumed, it should still be related to the presence of the DLs, since the leakage increases upon introduction of DLs into the sample. The defect profiles obtained from process simulations with S-Process (using the model by Zographos *et al.*[32]) are, therefore, adjusted to match the actually determined total concentration measured by TEM and are then used for device simulation. As a starting point, typical parameters of a mid-gap recombination centre in Si are used: $E_T = E_C - 0.55\,eV$, $\sigma_n = \sigma_p = 10^{-15}\,cm^2$. Measured capture cross sections cover a wide range (Refs. 33 and 34) and $\sigma_n$ may differ from $\sigma_p$ by orders of magnitude. The value of $10^{-15}\,cm^2$ is an "average" and is provided in S-Device as a default value. The first step is to fit the IV characteristics of the reference sample. This is achieved by defining a uniform defect distribution with a defect concentration of $N_D = 7 \times 10^{14}\,cm^{-3}$. The uniform defect distribution and the extended defects are considered as independent SRH recombination channels. Since in the reference sample there is no amorphising implant, no current is obtained from the defects defined through the dislocation loops, because their concentration is almost zero. In the case of implanted samples, the current contributions of the uniform defect distribution can be neglected compared to the major contributions of the high concentration of DLs. All simulated IV characteristics had the same command file set up and used the same parameters for the electrical simulation, the only difference lies in the different process simulation outputs. However, with such parameters one fails to reproduce the measured leakage currents of the $n^+p$ diode implanted with Ge at a dose of $10^{15}\,cm^{-2}$ by a factor of ~20. In the plots of Fig. 22 this factor was included by increasing the capture cross sections by a factor of 20 to match the

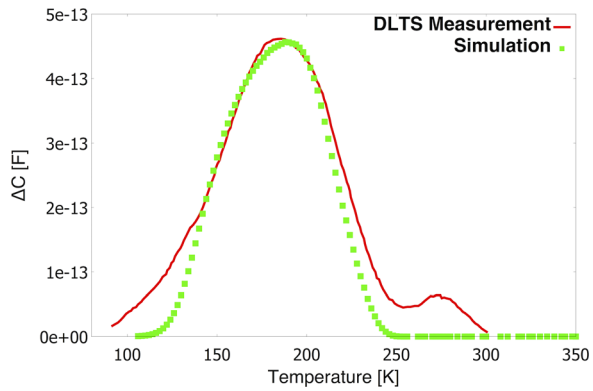


FIG. 21. DLTS simulation of defect level $E_T = E_C - 0.35\,eV$ with $\sigma_n = \sigma_p = 10^{-15}\,cm^2$. The energy level is adapted from E(0.35) to E(0.40) in order to recover for the DLTS peak shift that occurs when the Coulomb repulsion is included for the DLs.

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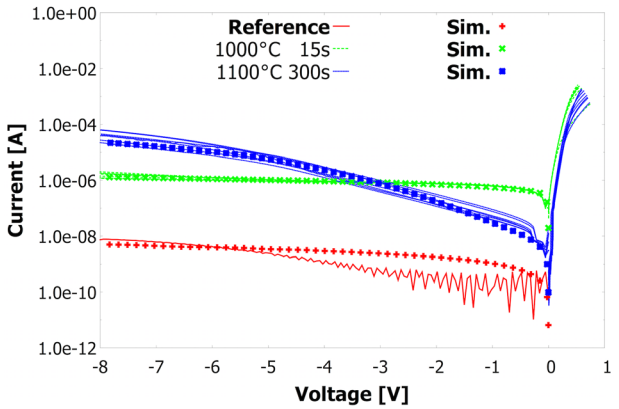


FIG. 22. Comparison between leakage measurements and simulations of the $2 \times 10^{15}\,\mathrm{cm}^{-2}$ Ge implanted n-type samples shown in Fig. 13. The concentration of atoms at the periphery of the DLs was used as defect concentration. The simulated concentration of active doping was manually corrected to account for the higher doping found by the CV measurements presented in Fig. 14.

measurements performed on $p^+n$-junctions containing DLs formed at 1000 °C or 1100 °C. The increase of the capture cross section had no impact on the reference sample, since the contribution of the DLs to the leakage current is negligible.

This failure might arise from the fact that the number of electrically active centres, though proportional to the number of atoms at the periphery (as suggested by DLTS and leakage current measurements, cf. Section II), could in absolute terms be higher than the absolute amount of peripheral atoms. Several studies (Refs. 35 and 36) indicate the close relation between metallic impurities being accumulated at dislocation defects and the presence of deep levels in the band gap which in turn lead to a reduction of free carrier lifetimes. It was not possible to correlate analytically the dislocation defect densities to the densities of impurities. But it cannot be ruled out that there might be more impurities bound to the dislocation loop than there are peripheral sites on this same loop.

Another possible reason for the misfit is of course that the assumed capture cross sections are not extracted from experimental data. It seems appropriate to simply increase the capture cross sections. On the other hand, it must be considered that an increase of the capture cross section to values of $\sigma = 2 \times 10^{-14}$ cm$^2$ means that the capture cross sections of neighbouring defects will overlap.

Apart from the absolute values of the leakage currents which can be fitted with increased capture cross-sections, it is found that the field dependence of the leakage current curves is reproduced remarkably well. The increased field dependence of the 1100 °C sample is not so much caused by the presence of DLs, but by the increased levels of active doping (cf. Fig. 14) which lead to high field strengths and, thus, to trap-assisted tunnelling. In contrast, the 1000 °C sample exhibits a very weak field dependence, which is in good agreement with the defect profile of the DLs. Indeed, at zero bias, the depletion region extends from about 200 nm down to almost the peak of the EOR defect profile (~600 nm), such that, at small biases, the peak is already completely located inside the depletion region. From this point, a further increase in the bias voltage does not increase the number of defects in the depletion region and, hence, the current as well does not significantly increase. This is another argument for the correctness of the assumption that the current is related to the presence of the DLs.

### 2. Leakage through coupled defect levels

If one does not want to make any assumptions on additional defect levels that could not be detected by DLTS, the measured leakage current should be explained on the basis of the levels that were experimentally found in samples containing DLs. When considered as independent recombination centres, neither the E(0.38) nor the H(0.25) level can generate a significant contribution to the measured leakage current. One possible way to obtain an increased current from these two levels is to use the Coupled Defect Level[37] (CDL) model available in S-Device. The carrier lifetimes are determined based on the peak defect concentration (extracted from the DLTS measurement and the measured capture cross section) as

$$\tau_\nu = N\, v_\nu\, \sigma_\nu,$$

where $N$ is the defect concentration, $v$ is the thermal velocity, and $\sigma$ is the capture cross-section for the respective charge carriers. The index $\nu$ indicates the actual carrier type, either electron or hole.

Since the defect concentration $N$ was extracted from DLTS measurements, it is appropriate to add a further consideration regarding this parameter. For a common point defect the occupation can be directly computed with

$$f = \frac{c_\nu(T)}{c_\nu(T) + e_\nu(T)}.$$

If the Coulomb repulsion is included in the expression for the emission to account for the extended nature of DLs, the occupation can no longer be computed directly since the emission depends on the occupation number $f$. It can, however, be found by an iteration scheme.

The result of such a computation is shown in Fig. 23. It can be seen that in the case of DLs (green line) the occupation probability of the defect population does not reach unity, because the emission drastically rises upon charging of the defect and inhibits further charging of the defect. This result implies that during the DLTS measurement of the DLs we only see a fraction of the electrically active defects, which were actually charged with a trapped carrier according to the occupation probability $f$. In the $p^+n$-junction devices investigated here, the ratio between full occupation and actual occupation was found to be about one order of magnitude. With this correction applied to the measured defect concentration, the simulation with the CDL model yields the results shown in Fig. 24.

Similar to the previous case (mid-gap level assumption), it is found that simulations based on the CDL model also reproduce well the field dependence of the leakage current curves, indicating that leakage currents can indeed be

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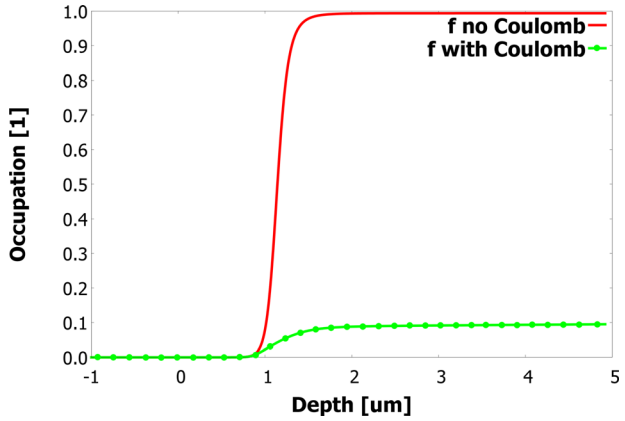


FIG. 23. Computed occupation probability for a defect population in a 1D device when considered as point-like defects (red line) or as dislocation loop (green line).

successfully simulated on the exclusive basis of the experimentally observed energy levels (i.e., with no need of assuming additional defect levels, which were not confirmed by the measurement). Also, it is important to note that this promising result is achieved in spite of a limitation associated to the implementation of the CDL model in the TCAD tool used in this work. In fact, the CDL model in S-Device cannot be used in conjunction with a depth-dependent defect profile for the computation of the coupled recombination (which was possible for the mid-gap level simulations, cf. Fig. 22). Instead, we used a constant and homogeneous defect concentration for the CDL simulations, which was obtained from DLTS measurements and corrected by the previously described factor $\frac{f_{Coulomb}}{f_{no\,Coulomb}}$.

### D. Discussion

The performed DLTS simulations result in a peak broadening which is strong enough to explain the observed broadening of DLTS peaks in the presence of extended defects. Besides the effects seen on the DLTS signals, other conclusions can be drawn, which directly impact the subsequent leakage current simulations. The obtained results offer the possibility to estimate the size of leakage currents in devices

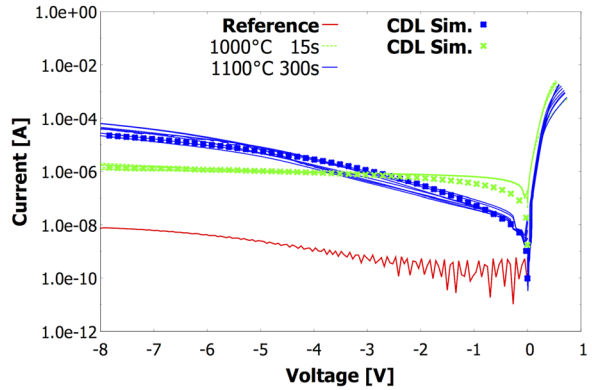


FIG. 24. Simulation of the same samples as in Fig. 22. Defect levels E(0.38) and H(0.25) are coupled using the CDL model in S-Device. Simulations were performed with the Huang-Rhys factor set to S = 1 and tunnelling masses of $m_{\Theta,e} = 0.22\ m_0$ and $m_{\Theta,h} = 0.21\ m_0$.

which contain extended defects after processing. This estimation can be made depending on the size, concentration and geometry of the underlying defects.

## IV. CONCLUSIONS

In this work, we have investigated the electrical properties of dislocation loops and their role in the generation of leakage currents in pn- or Schottky junctions both experimentally and through simulations.

Dislocation loops introduce a significant increase in leakage currents when they are located in the depletion region. This has been attributed to two broad defect peaks located at $E_c - 0.38$ eV (electron trap) and $E_v + 0.25$ eV (hole trap). The leakage current also increased significantly with an increase in the dislocation concentration. Based on the comparison between structural defect parameters extracted from TEM and electrical defect concentrations extracted from DLTS, it is concluded that the defects related to the atoms located on the loop perimeter are the likely sources of the measured DLTS signals. Further investigations are necessary to understand effects like the elevated leakage currents in the case where the defects are not located in the depletion region.

Despite some open questions remaining, the combined use of defect models and recently developed DLTS simulation offers new possibilities to describe the electrical activity of extended defects and allows reducing the number of assumptions and fitting parameters needed for the simulation of leakage currents, therefore improving their predictability.

Two different approaches were discussed to perform leakage simulations. We found that simulations based on the CDL model reproduce well the leakage current values and their field dependence behaviour, indicating that leakage currents can indeed be successfully simulated on the exclusive basis of the experimentally observed energy levels.

## ACKNOWLEDGMENTS

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement No. 258547 (ATEMOX). Special thanks go to Ray Duffy for his long and inspiring discussions throughout this work.

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