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## Toward Successful Integration of Porous Low-k Materials: Strategies Addressing Plasma Damage

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The increasing sensitivity of porous low dielectric constant materials to process damage constitutes a major roadblock to their implementation in back-end-of-the-line (BEOL) wiring structures for advanced technology nodes. In the early 2000s and in anticipation to future low-k related integration challenges, the semiconductor industry started to investigate the possibility to repair or prevent this damage. It is remarkable that the most disruptive solutions proposed today are inspired from the work initiated more than 10 years ago. In this review we first describe the accepted mechanisms for plasma damage, followed by a quick summary of the methods used to quantify its extent on both blanket films and patterned structures. We then report on the past and current strategies developed to mitigate the plasma damage of porous, low-k materials during damascene integration processes.

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The integration of insulators with decreasing dielectric constants,  $k$ , in modern microelectronic devices has been critical in maintaining and improving their performance from one generation to the next.<sup>1,2</sup> The initial strategy of increasing the carbon content and later by introducing porosity (air) to lower the dielectric constant of the insulating material were adopted early on. This was in large part due to the fact that it seemingly provided a long-term pathway for generational extendibility. However, it was also acknowledged that the convergence of increasing porosity and decreasing device feature sizes would ultimately lead to severe integration issues for dielectric insulators with  $k < 2.7$ .<sup>3-6</sup>

The resulting structural changes in both density and network-connectivity (as compared to  $\text{SiO}_2$ ) negatively impacted the mechanical properties of the porous low- $k$  materials,<sup>7-13</sup> leading in some cases to drastic failure during chip packaging.<sup>14</sup> This is currently solved by chip design, post-deposition treatments of existing low- $k$  materials with a thermal ultraviolet (UV) source<sup>15,16</sup> or laser spike annealing (LSA)<sup>17</sup> and through the development of carbon-bridged materials with superior mechanical properties at a given  $k$ .<sup>18-23</sup>

While the decrease in mechanical properties has been successfully addressed, integration problems related to the increased porosity with decreasing  $k$  are still pending. In case of the latter, the huge increase in accessible surface area leads to integration related damage, such as material modification occurring during exposure to plasma and wet chemical processes.<sup>5,24-28</sup> Chemically, such damage typically corresponds to a loss of carbon groups and the formation of Si-OH units, see Figure 1. As a result, the insulator electrical properties, such as dielectric constant, leakage current and breakdown voltage are significantly compromised. If not addressed, these changes would lead to device failure during reliability qualification.

In this paper, we discuss the past and current strategies developed to mitigate the plasma damage of porous, low- $k$  materials during damascene-type integration processes. We first describe the known, proposed plasma damage mechanisms, followed by methods used to evidence this damage on both blanket films and patterned structures. In the second part, we discuss the different approaches evaluated to address topics such as repair of material damage after processing or alternatively preventing the damage in the first place.<sup>29-32</sup>

It is worth noting that the semiconductor industry started to investigate some of these topics as early as 2000; however, due to the lack

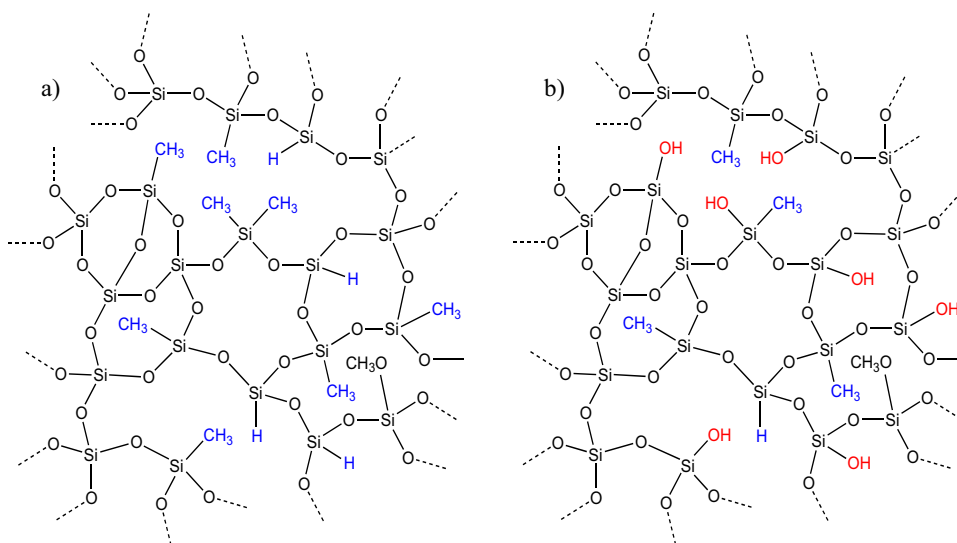
of success with the early approaches and the urgent need for solutions, it is only recently that disruptive approaches have been proposed (see Figure 2).

### Damage Mechanisms

During integration, the low- $k$  dielectric material is exposed to various damaging plasma processes. These plasma steps can be divided into two categories: plasma etching steps and post etch plasma treatments.

Plasma etching steps are used to transfer the patterns from a mask to a material of interest. For interconnect fabrication, porous low- $k$  dielectrics are exposed to plasma etching steps intended to etch the porous low- $k$  (the footprint of either the metal line or the via) and the dielectric barrier (typically SiCN). In both cases, capacitive fluorocarbon-based plasmas can be combined with additional gases such as Ar or  $\text{N}_2$ . Depending on the carbon to fluorine ratio in the feed-gas fluorocarbon molecule, the plasma will be more (for large [C]/[F] ratio) or less (for [C]/[F] close to 1/4) polymerizing.<sup>33,34</sup> When the porous low- $k$  dielectric is exposed to such plasmas, photons and radicals may damage both the exposed sidewalls and the etch front. Moreover, ions with grazing angle incidence may damage the sidewalls while higher energy ions with normal incidence damage the etch front.<sup>34-37</sup> The synergy between radicals, photons and ions leads to a partial modification of the porous low- $k$  dielectric with some carbon depletion and formation of Si-F and Si-OH terminal groups, which facilitate water uptake.<sup>34,38</sup> When the plasma is sufficiently polymerizing, deposition of fluorocarbon species at the sidewalls limits the species diffusion and reduces the plasma-induced damage.<sup>34,39</sup> At the etch front, normal incidence ion bombardment breaks bonds which releases H and O radicals that can eventually damage the low- $k$ . It also leads to surface densification that reduces the diffusion velocity.<sup>40</sup> It is also possible that etching may partially consume the damaged layer, thus minimizing the plasma-induced damage.<sup>38</sup> During porous low- $k$  etching, a strong surface roughness builds up at the etch front because of surface densification and material modification creating an uneven surface density and composition.<sup>25,41</sup> When polymerizing etching processes without oxygen are used, the plasma-induced damage can be minimized. In more recent years, special attention has been paid to the impact of V-UV only to the ULK physical properties. It was demonstrated that no structural or chemical modifications are done to the low- $k$  material upon V-UV only exposure, but trapped charge

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**Figure 1.** a) Idealized chemical structure of low-k organosilicate materials before plasma damage and b) same structure after plasma damage.

accumulation occurs, affecting its electrical properties (capacitance, breakdown voltage and leakage current).<sup>42</sup>

Post etch plasma treatments are performed after porous low-k patterning and may have several purposes such as organic materials removal (i.e. photoresist), surface cleaning, pore sealing, defluorination or residue prevention. These plasma processes are usually either oxygen-based (oxidizing plasmas) or hydrogen-based (reducing plasmas). With oxygen-based plasmas, the highly reactive O radicals from the plasma can diffuse inside the pores and convert the Si-CH<sub>3</sub> terminal bonds into hydrophilic Si-OH terminal bonds.<sup>38,43</sup> This modification is larger for highly porous materials and is favored by a high oxygen radicals density in the plasma.<sup>44</sup> Hydrogen-based plasmas are much less damaging than oxidizing plasmas; nevertheless, hydrogen radicals can still partially damage porous low-k dielectrics, particularly when V-UV photons assist the breaking of chemical bonds.<sup>37,38,43,44</sup>

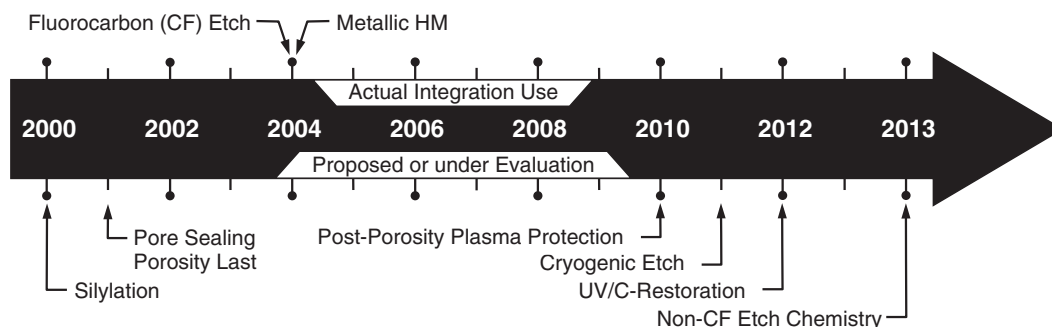
In addition to plasma related steps, porous low-k dielectrics may also be damaged during the other processing steps required for the integration. During the metallic barrier deposition, metallic precursors can diffuse inside the pores and modify the material.<sup>45</sup> However, current metallic barriers used to prevent Cu diffusion in the ULK are deposited by PVD, a process that minimizes barrier ingress into the ULK porosity as opposed to precursor diffusion observed with ALD. During the chemical-mechanical planarization (CMP) step, when the surface of the porous low-k dielectric is revealed (so-called direct CMP), surfactants from the CMP slurry can diffuse inside the pores and create hydrophilic sites inside the pores that lead to moisture uptake.<sup>46-48</sup> In manufacturing, the top surface of the low-k remains

capped while undergoing conventional CMP processes, preventing the issues described above.

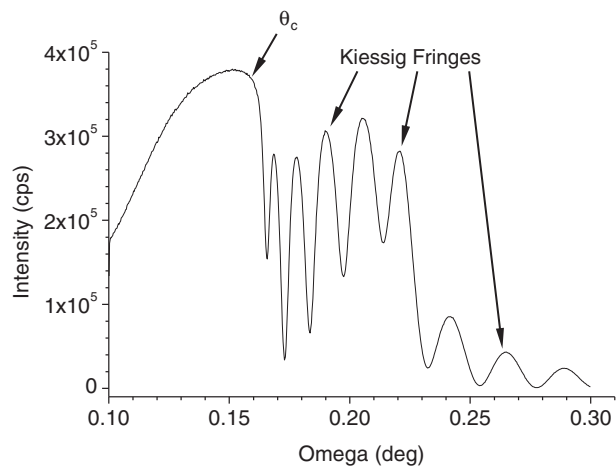
In summary, the major issue with respect to porous low-k damage during any processing step is the diffusion of reactive species into the pores that can then modify the material and change its near-surface and bulk properties.

### Damage Characterization

*Methodologies on blanket films.—Plasma induced damage.—* One simple and easily reproducible way of assessing low-k dielectric plasma resistance is the plasma induced damage (PID) test. As an example, pristine low-k films are exposed to an aggressive plasma (O<sub>2</sub> or NH<sub>3</sub> type), which mimics the integration ashing step where the photoresist is removed. During this step the low-k material's organic content at the top-surface is lost due to chemical modification and in addition, pores may collapse. As a consequence, the pristine top-surface is transformed into a dense, hydrophilic, SiO<sub>2</sub>-like layer. The plasma treated material is then dipped in a solution of 1/300 (wt/wt) dilute aqueous hydrofluoric acid (DHF) for 60 seconds, which dissolves the hydrophilic damaged layer at a rate orders of magnitude higher than the hydrophobic, pristine material. Following the DHF rinse, the total thickness loss  $t_{\text{pristine}} - t_{\text{after plasma+DHF rinse}}$  is measured. The PID can then be expressed as: i) the total thickness loss ii) the ratio of total thickness loss over the initial film thickness or iii) a value normalized to a standard material of known PID, which is the preferred methodology in the semiconductor industry.



**Figure 2.** Timeline of strategies investigated to mitigate plasma damage in dielectric insulators; top – date of manufacturing implementation, bottom – date first reported.



**Figure 3.** Typical XRR scan of a 150nm thick spin-on,  $k = 2.3$  dielectric film.

**Fourier transform infrared spectroscopy.**—Fourier transform infrared (FTIR) spectroscopy is a common technique employed to characterize the structure of organosilicate-based, porous low- $k$  dielectrics.<sup>49</sup> Absorption bands from Si-O-Si and Si-CH<sub>3</sub> groups located at  $\sim 950$ - $1250$  and  $\sim 1273$   $\text{cm}^{-1}$  are representative of methyl silsesquioxane materials. In the case of low- $k$  materials containing carbon bridges, the bands at  $1365$  and  $1409$   $\text{cm}^{-1}$  are associated with C-H vibrations for Si-CH<sub>2</sub>-Si and Si-CH<sub>2</sub>CH<sub>2</sub>-Si, respectively. While the  $1365$   $\text{cm}^{-1}$  band is unique to the single-carbon bridge, bands located around  $1400$   $\text{cm}^{-1}$  and  $1250$   $\text{cm}^{-1}$  can be attributed to both two-carbon bridges and pending Si-CH<sub>3</sub> groups. As of today, the carbon depletion occurring during exposure to plasma processes has primarily focused on the reduction of the Si-CH<sub>3</sub> absorption band at  $\sim 1273$   $\text{cm}^{-1}$ . Additional post-etch absorption bands at  $930$ ,  $960$  and between  $\sim 3000$  and  $\sim 3700$   $\text{cm}^{-1}$  may also be detected and represent Si-F, Si-OH and -OH bonds, respectively.<sup>34,50</sup>

Experimentally, the ambient atmosphere should be precisely controlled during the characterization since damaged porous low- $k$  are highly sensitive to humidity.<sup>51</sup> For thin film analysis, FTIR sensitivity can be improved by working in attenuated total reflectance (ATR) or multiple internal reflection (MIR) mode.<sup>52,53</sup>

**X-ray reflectivity.**—X-Ray reflectivity (XRR) is a method that involves exposing a sample to a monochromatic X-ray beam, at grazing incident angles (typically  $0^\circ$ - $5^\circ$ ) and monitoring the intensity of the reflected beam in the specular direction. The reflections at the surface and interfaces rely on Fresnel equations and are ruled by the electron densities in the different layers. A typical XRR scan is shown Figure 3: when the incident angle is below a critical angle,  $\theta_c$ , the

**Table I.** Fitting data of a  $k = 2.2$ , low- $k$  dielectric material before and after O<sub>2</sub> plasma treatment (5sec, 600W).

Fitting Model	Low- $k$ Material (undamaged)		Low- $k$ Material (O <sub>2</sub> Plasma-treated)	
	$t$ (nm)	$\rho$ ( $\text{g}/\text{cm}^3$ )	$t$ (nm)	$\rho$ ( $\text{g}/\text{cm}^3$ )
Layer 3	-	-	7	2.20
Layer 2	-	-	20	1.64
Layer 1	592	1.09	554	1.09

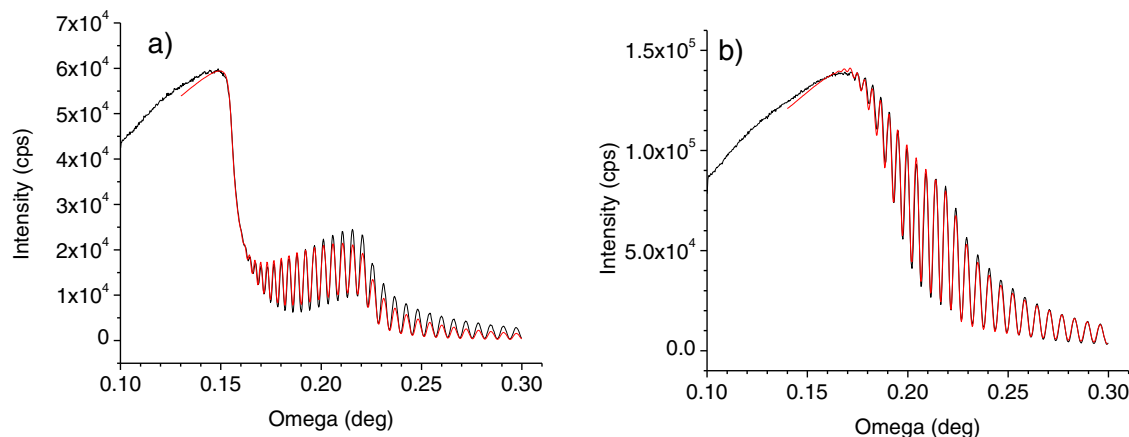
X-ray beam is totally reflected by the sample surface. When  $\theta$  reaches  $\theta_c$ , part of the X-ray beam penetrates into the film, leading to an initial, sharp drop in intensity. Above  $\theta_c$ , reflections at the different interfaces occur and as a consequence interference fringes are obtained (referred to as Kiessig fringes).  $\theta_c$  varies depending on the sample but it is usually below  $0.2^\circ$  for porous low- $k$  materials and it is directly related to the film density. The film thickness and roughness can be determined from the periodicity and change in intensity of the Kiessig fringes, respectively.

Practically, the sample's density, thickness and roughness of the different layers of a sample are determined through software data fitting. It is worth mentioning that a good knowledge of the sample (in terms of deposition conditions and processing history) is important information to enable the choice of a realistic fitting model.

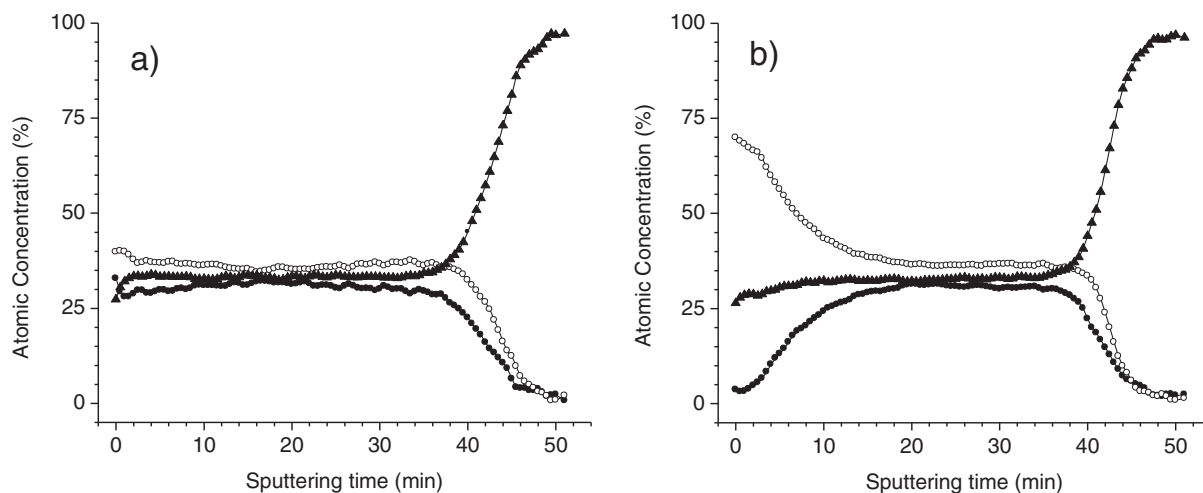
XRR is used to characterize both pristine and damaged low- $k$  materials. In the first case, the low- $k$  material density is constant throughout the film thickness and the data can be fitted using a 1-layer model (Fig. 4a). For comparison, the XRR scan of the same dielectric material after O<sub>2</sub> plasma treatment (600W, 5sec) is presented Fig. 4b.

In case of the latter, several observations can be made:  $\theta_c$  is shifted toward higher angles, the drop in intensity at  $\theta_c$  is not as sharp and the fringes and  $\theta_c$  overlap. In that case, multi-layer models are required to accurately fit the data, as exemplified in Table I.

Layer 1 displays a density identical to that of the pristine low- $k$  material, indicating that the bottom part of the plasma treated film was preserved. Since damage was located at the top-portion of the film, two supplemental layers (referred to as layer 2 and layer 3) with increasing density were added to properly fit the scan. Several conclusions can be drawn from this model. First, the use of two additional layers with increasing density to fit the plasma damage indicates that the latter is not homogeneous throughout the film thickness but gradually decreases in intensity as the plasma ions and radicals penetrate deeper into the porous matrix. Second, pore collapse and material densification occur as also supported by the 9nm total thickness decrease. Lastly, the overall low- $k$  material damage was significant as demonstrated by both the 38nm bulk (i.e layer 1) thickness decrease and the  $2.2\text{g}/\text{cm}^3$



**Figure 4.** XRR scan and data fitting of a) pristine low- $k$  material,  $k = 2.2$ ; b) same material after O<sub>2</sub> plasma treatment at 600W for 5sec. — experimental data, — fitted data.



**Figure 5.** XPS depth profiles of the same  $k = 2.4$  porous dielectric material using identical sputtering rates; a) pristine b) after  $O_2$  plasma treatment. ● Carbon, ○ Oxygen, ▲ Silicon.

density value detected at the top-surface, which corresponds to carbon-free, densified silica. As a general guideline, one should always keep in mind that multi-layer fitting can lead to different results and should be considered with care.

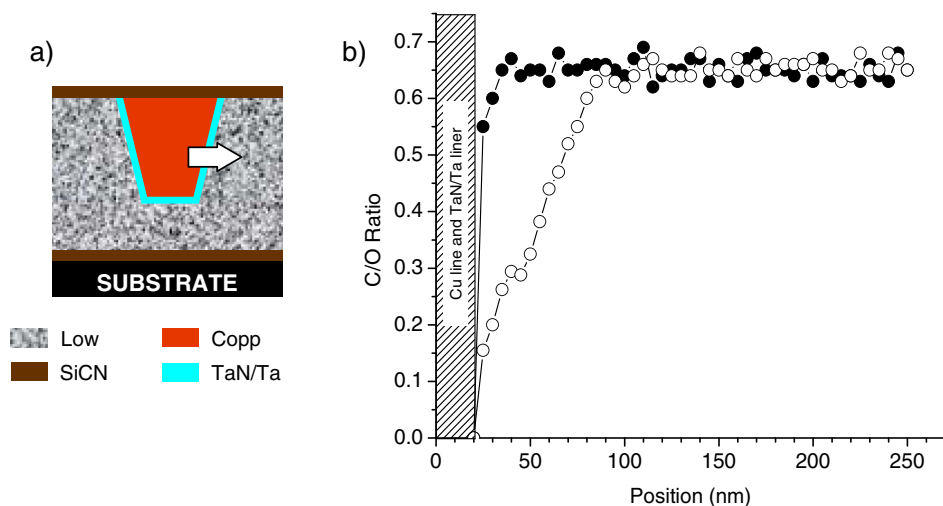
**X-ray photon spectroscopy.**—X-ray photoelectron spectroscopy (XPS) is a surface-sensitive spectroscopic technique that allows for the quantitative measurement of a material's elemental composition. An X-ray beam is sent on the material's surface, and the kinetic energy and number of electron that are liberated from the top 10nm of the material are collected and analyzed. If coupled with ion etching/sputtering, XPS can be carried out in a “depth-profiling mode”. The sputtering will progressively expose deeper content of the sample while simultaneously analyzing the elemental composition. In the case of low- $k$ , organosilicate-based dielectric materials, chemical plasma damage can thus be evidenced by monitoring the atomic concentrations of elements such as C, O and Si, throughout the film thickness, as illustrated in Figure 5.

With regard to the pristine dielectric material, the different atomic concentrations appear constant throughout the film thickness, indicative of a homogeneous chemical composition. After approximately 38min sputtering, the Si substrate interface is reached as both carbon and oxygen concentrations drop precipitously and only Si is detected. In comparison, the plasma treated sample exhibits a high initial oxygen concentration coupled to a very low carbon concentration, indicating top surface damage in the form of carbon-depletion reactions. Deeper probing of the film atomic composition reveals a gradual increase in carbon content and a concomitant decrease in oxygen concentration. After approximately 20min sputtering (corresponding to roughly 30% of the total film thickness) the various atomic concentrations are back at a level commensurate with the pristine dielectric material.

**Ellipsometric porosimetry.**—Ellipsometric porosimetry (EP) is a technique that combines spectroscopic ellipsometry with an adsorption tool, to get information on thin films porosity. Practically, spectroscopic ellipsometry measurements (based on the change in polarization of a light wave after reflection on the thin film surface) are carried out in a chamber where the partial pressure of the adsorbate (typically toluene) progressively increases or decreases. By monitoring the change in optical properties and thickness of the film during adsorption and desorption of toluene (or any other adsorbate), information about the film's pore diameter and pore size distribution (PSD) can be obtained. In the case of plasma damaged samples, modifications, such as top-surface densification, can be readily evidenced by shrinkage in pore size and/or decrease in porous volume.

**Time-of-flight secondary ion mass spectrometry (TOF-SIMS).**—Time-of-flight secondary ion mass spectrometry (TOF-SIMS) is a surface sensitive analytical method that uses a focused, pulsed particle beam (primary ion beam) to dislodge molecules or molecular fragments from the topmost sample surface in the form of secondary ions. Primary ion beams are typically based on Ga or Cs, although other materials such as Xe, Ar,  $SF_6$ ,  $O_2$  and even fullerene can be employed. The ejected secondary ions are then accelerated into a mass spectrometer, where the time to reach the detector (time-of-flight) is measured. TOF-SIMS may be used in a static mode, useful for monolayer surface analysis through secondary ions, molecules or clusters, or in a dynamic mode, useful for depth profiling of the elemental sample composition. Both modes have been successfully employed to study plasma damage in low- $k$  dielectric materials. In the case of ashing chemistries, static TOF-SIMS was used to study the nature of the top surface, while dynamic TOF-SIMS provided additional information concerning the lack or presence of additional damage in the bulk of the dielectric material.<sup>54,55</sup> Similarly, the mechanism of fluorocarbon-based etch plasmas could be established using static SIMS,<sup>56,57</sup> while confirming bulk dielectric damage in the form of carbon depletion by dynamic SIMS. Minimum plasma damage and pore sealing by oxygen-free fluorocarbon plasmas could also be corroborated using TOF-SIMS among other characterization techniques.<sup>58</sup>

**Electrical measurements.**—The dielectric constant ( $k$ ), the breakdown voltage and the leakage current of blanket dielectric films are routinely measured using metal-insulator-semiconductor (MIS) structures. These structures are prepared by evaporation of aluminum through a contact mask to form Al dots of different sizes on the film. The measurements are typically conducted at  $150^\circ C$  to eliminate possible contributions of the physisorbed water. To calculate ( $k$ ), the capacitance, the film thickness and the area of each dot need to be precisely known. The measurement of the capacitance is generally conducted at a frequency of 10 kHz using a LCR meter connected to the wafer with wafer probers. The circular dot area is calculated after acutely measuring the diameter under a microscope. The film thickness is typically obtained using X-ray reflectivity, spectral reflectivity or ellipsometry. After recording the dielectric constant, breakdown testing is performed through a series of current-voltage (I-V) measurements averaged over 60 dots per wafer. Each I-V is taken to failure and the breakdown field (breakdown voltage divided by film thickness, reported in MV/cm) of each site is determined to create a field failure distribution. Low dielectric constant materials with a high breakdown voltage are necessary to survive the localized high



**Figure 6.** a) Cross-sectional view of TEM-EELS area of analysis (arrow indicates scan direction) and b) C/O elemental ratio as a function of spatial location: ● undamaged low-k, ○ damaged low-k.

fields existing in microprocessors. For instance, blanket films made of  $k = 2.7$  dielectrics used in manufacturing breakdown around 9-10 MV/cm, this value decreases quickly with the introduction of porosity. Leakage and charge transport can also be determined for each I-V curve. The leakage current  $J$  (A/cm<sup>2</sup>) is recorded as a function of field strength until the breakdown field is reached. It is usually reported at a field of 1MV/cm, with a value of less than  $10^{-9}$  A/cm<sup>2</sup> indicating acceptable leakage. As anticipated, this value increases with increasing porosity and silanol content.

It is worth noting that the dielectric constant, the breakdown voltage and the leakage current are key electrical properties of the insulating material but they don't automatically translate into higher device reliability once the film is integrated. The possibility to extrapolate bulk film electrical properties to single and dual damascene structure reliability data is still an active field of research to facilitate the selection of the best low-k dielectric material at an early development stage.

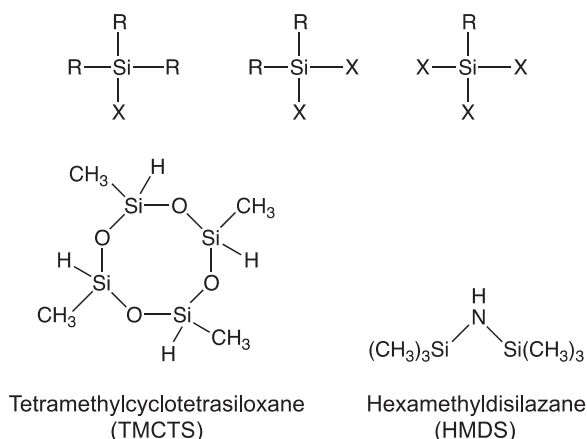
**Techniques applied to patterned structures.—Transmission electron microscopy-electron energy loss spectroscopy.**—Transmission electron microscopy – electron energy loss spectroscopy (TEM-EELS) is a useful technique to evaluate low-k material damage in patterned structures. The TEM enables spatial resolution needed to localize the damage while EELS allows the quantification of such damage by relating the electrons loss of energy due to inelastic scattering to their composition and ratio in the film. The areas of interest are typically around the metallic lines and below the cap (Figure 6a). For example, the results are typically represented by plotting the C/O ratio as a function of the spatial location. A profile, such as the one presented in Figure 6b, where the composition of the low-k material is invariant close to the liner and in between the metallic lines indicates that there is minimum or no damage. Conversely, if a roll-over is observed (Figure 6b), it strongly suggests that the low-k material lost a significant amount of carbon during processing and is seriously damaged.

**Scatterometric porosimetry.**—In 2010, a technique called scatterometric porosimetry was proposed to characterize pattern sidewalls.<sup>59,60</sup> It relies on the combination of ellipsometric scatterometry and ellipsometric porosimetry. The optical index of damaged porous low-k materials under vacuum is very close to the optical index of the undamaged one. In contrast, under moist ambient conditions, water condensation inside the damaged pores of the porous material leads to a dramatic increase of the optical index. It is thus possible to first perform a scatterometric measurement under vacuum to determine the pattern geometry without taking into account the damaged material. In a subsequent experiment conducted under moist ambient conditions, the geometry of the damaged layer can be identified. This technique was validated on complex patterns of porous low-k dielectrics integrated at the 45 nm technology node.<sup>61</sup>

**Capacitance and time dependent dielectric breakdown.**—From an integration point of view, electrical measurements are among the most relevant to assess the damage of porous low-k dielectrics. Practically, only semiconductor companies and large-scale research institutes have the ability to build such test structures because their fabrication requires the use of complex tools in a cleanroom environment. Initial test structures for low-k damage characterization are based on a single metal level and are built at relaxed ground rules. Typically, comb/serpentine (also called meander fork) or comb/comb (fork/fork) patterns are designed to measure the interline capacitance, the time dependent dielectric breakdown (TDDB), the breakdown field, and the leakage current.<sup>62</sup> The electrical data obtained from such structures represent the combined damage of all the process steps. To study the intrinsic reliability of metallic barriers and insulators, Zhao et al. proposed in 2009 a planar capacitor test structure, called “Pcap”.<sup>63</sup> In this approach, the insulator is deposited in a large cavity etched in SiO<sub>2</sub> on silicon. The metallic barrier and the copper are then deposited, forming a planar MIS capacitor. With such structures, the insulator is not exposed to damaging steps and only the impact of the metallic barrier deposition step on the TDDB can now be determined. However, these test structures, *vide supra*, are not sufficient to fully qualify a dielectric material and process for advanced development at a given technology node. Instead, a full 3-level metal structure built at the targeted device dimensions is necessary to acquire electrical reliability (TDDB) and performance ( $k_{\text{effective}}$ ) data.

### Damage repair and /or prevention

**Repair.**— The restoration of dielectric properties in plasma damaged, porous insulators by silylation treatments has been extensively studied and is well documented in the literature.<sup>64-69</sup> In general, the repair process may involve wet or vapor phase capping by alkyl silanes, such as hexamethyldisilazane (HMDS), of the majority of highly polar SiOH groups, generated during plasma damage. Of these repair processes, vapor phase reactions are preferred due to good compatibility with existing equipment. The aim of the silylation treatment is to replenish the carbon content of the damaged dielectric and to restore the hydrophobic character of the initial dielectric material. Typical silylating agents are shown in Figure 7, which differ primarily in the number of reactive endgroups, ranging from monofunctional to trifunctional reagents and the nature of the reactive functionality. Eliminating the most reactive chlorosilanes due to non-suitability for semiconductor applications, primarily alkoxy and alkylamino-endgroup containing candidates remain. Of the two candidates the alkyamino-derivates are the most reactive and readily amenable for vapor phase applications. In addition, there is a general consensus that difunctional silylating agents are most effective.<sup>70,71</sup> However, in the absence of



**Figure 7.** Typical silylating reagents with varying functionality and end-groups, where R = -H, -CH<sub>3</sub>, -alkyl and X = -Cl, -OR, -N(R')<sub>2</sub> where R' = alkyl.

neighboring silanol groups, such reagents may only react at one end with the damaged dielectric surface. In this case, the partially reacted difunctional silane can now reintroduce silanol groups when hydrolyzed by ambient exposure and/or polymerize to form siloxane chains. The use of a monofunctional/difunctional silylating mixture appears to be a solution to this problem.<sup>72</sup>

In actual practice, the use of such silylation reactions rarely restores the damaged dielectric material back to its original state.<sup>21,73</sup> It is worth noting, that cyclic siloxanes, such as tetramethylcyclotetrasiloxane (TMCTS), have also been successfully employed.<sup>74-77</sup> Such reagents require significantly higher silylation temperatures and are not as efficient in restoring the dielectric constant as compared to more reactive alkylsilanes. However, this repair scheme provides the added benefit of significantly enhancing mechanical properties as reflected by the doubling of Young's modulus and a corresponding increase in adhesion energy from less than 1 to approximately 13 J/m<sup>2</sup> for Ar-plasma damaged porous SiO<sub>2</sub> films before and after TMCTS treatment at 400°C, respectively.<sup>78</sup>

Although these repair processes were developed for dielectric materials with  $k \leq 2.4$ , the reluctance of the semiconductor industry to follow the very aggressive dielectric roadmap obviated the use of silylation approaches. At that time, the more conservative dielectric targets of 2.55 to 2.7 allowed DHF removal of the damaged area without significantly affecting the critical dimensions of the ground-rules. With shrinking device dimensions and more aggressive dielectric targets, this approach was no longer viable. Hence, dielectric repair had to be revisited. In this context, two alternative repair processes have been recently reported.<sup>79,80</sup> Both processes utilize a combination of thermal/UV treatments in the presence of precursor reagents capable of capping pendant SiOH groups. The reactive precursors are typically silylating agents or other non-silicon based compounds that can donate carbon fragments, preferably in the form of methyl groups.

A group at Novellus Systems disclosed an approach that appears to be primarily focused on silane based precursor reagents in combination with UV-radiation.<sup>80</sup> Here, the radiation wavelength profile is selected to achieve  $k$  recovery with little or no dielectric material shrinkage and where the majority of the UV radiation has  $\lambda \sim 300$  to 450nm and less than 10% of the UV radiation with  $\lambda < 300$ nm. The choice of the longer wavelength UV radiation profile is apparently based on reports of the damaging effect of short wavelength UV radiation on porous dielectric materials in the form of C-stripping reactions, crosslinking and film densification.<sup>81-83</sup>

In contrast, a group at Applied Materials reports the use of reactive carbon precursors in the presence of heat and UV radiation to treat the defective film.<sup>79,84</sup> Suitable carbon containing reagents include acetylene, ethylene, 1,3-butadiene and isoprene. Here, the UV radiation wavelength profile is chosen to fall primarily below 300nm

to promote carbon incorporation. More precisely, the most efficient UV wavelength is dictated by the nature of the carbon containing precursor, e.g.  $\lambda = 200$ -220nm for butadiene and  $\lambda = 120$ -180nm for acetylene. From this, it is apparent that highly energetic UV radiation is required to convert the unsaturated carbon precursors into reactive species, which are capable of capping pendant SiOH groups. In addition, silane based reagents similar to the ones described by the previous group including vinyltrialkylsilanes are also proposed. In a recent publication by the Applied Materials group, their Onyx<sup>TM</sup> UV-assisted silylation process<sup>85</sup> of undisclosed chemical nature is reported to achieve dielectric constant repair to within 5% of the original value for a  $k = 2.2$  material which had been plasma damaged to  $k = 2.5$ . Corresponding improvements in leakage current were also reported, although the values for repaired samples fall halfway in between those for the pristine and damaged samples. Water contact angle measurements indicated a full recovery from 20 degrees for the damaged sample back to 100 degrees. In addition, TEM-EELS characterization of TaN incursion of the previously damaged and then repaired porous matrix revealed significant pore sealing by this approach.

Clearly, the two approaches largely differ in the choice of the UV wavelength profile. While the less energetic UV exposure ( $\lambda_{UV} > 300$ nm) requires longer exposure/reaction times at higher process temperatures, typically 5 minutes and 400°C, respectively, the more energetic UV exposure ( $\lambda_{UV} < 300$ nm) requires shorter exposure/reaction times at significantly lower process temperatures, typically 30 seconds and 200°C, respectively. It should be noted that long UV exposures with significant wavelength components below 300nm can lead to serious fragmentation and carbon loss of the low- $k$  dielectric material; hence, efficient dielectric repair depends on the optimum balance of reactive precursor, UV wavelength, reaction/exposure time and temperature.

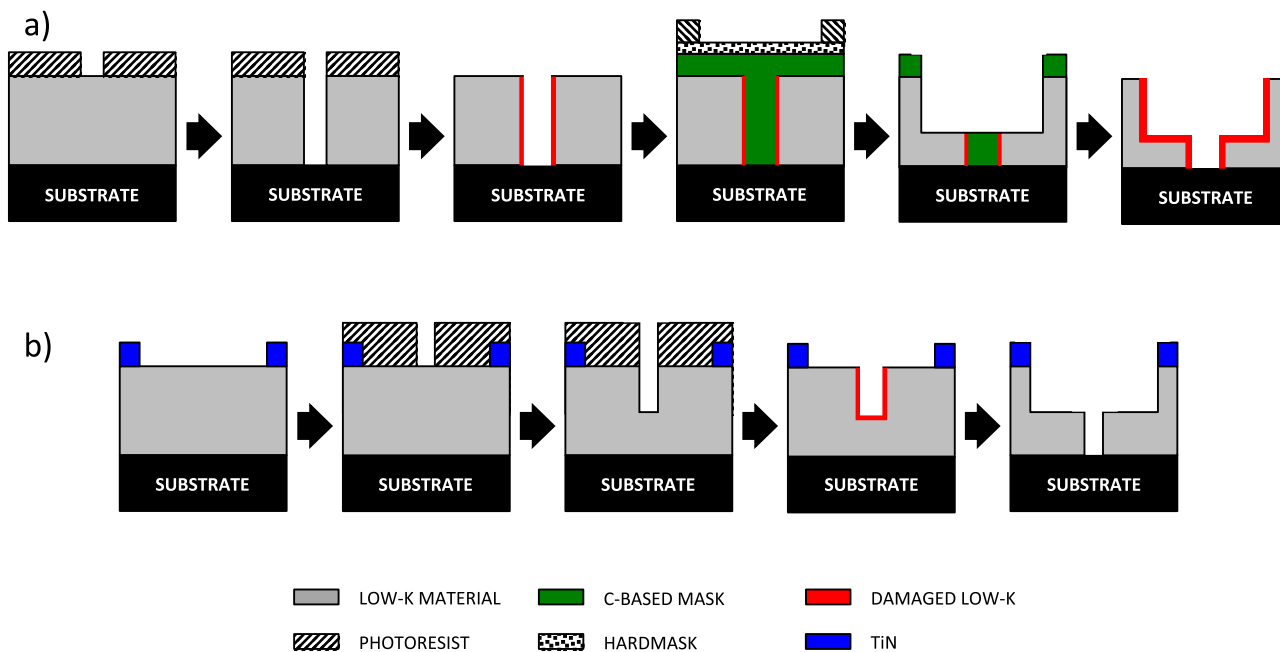
Based on the limited amount of available information, it is not obvious how the more recent UV/ silylation repair processes offer significant improvements over the earlier vapor phase silylation approaches without a direct side-by-side comparison on current technology based candidates.

#### *Prevention.—Metallic hard mask & impact of etch chemistry.—*

There are several integration schemes for porous low- $k$  / copper interconnect fabrication depending on the sequence of trench and via formation, as illustrated in Figure 8. Each integration scheme is associated with a typical mask material. For the "via-first" integration scheme, the via is patterned first using a photoresist etch mask and the trench is etched afterward using a carbon-based mask in a tri-layer stack. Following the etch step, the carbon-based mask must then be removed using plasma-based treatments (typically oxygen plasma) that damage the porous low- $k$  dielectric. For this reason, the industry moved toward the "trench-first" metal hard mask scheme that is the dominant strategy nowadays. Here, the footprint of the trench is defined in a metallic mask (typically TiN). The via is then defined and (partially) etched using a photoresist mask. The resist is removed by plasma and the bottom of the via and the trench are etched at once using the metallic mask. The metallic mask is finally removed by CMP during the metallization, which avoids using damaging plasma processes.

However, changing the mask material has consequences on the etching processes. Indeed, low- $k$  etching processes with a TiN hard mask need to be performed at higher temperature in fluorine-rich plasmas,<sup>86</sup> which tends to increase the porous low- $k$  modification compared to processes developed for low- $k$  etching with carbon-based masks.<sup>39</sup> In addition, some residues grow on the metal hard mask after the patterning when the fluorinated TiN is exposed to the moist ambient conditions.<sup>87</sup> To prevent this growth, post etch treatments can be implemented, but they may potentially also participate in porous low- $k$  damage.<sup>88</sup>

In order to reduce the plasma-induced damage during the patterning steps, oxygen-free plasmas with additional polymerizing gases to limit plasma radical diffusion at the sidewalls are required. However, standard plasma processes have reached their limit and cannot



**Figure 8.** Simplified process flow illustrating (a) “via-first” and (b) “trench-first” metal hard mask integration flow for interconnect fabrication.

pattern damage-free porous low-k structures. Breakthrough patterning technologies are now required to facilitate the integration of porous materials. In this regard, Posseme et al. recently reported an innovative etch process, which is conceptually similar to the previously described polymerizing-type fluorocarbon etch.<sup>89,90</sup> Here, a Si-based etch gas in combination with argon, nitrogen and/or oxygen is claimed to produce sidewall passivation layers comprised of silicon nitride ( $\text{SiN}_x\text{F}_y$  or  $\text{SiN}_x\text{Cl}_y$ ), silicon oxide ( $\text{SiO}_x$ ) or silicon oxynitride ( $\text{SiON}_x\text{F}_y$  or  $\text{SiON}_x\text{Cl}_y$ ), depending on the exact composition of the starting gas mixture. Typical Si-containing etch gases, such as  $\text{SiF}_4$ ,  $\text{SiCl}_4$ ,  $\text{Si}_x\text{H}_y$  (where  $x/y \geq 0.3$ , preferably  $\geq 0.5$ ) were disclosed. Initial data suggests that these type of passivation layers are more effective in blocking reactive species diffusion into the pores, preventing plasma-induced damage.

**Impact of etch temperature (cryo-etch).**—One strategy recently demonstrated to significantly reduce plasma-induced damage to ULK material during integration, was the implementation of plasma etch processes at cryogenic temperatures.<sup>32,91</sup> It is well known that chemical processes in plasma etching processes follow an Arrhenius law where the reaction rate is proportional to  $A \exp[-E_A/RT]$ . Therefore, decreasing the reaction temperature to cryogenic levels also lowers the reaction rate constant of the different reactive species in the plasma. As a result, it is anticipated that cryogenic conditions should still enable etching of the low-k material while at the same time reducing the plasma damage. This was successfully achieved by Iacopi et al. in 2011, who demonstrated that the sticking coefficient (physical adsorption rate), recombination factor and Thiele modulus all increased at low temperatures.<sup>32</sup> As a result, early irreversible adsorption of the plasma radicals to the low-k material surface (surface confinement) occurred, thus reducing the penetration depth into the porous matrix and limiting the damage. Radical penetration was studied by exposing nanoporous hybrid organic-inorganic thin films with 40% fully interconnected porosity and an average pore size of 4 nm to a highly damaging  $\text{O}_2$ -based plasma at various temperatures: (296K, 240K, and 200K). The exposed/damaged films were then examined by STEM/EELS and XRR to monitor the extent of damage and thickness of the preserved pristine material. It was concluded that for equivalent oxidizing exposure times, the sample processed at 200K had radical penetration into the dielectric material that was three times smaller than that of the sample processed at 296K. Based on these findings,

other groups have investigated the etching and plasma damage of low-k dielectric materials at cryogenic temperatures using more elaborate plasma chemistries. When a pure  $\text{SF}_6$  plasma was used, the authors proposed that the protection observed at low temperature is due to etch reaction by-products, such as alkyl alcohols and aldehydes “sealing” the open pores of the porous matrix.<sup>91,92</sup> The same group has also shown that by adding a given ratio of  $\text{SiF}_4/\text{O}_2$  to the  $\text{SF}_6$  plasma, one can deposit a passivation layer of  $\text{SiO}_x\text{F}_y$  polymer on the sidewalls, which prevents lateral etching.<sup>91</sup> Due to ion bombardment, this passivation layer is quickly consumed at the etch front (i.e. trench bottom) as long as the  $\text{SiF}_4$  content in the plasma remains below a certain value. Indeed for a 3:1  $\text{SiF}_4:\text{O}_2$  ratio an etch-stop phenomenon was observed. It is worth mentioning that while the passivation layer is largely desorbed as the wafer is heated back to ambient temperature, the etch by-products require an additional thermal annealing to 350°C to be decomposed. Even though no additional damage was observed, the original k value of the material before etch is not retained. The increase in k can be attributed to densification that occurred during etch and/or incomplete removal of passivation layer/etch by-product related species. Due to the required new tooling and difficulties in optimizing etch chemistries to yield acceptable etch rates while eliminating etch damage at cryogenic temperatures, this plasma etch method is purely a research venture at this time and no known semiconductor manufacturer is currently integrating chips using cryogenic etch.

**Pore sealing.**—Since the introduction of copper in 1997, the sidewalls and bottom surface of metallic lines have been fully covered with a Ta/TaN diffusion barrier deposited by PVD. However, with the introduction of porous low-k materials, two new concerns were raised: a) sidewall uniformity of the diffusion barrier at smaller thicknesses and b) pore penetration of precursor species (specific to deposition by atomic layer deposition (ALD)). In this context, the pore sealing concept emerged as a potential solution to the aforementioned concerns. In general, the pore-sealing step takes place on a patterned dielectric material as part of the ashing step, prior to diffusion barrier deposition. Two main techniques to seal the pores have been reported in the literature: plasma treatment and liner deposition. In the first case, the objective is to create a dense  $\text{SiO}_2$ -like thin layer at the dielectric material surface. Regarding the evaluated plasma chemistry, oxygen based chemistries were excluded as they strongly promote silanol formation within the ULK,<sup>93</sup> leading to moisture uptake and increase in k.



Consequently, reducing plasma chemistries such as  $N_2/H_2$ ,  $NH_3$ <sup>93,94</sup> or more exotic combinations such as  $N_2/Ar$ ,  $He/N_2$ ,  $CH_4$ <sup>95,96</sup> were used. In this case, efficient pore-sealing was demonstrated when the plasma processing conditions (mainly plasma power/bias and exposure time) were optimized. For dielectric materials with moderate porosities ( $2.2 < k < 2.5$ ), the plasma damage cannot be confined to the dielectric material surface (typically within the first nm of film thickness). Hence, another less damaging plasma sealing approach was proposed using a gas cluster ion beam (GCIB) technique. Here, low individual atomic kinetic energy ensures that the ion clusters interact with the immediate material surface only.<sup>97</sup> Employing this technique, pore sealing of materials with a dielectric constant as low as 2.2 could be successfully achieved. Regardless of the sealing strategy, if the dielectric material porosity becomes highly interconnected, the plasma ions and radicals can then deeply penetrate into the material and cause severe damage, offsetting the benefits of pore sealing. In that case, the liner deposition strategy that consists of depositing a thin layer of a different material on the porous material surface seems to be the most promising to seal the pores.

Dry processes are primarily considered for the liner deposition as ULK materials must stay away from humidity. Consequently physical or chemical vapor deposition techniques are traditionally employed. In order to maintain the dielectric material insulating properties, the liner's thickness and dielectric constant need to be as low as possible. Silicon carbides or nitrides, with  $k$  ranging from 4 to 5, are the commonly auditioned liners.<sup>98–100</sup> Silica-type liners with a lower  $k$ , such as  $SiO_2$  ( $k \sim 4$ )<sup>101,102</sup> or plasma polymerized organic silica (referred to as DVS-BCB,  $k = 2.7$ )<sup>103</sup> have also been studied, but they were eventually discarded as their oxidizing deposition environment favors moisture uptake and their lower density leads to less efficient barrier properties. While it is relatively easy to deposit thin liners on low porosity dielectric materials, especially by ALD, it becomes a lot more challenging when the pore size is on the same order or bigger than the precursor molecules. In that case, a couple of major drawbacks arise: i) thicker liners are needed to form pin-holes free barriers,<sup>102,104,105</sup> and ii) the precursor molecules deposit inside the pores before a continuous layer is actually formed on the material surface.<sup>106</sup> Even though the latter could help ensure a good adhesion between the two materials, it should be avoided (or limited to a few nanometers at the interface) to keep the increase in  $k_{\text{effective}}$  at a minimum. One way to mitigate this penetration phenomena is to pre-treat the dielectric material surface prior to liner deposition. For instance, a light plasma treatment (as described above) can narrow the pore diameter of the top surface without causing major damage, physically limiting the liner precursor penetration or diffusion. The results can also be obtained by chemical means: UV-assisted restoration<sup>107</sup> or silylation type treatments<sup>108</sup> can substitute silanols (formed during previous integration steps) with carbon groups, whose hydrophobic behavior inhibits interactions between pore walls and precursors.

Recently, Armini et al. proposed a more exotic route using self-assembled monolayers (SAMs) to seal the pores of a highly porous ULK with  $k = 2.0$ . The first step consists in creating hydroxyl groups on the ULK surface and is done by either an  $Ar/H_2$  plasma treatment<sup>109</sup> or an immersion in DHF, tetramethylammonium hydroxide (TMAH) or a sulfuric peroxide mixture.<sup>110</sup> Following surface hydroxylation, SAMs derived from 11-cyanoundecyltrichlorosilane are deposited (using either dry or liquid processes) and grafted on the ULK surface. It is worth mentioning that to get high SAMs surface coverage, i.e. efficient pore-sealing, a large number of OH groups have to be present on the ULK surface before grafting. When the ULK surface hydroxylation was done by solvent immersion, a significant increase in the ULK dielectric constant ( $k > 3$ ) that can be ascribed to SAMs pore penetration was obtained. In the case of  $Ar/H_2$  plasma treated ULK, if the plasma conditions are optimized, the increase in dielectric constant can be mitigated ( $k = 2.7$ ).

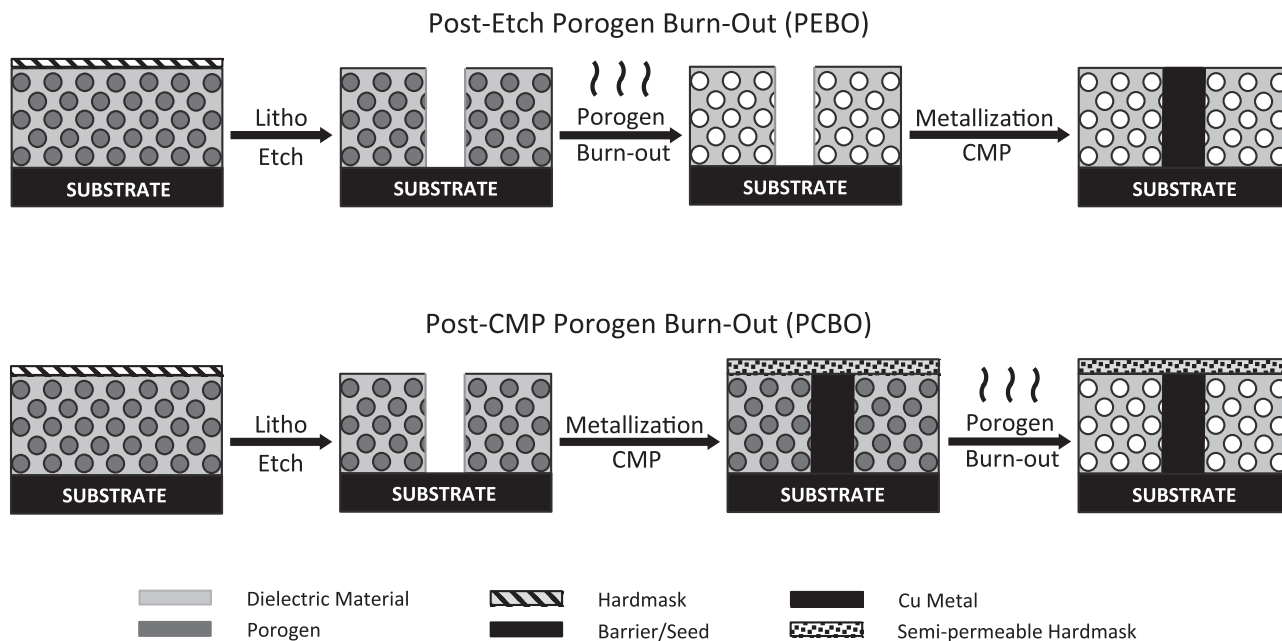
As of today, pore sealing has not been implemented. In fact, the current  $k = 2.4$  low- $k$  dielectric materials benefit from the recent

advances in material chemistry and display small pores (diameter  $< 2\text{nm}$ ) only. Therefore thin Ta/TaN diffusion barriers can still be directly deposited on these insulators without compromising electrical reliability.

*Porosity last.*—An innovative way to address plasma related damage and decreased mechanical properties in porous materials was realized early on by conducting the damascene-based processing in the pre-porous state.<sup>111–114</sup> Here, the ability to conduct detrimental process steps on a robust, non-porous material would greatly minimize degradation of electrical properties by ash and etch steps as well as to enhance the mechanical integrity during CMP. Subsequent generation of the porosity to lower the dielectric constant would occur following such process steps. However, this required a thermally labile, organic pore generator (porogen) that exhibited good thermal stability at temperatures conducive to high degrees of dielectric material cure. This in turn would minimize material collapse and shrinkage during later thermal decomposition of the pore generator (porosity generating step) at higher temperatures. Ideally, the pore generators would be thermally stable to  $350^\circ\text{C}$  and decompose cleanly and completely by  $400^\circ\text{C}$ . Unfortunately, such porogens are not very common. The best-known materials are particle-based porogens with thermally stabilities in the  $250\text{--}300^\circ\text{C}$  range and which require decomposition temperatures  $> 400^\circ\text{C}$ .<sup>115,116</sup> The integration strategy based on this concept is illustrated in Figure 9 and can be exercised at two different stages of a typical damascene integration scheme, i.e. after pattern etch or after metallization and CMP. The post-etch burn-out (PEBO) approach primarily prevents plasma damage of the dielectric material and facilitates smooth sidewalls even after porogen burn-out. While the former is a direct result of the non-porous nature and low surface area of the insulator, the latter is believed to occur due to plasma interaction with the porogen material. Alternatively, applying this strategy after CMP, post-CMP burn-out (PCBO), plasma damage of the dielectric material is again minimized while additionally providing enhanced mechanical integrity during CMP. However, the PCBO approach requires a semi-permeable hard mask to facilitate escape of the porogen volatiles during burn-out.

Although conceptually elegant, the pre-porous integration of low- $k$  dielectric materials suffered from considerable material shrinkage<sup>117</sup> (about 5%) leading to change in critical dimensions, as well as promoting high internal film stress. This stress would be compounded during buildup of the stack, ultimately leading to mechanical failure of the device. In addition, difficulties were encountered with plasma-based lithography rework.<sup>118</sup> Finally, the need for burn-out temperatures in excess of  $400^\circ\text{C}$  to assure complete porogen removal is currently considered to be too high for Cu metallization. In spite of the novelty of the approach at the time, this particular strategy was abandoned. Nevertheless, these drawbacks were addressed by the post porosity plasma protection (P4) strategy years later, *vide infra*.

*Post-porosity plasma protection.*—The post-porosity plasma protection (P4) process was designed to protect fully cured, i.e. dimensionally stable, porous low- $k$  dielectric materials during integration. This concept was inspired by the protection/deprotection approach used extensively in organic chemistry, where a functional group is shielded during a chemical transformation and then eventually restored. Here, the pores of a porous dielectric material are filled with a sacrificial agent (typically a polymer), leading to the formation of an apparent dense material.<sup>30</sup> Since the porosity is masked and the total carbon content has been significantly increased, the harmful integration steps (etching, ashing and CMP) may then be carried out with limited damage. Following either etch or CMP, the filler is removed by thermal means, restoring the initial dielectric constant. It is noteworthy, that due to complete cure of the initial matrix material, no shrinkage is obtained during the filler burn-out, unlike the porosity last approach. The P4 process is implemented in 3 major steps as illustrated on Figure 10: 1) a polymer solution is spin-deposited on the porous, low- $k$  material surface, 2) the wafer with the insulator/filler-polymer stack is heated above the polymer's  $T_g$  (typically  $125\text{--}175^\circ\text{C}$  for 2 to 5 minutes) to fill the porosity by capillary action in a so-called post-apply



**Figure 9.** Proposed, simplified single damascene integration pathways of low-k dielectric materials in the pre-porous state.

bake (PAB) step and 3) excess fill-polymer remaining on the dielectric material surface (referred to as overburden) is finally removed by a solvent rinse.

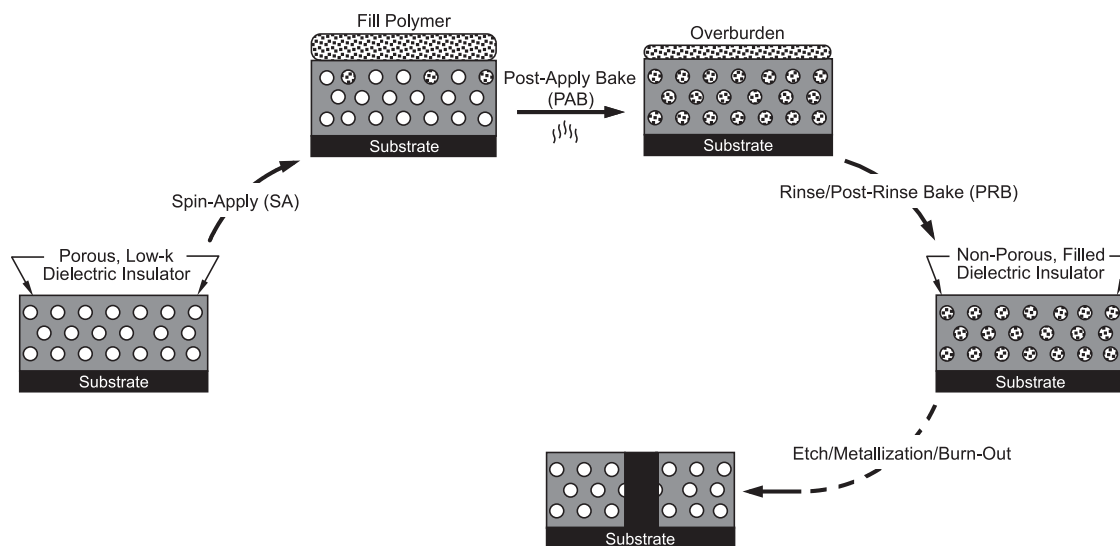
At this point, the dielectric material is not only protected, but it also displays a clean surface, a mandatory requirement to pursue further integration. Following completion of the integration processes, the filler is removed by using a short thermal treatment at 400°C.

For this process to be successfully applied, the filler must meet several stringent requirements. First, its molecular weight needs to be compatible with the pore size of the dielectric material to ensure that pore filling is possible. Second, the polymer should exhibit a low viscosity under pore filling conditions to minimize filling time. Third, the polymer needs to be stable up to 350°C (in an oxygen-free environment) to survive integration and cleanly decompose by 400°C. Such a narrow process window between thermal stability and decomposition is very challenging to achieve with relatively low molecular weight filler materials.

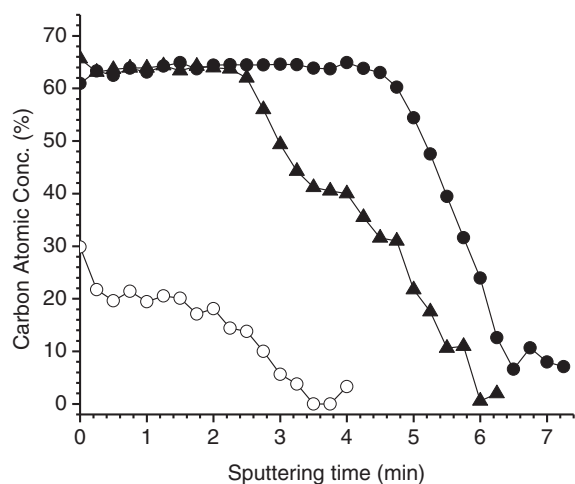
Practically, several measurements should be conducted after step 3) to assess the fill level and its uniformity throughout the film thickness and across the wafer surface. In this regard, XRR is commonly used to detect density gradients throughout the film thickness due to non-uniform pore filling. Moreover, provided that the dielectric material porosity,  $v$ , was preliminarily measured, XRR also enables to calculate the fill level,  $F$ , through the determination of the filler density,  $\rho_{filler}$ , as well as those of the pristine ( $\rho_{diel}$ ) and filled dielectric material ( $\rho_{f-diel}$ ) materials, using equation 1.

$$\rho_{f-diel} = \rho_{diel} + (v \times F)\rho_{filler} \quad [1]$$

XPS depth profiling can also be performed to support the XRR fitting models. Thus, fill effectiveness can be established by comparison of the carbon content of the pristine with P4 treated dielectric material, while fill homogeneity throughout the film thickness can be confirmed by monitoring the carbon content as a function of sputtering depth. This is illustrated in Figure 11, which displays the depth dependent



**Figure 10.** Simplified schematic of process steps integral to the P4 process.



**Figure 11.** Carbon atomic concentration collected by XPS depth-profiling on a dielectric material at  $k = 1.8$  at a fixed filler molecular weight and as a function of fill temperature.  $\circ$ ) unfilled material,  $\blacktriangle$ ) low temperature fill,  $\bullet$ ) high temperature fill.

C atomic concentration measured by XPS (using the same sputtering rate) on a  $k = 1.8$  dielectric material as a function of fill temperature. Since the backbone chemical structure is the same for all samples, the differences observed can be directly ascribed to differences in filling. The carbon concentration of the unfilled material is  $\sim 20\%$  and quickly decreases to near  $0\%$  upon approaching the Si substrate interface as the porous material has a very low resistance to sputtering. In comparison, the filled materials have a much higher initial carbon concentration of  $\sim 64\%$  due to the presence of the high carbon content filler in the pores. The primary difference between filled samples is the C content as a function of film depth. While the sample filled at low temperature exhibits a gradual decrease in C atomic concentration as a function of sputtering depth, indicating non-uniform filling, the C atomic concentration of the sample filled at high temperature remains at the initial level of approximately  $64\%$  and then drops sharply upon approaching the Si interface, reflecting uniform filling throughout the film thickness.

Presumably, the higher fill temperature facilitates faster and deeper filler penetration into the porous structure as a result of increased diffusion kinetics and lower filler viscosity. In case of the completely filled sample the sputtering time to reach the bottom of the film was a lot longer as compared to that of the unfilled material due to the presence of the filler, i.e. decreased sputtering rate.

Once high and uniform fill of the porous dielectric material is established, the filler protection efficacy can be assessed, as a first step, on blanket films and patterned structures thereafter. For blanket films this is readily achieved using the PID test, *vide supra*. When applied to a series of spin-on polyoxycarbosilane (POCS) based low- $k$  dielectric materials with an identical backbone but different porosities ( $k = 1.8 - 2.4$ ), the measured PID (thickness loss) as a function of porosity, using a polymeric methacrylate filler, is shown in Table II.

The PID of the unfilled (unprotected) films increases exponentially with increasing porosity, reflecting the higher susceptibility of the more porous samples to plasma damage. The increase in plasma damage is a direct consequence of increasing porosity, pore size and pore connectivity, which combined, lead to much higher accessible surface area for plasma ions and radicals. In contrast, the corresponding filled (protected) films display a virtually constant and minimal PID of about 20-30nm, irrespective of porosity. This result can be explained by the overall higher carbon content of protected dielectric material as compared to unprotected and to the formation of an apparent dense material physically limiting ion and radical penetration. Altogether, the level of protection between filled (dense) and unfilled (porous) samples as a function of porosity illustrates the inherent

**Table II.** PID of filled (protected) and pristine (unprotected) low- $k$  dielectric materials as a function of porosity.

Porosity (%)	PID (nm)		Protection (%)
	Unfilled	Filled	
23	31	20	35
26	39	21	45
29	46	19	59
37	77	27	65
49	172	24	86

utility of the P4 strategy to mitigate plasma damage of dielectric materials at higher porosities, i.e. decreasing dielectric constants.<sup>31</sup>

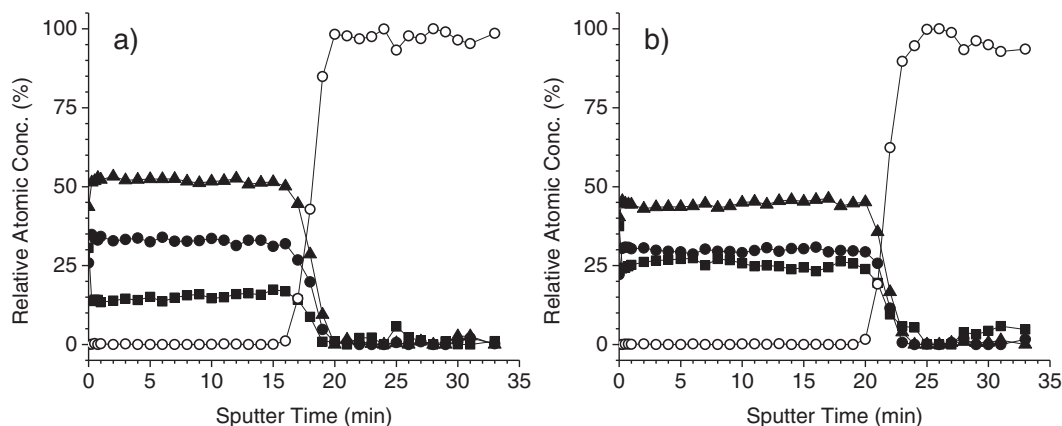
To evaluate the P4 efficacy under more realistic conditions, 200mm wafers were coated with dielectric films at  $k = 1.8, 2.0$  and  $2.2$ . Both unprotected and protected samples were then patterned (250nm lines and spaces) to form trenches of identical dimensions, allowing for a side-by-side comparison. The scanning electron microscopy (SEM) cross-sections of the different patterned specimens, previously reported by Frot et al.,<sup>31</sup> point to the effectiveness of the P4 strategy. Unprotected patterned samples exhibit numerous defects in the trench profile, such as undercuts below the hard mask, pitting and micro-trenching at the bottom of the line, as well as sidewall bowing. These features become more pronounced as  $k$  decreases, ultimately leading to a total blow-out of the critical dimensions. In comparison, protected patterned samples display very well defined trenches with straight sidewalls and retention of the critical dimensions, independent of the porosity. These results are in excellent agreement with the blanket film PID results and illustrate the efficacy of the P4 strategy. It is worth noting that among all the mentioned strategies, P4 is the only strategy with an increasing beneficial effect as  $k$  decreases, providing a path toward “damage-free” dielectric material integration at more aggressive dielectric targets. While it is not yet implemented in manufacturing, it is currently evaluated at an advanced development stage.

*Additional P4 issues when applied to plasma-enhanced chemical vapor deposited (PECVD) dielectric materials @  $k = 2.4$ .*—While the original P4 strategy was designed to address plasma damage in highly porous, spin-deposited materials with very aggressive dielectric targets ( $k < 2.4$ ), current dielectric targets are actually significantly less aggressive. As a result, it has become necessary to ascertain the applicability of this strategy to PECVD deposited dielectric candidates at current dielectric targets of  $k = 2.4$ . Of course, this requires the re-optimization of the P4 process to take into account differences in surface properties, porosity and pore size/interconnectivity.

Indeed, due to the smaller pore size/interconnectivity, lower molecular weight fillers have to be employed to achieve filling of the accessible pores. First, the decrease in filler molecular weight along with the more hydrophobic PECVD dielectric material surface (as compared to spin-on materials) often lead to fast surface de-wetting after filler spin-apply and/or after the PAB step. While de-wetting after spin-apply prevents filler penetration into the porous matrix during PAB and represents a serious problem, de-wetting after PAB is less serious, although it may preclude complete filling. Second, partial or complete filler “wash out” may occur during overburden removal.

To mitigate surface de-wetting issues, several strategies can be considered. First, surface modifications, such as a light plasma treatment, can be performed prior to pore filling in order to decrease the surface energy. Using this strategy, it is necessary to have a good control of the plasma to avoid pore diameter shrinkage and damage to the dielectric material. Second, surface de-wetting can be avoided by introduction of a suitable additive in the filler solution that would help maintain a good surface wetting during PAB.

Such additives would require thermal stabilities similar to the fill polymer if the additive penetrates the porosity, or they should be rinsed off during overburden removal if the additive does not infiltrate the



**Figure 12.** XPS elemental depth profiles of a) unfilled ULK b) ULK refilled with polyacrylate. ■) carbon, ▲) oxygen, ●) ULK silicon, ○) substrate silicon.

pores. Lastly, the filler chemistry itself can be modified to increase its compatibility with the surface of the low-k dielectric material.

Regarding the filler “wash out”, this remains an area of active research and novel solutions to this problem need to be developed.

**In-situ P4.**—In light of the difficulties encountered when trying to fill porous dielectric materials comprised of small and less-interconnected pores, the need for low molecular weight fillers prompted an alternate P4 approach, referred to as in-situ P4, where the porosity is filled with monomers or low molecular weight oligomers followed by polymerization inside the pores of the dielectric material. Inspiration for this approach was derived from literature reports describing the successful polymerization of monomers in nanoporous scaffolds or hosts for other applications.<sup>119–121</sup> Similarly to the standard P4 process it is crucial to achieve high pore filling levels with the monomer along with a polymerization rate conducive to process windows for single wafer integration of less than 10 minutes, preferably less than 5 minutes. One successful example of this alternate P4 approach is demonstrated by polymerizing a polyacrylate inside the pores of a current PECVD material candidate ( $k = 2.3$ ) with an average pore size of 1.5nm. Using a lauryl acrylate monomer with 1% by weight benzoyl peroxide, we were able to achieve 80% filling of the total available porosity after polymerization. The successful filling was confirmed by an increase in the film density from 1.105 to 1.371  $\text{g}/\text{cm}^3$  as measured by XRR along with a corresponding increase in refractive index from 1.34 to 1.43 as measured by spectral reflectivity. Moreover, depth-profiling XPS confirmed that the refill was homogenous throughout the film thickness as evidenced by the level profile of the relative atomic concentration of carbon, see Figure 12. The protection efficacy of this method was then tested using the PID method. In this case, the damaged thickness for the unprotected PECVD ULK ( $k = 2.3$ ) was 32 nm; for the protected sample the thickness loss after DHF dip was only 14 nm.

**Cryo P4.**—Analogous to the standard P4 strategy, Baklanov et al. disclosed a similar protection scheme with the proviso that both pore fill and plasma etch steps are performed at low temperatures.<sup>122</sup> Corresponding porous dielectric materials with porosities between 10 and 80%, pore sizes from 0.2 to 1000nm and film thicknesses of 600nm or less are called out. In this modified P4 approach, the selection of the refill material is also very crucial. Once the porosity is fully or partially refilled, the material of choice (liquid or gas) must change into a solid at the cryogenic temperatures and pressures of choice. Suitable fluids candidates called out can be inorganic ( $\text{CO}_2$ , Xe,  $\text{NH}_3$ ,  $\text{H}_2\text{O}$  and  $\text{SF}_6$ ), organic hydrocarbons (toluene,  $\text{C}_6 - \text{C}_{12}$  alkanes) and halocarbons such as fluorocarbons with fluorine to carbon ratios of 2. ( $\text{C}_2\text{F}_4$ ,  $\text{C}_4\text{F}_8$ ).

In contrast to the direct introduction of the refill material into the reaction chamber, it can be produced in-situ from the products of the plasma interaction with the dielectric material to form a  $\text{SiO}_x\text{F}_y$  type protective material as described previously in the cryogenic etch

section of this article. Another refill fluid that can be produced in-situ is  $\text{H}_2\text{O}$ , upon interaction between oxygen plasma and an organosilicate resist layer.

After pattern etch, the removal of the refill material (i.e. de-protection) is achieved by raising the surface temperature of the dielectric material and chamber pressure to the vaporizing/sublimation temperature and pressure of the selected refill material preferably between 15 to 80°C but typically between 20 to 25°C. An additional advantage disclosed with this cryogenic protection method is that the resist used in the patterning etch step can be removed while the porous material is still filled therefore limiting the damage associated with the resist strip step.

As with the previous cryogenic etch approach, implementation of this method is limited due to the required development of new tooling and materials with optimum cryogenic properties.

## Conclusions

In summary, the sensitivity of porous low-k materials to plasma damage represents one of the major challenges for current and future BEOL integration. The semiconductor industry is actively looking for different solutions to prevent, minimize or repair this damage, many of which are inspired by research conducted 10 years ago. Novel etch chemistries, either at cryogenic or room temperature will emerge. Repair in the form of silylation combined with a UV/thermal treatment will remain a potential approach if the damage is not too severe and occurs with minimum material densification. Finally, a more complete solution based on the protection of porosity by refilling the pores, known as P4 (and cryo-P4), could provide a cornerstone in the integration of low-k materials if the filler exhibits the desired properties and compatibility with current integration schemes can be successfully demonstrated.

## References

1. V. McGahay, *Materials*, **3**, 536 (2010).
2. W. Volksen, R. D. Miller, and G. Dubois, *Chem. Rev.*, **110**, 56 (2010).
3. G. Dubois and W. Volksen, in *Adv. Interconnects ULSI Technol.*, M. R. Baklanov, P. S. Ho, and E. Zschech Editors, p. 3, Wiley (2012).
4. R. J. O. M. Hoofman, V. H. Nguyen, V. Arnal, M. Broekaert, L. G. Gosset, W. F. A. Besling, M. Fayolle, and F. Iacopi, in *Dielectric Films for Advanced Microelectronics*, M. Baklanov, K. Maex, and M. Green Editors, p. 199, Wiley (2007).
5. W. Volksen, K. Lioni, T. Magbitang, and G. Dubois, *Scripta Mater.*, **74**, 19 (2014).
6. K. Mosig, T. Jacobs, K. Brennan, M. Rasco, J. Wolf, and R. Augur, *Microelectron. Eng.*, **64**, 11 (2002).
7. A. Grill, D. Edelstein, M. Lane, V. Patel, S. Gates, D. Restaino, and S. Molis, *J. Appl. Phys.*, **103**, 054104/1 (2008).
8. E. P. Guyer, M. Patz, and R. H. Dauskardt, *J. Mater. Res.*, **21**, 882 (2006).
9. A. Jain, S. Rogojevic, S. Ponoth, N. Agarwal, I. Matthew, W. N. Gill, P. Persans, M. Tomozawa, J. L. Plawsky, and E. Simonyi, *Thin Solid Films*, **398-399**, 513 (2001).

10. H. Li, Y. Lin, T. Y. Tsui, and J. J. Vlassak, *J. Mater. Res.*, **24**, 107 (2009).
11. M. S. Oliver, G. Dubois, M. Sherwood, D. M. Gage, and R. H. Dauskardt, *Adv. Funct. Mater.*, **20**, 2884 (2010).
12. M. D. Ong, W. Volksen, G. Dubois, V. Lee, P. J. Brock, V. R. Deline, R. D. Miller, and R. H. Dauskardt, *Adv. Mater.*, **20**, 3159 (2008).
13. K. Vanstreels, C. Wu, P. Verdonck, and M. R. Baklanov, *Appl. Phys. Lett.*, **101**, 123109/1 (2012).
14. R. A. Susko, T. H. Daubenspeck, T. A. Wassick, T. D. Sullivan, W. Sauter, and J. Cincotta, *ECS Trans.*, **16**, 51 (2009).
15. F. Iacopi, Y. Travaly, B. Eyckens, C. Waldfried, T. Abell, E. P. Guyer, D. M. Gage, R. H. Dauskardt, T. Sajavaara, K. Houthoofd, P. Grobet, P. Jacobs, and K. Maex, *J. Appl. Phys.*, **99**, 053511/1 (2006).
16. A. Zenasni, B. Remiat, C. Waldfried, C. Le Cornec, V. Jousseau, and G. Passenard, *Thin Solid Films*, **516**, 1097 (2008).
17. W. Volksen, G. Dubois, A. Kellock, T. P. Magbitang, R. D. Miller, D. Miller, S. Cohen, E. E. Simonyi, L. Ramirez, D. Markle, S. Chen, S. Zhou, X. Wang, and Y. Wang, *J. Electrochem. Soc.*, **155**, G224 (2008).
18. G. Dubois, W. Volksen, T. Magbitang, M. H. Sherwood, R. D. Miller, D. M. Gage, and R. H. Dauskardt, *J. Sol-Gel Sci. Technol.*, **48**, 187 (2008).
19. G. Dubois, W. Volksen, T. Magbitang, R. D. Miller, D. M. Gage, and R. H. Dauskardt, *Adv. Mater.*, **19**, 3989 (2007).
20. Y. Matsuda, J. S. Rathore, L. V. Interrante, R. H. Dauskardt, and G. Dubois, *ACS Appl. Mater. Interfaces*, **4**, 2659 (2012).
21. W. Volksen, S. Purushothaman, M. Darnon, M. F. Lofaro, S. A. Cohen, J. P. Doyle, N. Fuller, T. P. Magbitang, P. M. Rice, L. E. Krupp, H. Nakagawa, Y. Nobe, T. Kokubo, and G. J. M. Dubois, *ECS J. Solid State Sci. Technol.*, **1**, N85 (2012).
22. W. Volksen, T. P. Magbitang, R. D. Miller, S. Purushothaman, S. A. Cohen, H. Nakagawa, Y. Nobe, T. Kokubo, and G. J. M. Dubois, *J. Electrochem. Soc.*, **158**, G155 (2011).
23. S. M. Gates, G. Dubois, E. T. Ryan, A. Grill, M. Liu, and D. Gidley, *J. Electrochem. Soc.*, **156**, G156 (2009).
24. S. Hualiang, D. Shamiryan, J.-F. De Marneffe, H. Huai, P. S. Ho, and M. R. Baklanov, in *Adv. Interconnects ULSI Technol.*, M. R. Baklanov, P. S. Ho, and E. Zschech Editors, p. 79, Wiley (2012).
25. R. L. Bruce, S. Engelmann, S. Purushothaman, W. Volksen, T. J. Frot, T. Magbitang, G. Dubois, and M. Darnon, *J. Phys. D Appl. Phys.*, **46**, 265303 (2013).
26. M. Darnon, N. Casiez, T. Chevolleau, G. Dubois, W. Volksen, T. J. Frot, R. Hurand, T. L. David, N. Posseme, N. Rochat, and C. Licitra, *J. Vac. Sci. Technol. B*, **31**, 011207/1 (2013).
27. Q. T. Le, G. Vereecke, H. Struyf, E. Kesters, and M. R. Baklanov, in *Adv. Interconnects ULSI Technol.*, M. R. Baklanov, P. S. Ho, and E. Zschech Editors, p. 129, Wiley (2012).
28. S. Satyanarayana, R. McGowan, B. White, and S. Hosali, *Semicond. Int.*, **28**, 63 (2005).
29. T. Frot, W. Volksen, T. Magbitang, S. Purushothaman, R. L. Bruce, S. Cohen, M. Lofaro, and G. Dubois, *Future Fab Intl.*, **39**, 67 (2011).
30. T. Frot, W. Volksen, S. Purushothaman, R. Bruce, and G. Dubois, *Adv. Mater.*, **23**, 2828 (2011).
31. T. Frot, W. Volksen, S. Purushothaman, R. L. Bruce, T. Magbitang, D. C. Miller, V. R. Deline, and G. Dubois, *Adv. Funct. Mater.*, **22**, 3043 (2012).
32. F. Iacopi, J. H. Choi, K. Terashima, P. M. Rice, and G. Dubois, *Phys. Chem. Chem. Phys.*, **13**, 3634 (2011).
33. T. Standaert, P. J. Matsuo, S. D. Allen, G. S. Oehrlein, and T. J. Dalton, *J. Vac. Sci. Technol. A*, **17**, 741 (1999).
34. N. Posseme, T. Chevolleau, O. Joubert, L. Vallier, and N. Rochat, *J. Vac. Sci. Technol. B*, **22**, 2772 (2004).
35. I. Reid, V. Krastev, and G. Hughes, *Microelectron. Eng.*, **83**, 2458 (2006).
36. Y. Iba, S. Ozaki, M. Sasaki, Y. Kobayashi, T. Kirimura, and Y. Nakata, *Microelectron. Eng.*, **87**, 451 (2010).
37. M. R. Baklanov, J.-F. de Marneffe, D. Shamiryan, A. M. Urbanowicz, H. Shi, T. V. Rakhimova, H. Huang, and P. S. Ho, *J. Appl. Phys.*, **113**, 041101 (2013).
38. D. Shamiryan, M. R. Baklanov, S. Vanhaelemeersch, and K. Maex, *J. Vac. Sci. Technol. B*, **20**, 1923 (2002).
39. M. Darnon, T. Chevolleau, T. David, J. Ducote, N. Posseme, R. Bouyssou, F. Bailly, D. Perret, and O. Joubert, *J. Vac. Sci. Technol. B*, **28**, 149 (2010).
40. J. N. Sun, D. W. Gidley, Y. Hu, W. E. Frieze, and E. T. Ryan, *Appl. Phys. Lett.*, **81**, 1447 (2002).
41. F. Bailly, T. David, T. Chevolleau, M. Darnon, N. Posseme, R. Bouyssou, J. Ducote, O. Joubert, and C. Cardinaud, *J. Appl. Phys.*, **108**, 014906 (2010).
42. H. Sinha, H. Ren, M. T. Nichols, J. L. Lauer, M. Tomoyasu, N. M. Russell, G. Jiang, G. A. Antonelli, N. C. Fuller, S. U. Engelmann, Q. Lin, V. Ryan, Y. Nishi, and J. L. Shohet, *Journal of Applied Physics*, **112**, 111101 (2012).
43. N. Posseme, T. Chevolleau, T. David, M. Darnon, O. Louveau, and O. Joubert, *J. Vac. Sci. Technol. B*, **25**, 1928 (2007).
44. M. A. Worsley, S. F. Bent, S. M. Gates, N. C. M. Fuller, W. Volksen, M. Steen, and T. Dalton, *J. Vac. Sci. Technol. B*, **23**, 395 (2005).
45. N. Posseme, T. Chevolleau, T. David, M. Darnon, J. P. Barnes, O. Louveau, C. Licitra, D. Jalabert, H. Feldis, M. Fayolle, and O. Joubert, *Microelectron. Eng.*, **85**, 1842 (2008).
46. H. Chaabouni, L. L. Chapelon, M. Aimadeddine, J. Vitello, A. Farcy, R. Delsol, P. Brun, D. Fossati, V. Arnal, T. Chevolleau, O. Joubert, and J. Torres, *Microelectron. Eng.*, **84**, 2595 (2007).
47. C. Dubois, A. Sylvestre, H. Chaabouni, and A. Farcy, *Microelectron. Eng.*, **87**, 333 (2010).
48. S. Gates, S. P. Rao, V. Anandan, M. Krishnan, S. Cohen, Y. Ostrovski, N. Klymko, M. Chace, and D. Canaperi, *Microelectron. Eng.*, **91**, 82 (2012).
49. A. Grill and D. A. Neumayer, *J. App. Phys.*, **94**, 6697 (2003).
50. R. K. Iler, *The chemistry of silica: solubility, polymerization, colloid and surface properties, and biochemistry*, Wiley (1979).
51. M. Darnon, T. Chevolleau, T. David, N. Posseme, R. Bouyssou, R. Hurand, O. Joubert, C. Licitra, N. Rochat, F. Bailly, and C. Verove, *IITC*, 3 pp. (2011).
52. N. Rochat, A. Chabli, F. Bertin, M. Olivier, C. Vergnaud, and P. Mur, *J. Appl. Phys.*, **91**, 5029 (2002).
53. N. Rochat, M. Olivier, A. Chabli, F. Conne, G. Lefeuvre, and C. Boll-Burdet, *Appl. Phys. Lett.*, **77**, 2249 (2000).
54. M.-S. Kuo, A. R. Pal, G. S. Oehrlein, P. Lazzeri, and M. Anderle, *J. Vac. Sci. Technol. B*, **28**, 952 (2010).
55. P. Lazzeri, G. J. Stueber, G. S. Oehrlein, R. McGowan, E. Busch, S. Pederzoli, M. Bersani, and M. Anderle, *J. Vac. Sci. Technol. B*, **24**, 2695 (2006).
56. M. R. Baklanov, K. P. Mogilnikov, and Q. T. Le, *Microelectron. Eng.*, **83**, 2287 (2006).
57. P. Lazzeri, X. Hua, G. Oehrlein, E. Iacob, M. Barozzi, M. Bersani, and M. Anderle, *Appl. Surf. Sci. FIELD Full Journal Title: Applied Surface Science*, **252**, 7186 (2006).
58. G. Mannaert, M. R. Baklanov, Q. T. Le, Y. Travaly, W. Boullart, S. Vanhaelemeersch, and A. M. Jonas, *J. Vac. Sci. Technol. B*, **23**, 2198 (2005).
59. R. Bouyssou, M. El Kodadi, C. Licitra, T. Chevolleau, M. Besacier, N. Posseme, O. Joubert, and P. Schiavone, *J. Vac. Sci. Technol. B*, **28**, L31 (2010).
60. C. Licitra, R. Bouyssou, M. El Kodadi, G. Haberfehlner, T. Chevolleau, J. Hazart, L. Virot, M. Besacier, P. Schiavone, and F. Bertin, *Thin Solid Films*, **519**, 2825 (2011).
61. R. Hurand, R. Bouyssou, M. Darnon, C. Tiphine, C. Licitra, M. El-kodadi, T. Chevolleau, T. David, N. Posseme, M. Besacier, P. Schiavone, F. Bailly, O. Joubert, and C. Verove, *IITC*, 3 pp. (2011).
62. A. M. Ionescu, G. Reimbold, and F. Mondon, *International Semiconductor Conference*, 27 (1999).
63. L. Zhao, Z. Tokei, G. G. Gischia, M. Pantouvaki, K. Croes, and G. Beyer, in *2009 IEEE International Reliability Physics Symposium, Vols 1 and 2*, p. 848 (2009).
64. J. M. Jung, H. S. Kwon, W.-K. Lee, B.-C. Choi, H. G. Kim, and K. T. Lim, *Microelectron. Eng.*, **87**, 1680 (2010).
65. B. Lahlouh, J. A. Lubguban, G. Sivaraman, R. Gale, and S. Gangopadhyay, *Electrochem. Solid-State Lett.*, **7**, G338 (2004).
66. T. Rajagopalan, B. Lahlouh, J. A. Lubguban, N. Biswas, S. Gangopadhyay, J. Sun, D. H. Huang, S. L. Simon, D. Toma, and R. Butler, *Appl. Surf. Sci.*, **252**, 6323 (2006).
67. B. Xie and A. J. Muscat, *Microelectron. Eng.*, **82**, 434 (2005).
68. T. C. Chang, Y. S. Mor, P. T. Liu, T. M. Tsai, C. W. Chen, C. J. Chu, F. M. Pan, W. Lur, and S. M. Sze, *J. Electrochem. Soc.*, **149**, F145 (2002).
69. T. C. Chang, Y. S. Mor, P. T. Liu, T. M. Tsai, C. W. Chen, Y. J. Mei, and S. M. Sze, *J. Electrochem. Soc.*, **149**, F81 (2002).
70. S. V. Nitta, S. Purushothaman, N. Chakrapani, O. Rodriguez, N. Klymko, E. T. Ryan, G. Bonilla, S. Cohen, S. Molis, and K. McCullough, *Adv. Met. Conf. 2005, Proc.*, 325 (2006).
71. T. Oszinda, M. Schaller, and S. E. Schulz, *J. Electrochem. Soc.*, **157**, H1140 (2010).
72. O. Boehm, R. Leitsmann, P. Plauenitz, T. Oszinda, M. Schaller, and M. Schreiber, *Microelectron. Eng.*, **112**, 63 (2013).
73. A. Bhanap, B. Korolev, S. Nitta, S. Purushothaman, G. Bonilla, and E. T. Ryan, *Solid State Technol.*, **50**, 79 (2007).
74. Y. Uchida, S. Hishiya, N. Fujii, K. Kohmura, T. Nakayama, H. Tanaka, and T. Kikkawa, *Microelectron. Eng.*, **83**, 2126 (2006).
75. A. Ishikawa, Y. Shishida, T. Yamanishi, N. Hata, T. Nakayama, N. Fujii, H. Tanaka, H. Matsuo, K. Kinoshita, and T. Kikkawa, *J. Electrochem. Soc.*, **153**, G692 (2006).
76. T. Seo, T. Yoshino, N. Ohnuki, Y. Seino, Y. Cho, N. Hata, and T. Kikkawa, *J. Electrochem. Soc.*, **156**, H98 (2009).
77. T. Seo, T. Yoshino, N. Ohnuki, Y. Seino, Y. Cho, N. Hata, and T. Kikkawa, *J. Electrochem. Soc.*, **158**, H659 (2011).
78. K. Kohmura, H. Tanaka, S. Oike, M. Murakami, N. Fujii, S. Takada, T. Ono, Y. Seino, and T. Kikkawa, *Thin Solid Films*, **515**, 5019 (2007).
79. K. S. Yim, T. Nowak, B. Xie, and A. T. Demos, Applied Materials, Inc., USA, U.S. Pat. 8,216,861 (2012).
80. B. N. Varadarajan, K. M. McLaughlin, and B. Van Schravendijk, Novellus Systems, Inc., USA, U.S. Pat. 8,465,991 (2013).
81. P. Marsik, A. M. Urbanowicz, P. Verdonck, D. De Roest, H. Sprey, and M. R. Baklanov, *Thin Solid Films*, **519**, 3619 (2011).
82. A. Zenasni, V. Jousseau, P. Holliger, L. Favennec, O. Gourhant, P. Maury, and G. Gerbaud, *J. Appl. Phys.*, **102**, 094107/1 (2007).
83. S. Eslava, F. Iacopi, A. M. Urbanowicz, C. E. A. Kirschhock, K. Maex, J. A. Martens, and M. R. Baklanov, *J. Electrochem. Soc.*, **155**, G231 (2008).
84. K. Chan and A. T. Demos, Applied Materials, Inc., USA, U.S. Pat. 20140004717 (2014).
85. B. Xie, K. Chan, D. Cui, H. Ren, D. Raj, E. Hollar, S. Baluja, J. Rocha, M. Naik, and A. Demos, *IITC*, 335 (2014).
86. M. Darnon, T. Chevolleau, D. Eon, R. Bouyssou, B. Pelissier, L. Vallier, O. Joubert, N. Posseme, T. David, F. Bailly, and J. Torres, *Microelectron. Eng.*, **85**, 2226 (2008).
87. N. Posseme, T. Chevolleau, R. Bouyssou, T. David, V. Arnal, J. P. Barnes, C. Verove, and O. Joubert, *J. Vac. Sci. Technol. B*, **28**, 809 (2010).
88. N. Posseme, R. Bouyssou, T. Chevolleau, T. David, V. Arnal, M. Darnon, P. Brun, C. Verove, and O. Joubert, *J. Vac. Sci. Technol. B*, **29** (2011).
89. N. Posseme, L. Vallier, C. L. Kao, C. Licitra, C. Petit-Etienne, C. Mannequin, P. Gonon, S. Belostotskiy, J. Pender, S. Banola, O. Joubert, and S. Nemani, *IITC*, 3 pp. (2013).

90. N. Posseme, S. Barnola, O. Joubert, S. Nemani, and L. Vallier, Commissariat A L'energie Atomique Et Aux Energies Alternatives, Applied Materials, Inc., Cnrs Centre National De La Recherche Scientifique, France, U.S. Pat. 20140187035A1 (2014).
91. L. Zhang, R. Ljazouli, P. Lefauchaux, T. Tillocher, R. Dussart, Y. A. Mankelevich, J.-F. de Marneffe, S. de Gendt, and M. R. Baklanov, *ECS J. Solid State Sci. Technol.*, **2**, N131 (2013).
92. L. Zhang, R. Ljazouli, P. Lefauchaux, T. Tillocher, R. Dussart, Y. A. Mankelevich, J.-F. de Marneffe, S. de Gendt, and M. R. Baklanov, *Ecs Solid State Lett.*, **2**, N5 (2013).
93. H. Cui, R. J. Carter, D. L. Moore, H. G. Peng, D. W. Gidley, and P. A. Burke, *J. Appl. Phys.*, **97**, 113302 (2005).
94. J. Shoeb and M. J. Kushner, *J. Vac. Sci. Technol. A*, **29**, 051305-1 (2011).
95. T. Abell and K. Maex, *Microelectron. Eng.*, **76**, 16 (2004).
96. M. Aimadeddine, V. Arnal, D. Roy, A. Farcy, T. David, T. Chevolleau, N. Posseme, J. Vitiello, L. L. Chapelon, C. Guedj, Y. Brechet, F. Volpi, and J. Torres, *IITC*, p. 81 (2006).
97. B. White, G. Book, J. Hautala, M. Tabat, and M. Ieee, *IITC*, p. 193 (2004).
98. Z. C. Wu, Y. C. Lu, C. C. Chiang, M. C. Chen, B. T. Chen, G. J. Wang, Y. T. Chen, J. L. Huang, S. M. Jang, and M. S. Liang, International Electron Devices Meeting, p. 595 (2002).
99. F. Iacopi, M. R. Baklanov, E. Sleenckx, T. Conrad, H. Bender, H. Meynen, and K. Maex, *J. Vac. Sci. Technol. B*, **20**, 109 (2002).
100. Z. Chen, K. Prasad, C. Y. Li, P. W. Lu, S. S. Su, L. J. Tang, D. Gui, S. Balakumar, R. Shu, and R. Kumar, *Appl. Phys. Lett.*, **84**, 2442 (2004).
101. T. Mourier, V. Jousseau, F. Fusalba, C. Lecornec, P. Maury, G. Passemard, P. H. Haumesser, S. Maitrejean, M. Cordeau, R. Pantel, F. Pierre, M. Fayolle, and H. Feldis, *IITC*, p. 245 (2003).
102. J. Bonitz, S. E. Schulz, and T. Gessner, *Microelectron. Eng.*, **76**, 82 (2004).
103. M. Tada, Y. Harada, T. Tamura, N. Inoue, F. Ito, M. Yoshiki, H. Ohtake, M. Narihiro, M. Tagami, M. Ueki, K. Hijioka, M. Abe, T. Takeuchi, S. Saito, T. Onodera, N. Furutake, K. Arai, K. Fujii, and Y. Hayashi, *IEEE International Electron Devices Meeting 2003*, 35.2.1 (2003).
104. F. Iacopi, C. Zistl, C. Jehoul, Z. Tokei, Q. T. Le, A. Das, C. Sullivan, G. Prokopowicz, D. Gronbeck, M. Gallagher, J. Calvert, and K. Maex, *Microelectron. Eng.*, **64**, 351 (2002).
105. F. Iacopi, Z. Tokei, Q. T. Le, D. Shamiry, T. Conard, B. Brijs, U. Kreissig, M. Van Hove, and K. Maex, *J. Appl. Phys.*, **92**, 1548 (2002).
106. N. Jourdan, M. B. Krishtab, M. R. Baklanov, J. Meererschaut, C. J. Wilson, J. M. Ablett, E. Fonda, L. Zhao, S. Van Elshocht, Z. Tokei, and E. Vancoille, *Electrochem. Solid-State Lett.*, **15**, H176 (2012).
107. Y. Kimura, A. Kobayashi, D. Ishikawa, A. Nakano, K. Matsushita, and N. Kobayashi, *IITC*, 3 pp. (2012).
108. A. Kobayashi, D. Ishikawa, K. Matsushita, and N. Kobayashi, *IITC*, 3 pp. (2013).
109. S. Armini, J. L. Prado, J. Swerts, Y. Sun, M. Krishtab, J. Meererschaut, M. Blauw, M. Baklanov, and P. Verdonck, *Ecs Solid State Letters*, **1**, P42 (2012).
110. S. Armini, J. L. Prado, M. Krishtab, T. Conard, J. Meererschaut, Q. T. Le, P. Verdonck, and M. R. Baklanov, *Ecs Journal of Solid State Science and Technology*, **3**, N3106 (2014).
111. C. S. Allen, N. Annan, R. M. Blankenship, M. K. Gallagher, R. H. Gore, A. A. Lamola, and Y. You, Shipley Company LLC, USA, U.S. Pat. 6,420,441 (2002).
112. T. J. Dalton, S. E. Greco, J. C. Hedrick, S. V. Nitta, S. Purushothaman, K. P. Rodbell, and R. Rosenberg, International Business Machines Corporation, USA, U.S. Pat. 6,451, 712 (2002).
113. K. H. Pfeifer, E. R. Engbrecht, and M. K. Gallagher, *Solid State Technol.*, **49**, 59 (2006).
114. J. M. Calvert and M. K. Gallagher, *Semicond. Int.*, **26**, 56 (2003).
115. R. D. Miller, W. Volksen, V. Y. Lee, E. Connor, T. Magbitang, R. Zafran, L. Sundberg, C. J. Hawker, J. L. Hedrick, E. Huang, M. Toney, Q. R. Huang, C. W. Frank, and H. C. Kim, *ACS Symp. Ser.*, **874**, 144 (2004).
116. Y. You, A. A. Lamola, R. H. Gore, M. K. Gallagher, and N. Annan, Shipley Company, L. L. C., USA, U.S. Pat. 6,271,273 (2001).
117. M. Fayolle, V. Jousseau, M. Assous, E. Tabouret, C. le Cornec, P. H. Haumesser, P. Leduc, H. Feldis, O. Louveau, G. Passemard, and F. Fusalba, *IITC*, 208 (2004).
118. B. White, A. Knorr, W. Engbrecht, B. Kastenmeier, S. Das, R. McGowan, S. Satyanarayana, and M. Gallagher, *Microelectron. Eng.*, **82**, 348 (2005).
119. P. Enzel and T. Bein, *Chem. Mater.*, **4**, 819 (1992).
120. K. Moller, T. Bein, and R. X. Fischer, *Chem. Mater.*, **10**, 1841 (1998).
121. N. Wang, M. T. Li, and J. S. Zhang, *Mater. Lett.*, **59**, 2685 (2005).
122. M. R. Baklanov, F. Iacopi, and S. Vanhaelemeersch, IMEC, Globalfoundries Inc., USA, U.S. Pat. 8,540,890 B2 (2013).