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Characterization of dynamic self-heating in GaN HEMTs using gate resistance measurement

Adrien Cutivet, Flavien Cozette, Meriem Bouchilaoun, Ahmed Chakroun, Osvaldo Arenas, Marie Lesecq, Jean-Claude De Jaeger, Abdelatif Jaouad, François Boone, and Hassan Maher

Abstract—This paper reports on a new method for the characterization of transistors transient self-heating based on gate end-to-end resistance measurement. An alternative power signal is injected to the device output (between drain and source) at constant gate-to-source voltage. The dependence of gate resistance with temperature is used to extract the thermal impedance of the device in frequency domain via electrical measurement. This new method is validated on common-gate AlGaIn/GaN high-electron-mobility transistors on Si substrate under different experimental conditions, which demonstrates its potential to provide complete dynamic self-heating models for power transistors.

Index Terms—GaN, temperature measurement, dynamic self-heating, gate metal thermometry, HEMT

I. INTRODUCTION

HEMTs based on GaN are attractive to RF and power electronics designers due to the outstanding GaN properties (wide band gap, high saturation velocity and high current density) allowing tremendous performance in terms of power density and cut-off frequency. Cost-wise, GaN based heterostructure on silicon substrate is of major interest for several telecommunication and power conversion markets. However, this technology suffers from inherent limitation in terms of heat dissipation affecting devices overall performance and reliability. Extracting accurately the device temperature is thus of prime importance for modeling electrical characteristics and predicting device lifetime.

Literature reports on an electrical method (G-RTD) using gate resistance temperature dependence to determine device temperature in a straightforward manner [1-3]. A comparison of this method with micro-Raman spectroscopy has proved this method to be reliable with a net uncertainty of $\pm 5\%$ [4]. G-RTD method is however restricted to transistors featuring

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A. Cutivet, F. Cozette, M. Bouchilaoun, A. Chakroun, O. Arenas, A. Jaouad, F. Boone and H. Maher are with Université de Sherbrooke, Sherbrooke QC J1K2R1 Canada (e-mail: adrien.cutivet@usherbrooke.ca).

F. Cozette, M. Lesecq and J.-C. De Jaeger are with Univ. Lille, CNRS, Centrale Lille, ISEN, Univ. Valenciennes, UMR 8520 - IEMN, F-59000 Lille, France (e-mail: flavien.cozette@ed.univ-lille1.fr).

double-ended gate where separated pads enable direct measurement of gate resistance. For transistors with a single gate access, the use of a dedicated metal sensor upon a passivation layer has been successfully demonstrated [5].

While many other studies detail successful approaches to measure on-wafer HEMT steady-state temperature, fewer studies are related on the matter of self-heating for time-dependent dissipated power. However, it is crucial to model the temperature rise for RF applications with time-dependent power level (such as radars and data transmission using amplitude modulation) and power electronics where transistors are used in switching operations.

In this frame, Micro-Raman spectroscopy has demonstrated the possibility to provide excellent accuracy with an approximate $1 \mu\text{m}$ spatial resolution and time resolutions down to 10 ns [6-8]. Thermoreflectance imaging has been proved to provide useful information in a complementary way with Micro-Raman [9]. Regarding methods based on electrical measurement, [10] reports on a method based on 3ω measurement using HEMT ON-resistance to extract thermal dynamic characteristic, but only in the linear operation mode of $I_d(V_{ds})$ characteristic (ohmic area).

In this paper, a new and robust electrical method for double-ended gate HEMTs is introduced, it makes use of gate resistance frequency measurement to monitor dynamic temperature variations at any bias point. This new method enables a complete and accurate thermal impedance determination suitable for further modeling and simulation works useful for power circuit designers.

II. EXPERIMENTAL PROCEDURE

A. Device Under Test

The method is carried out on a coplanar common-gate AlGaIn/GaN MOS-HEMT fabricated on commercial epi-wafers (EPIGaN) grown by Metal-Organic Chemical Vapor Deposition (MOCVD) on Si substrate. The epitaxial structure consists of a $1.8 \mu\text{m}$ $\text{Al}_{0.18}\text{Ga}_{0.82}\text{N}$ back barrier layer, a 150 nm undoped GaN channel layer, a thin 4 nm $\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ barrier layer and a 50 nm SiN in-situ dielectric layer. A sheet carrier density of $1.08 \cdot 10^{13} \text{ cm}^{-2}$ and an electron mobility of $1810 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ are determined by Hall Effect measurement. The 50 nm SiN dielectric layer is dry-etched before e-beam evaporation of the ohmic contact metal stack (Ti/Al/Ni/Au). After annealing, a nitrogen ion implantation isolation is performed and the contact resistance determined by TLM

measurement is $0.35 \Omega \cdot \text{mm}$. The 50 nm SiN dielectric layer is dry-etched in the gate electrode area and a 5 nm SiO_x gate dielectric is deposited by PECVD [11]. A Ni/Au (40/600 nm) metal deposition is performed featuring photolithography and e-beam evaporation to make a 1.5 μm long meander gate electrode with 0.5 μm and 2.0 μm field-plate extensions toward source and drain respectively. The deposited Au resistivity is evaluated to be $9.1 \times 10^{-8} \Omega \cdot \text{m}$. Gate leakage current is lower than 10 nA for all biases used in this study thanks to the high quality of the gate oxide layer. Gate-to-drain and gate-to-source distances are 6.0 μm and 1.5 μm respectively for a total gate width of 318 μm . A SEM image of the device is shown in figure 1.

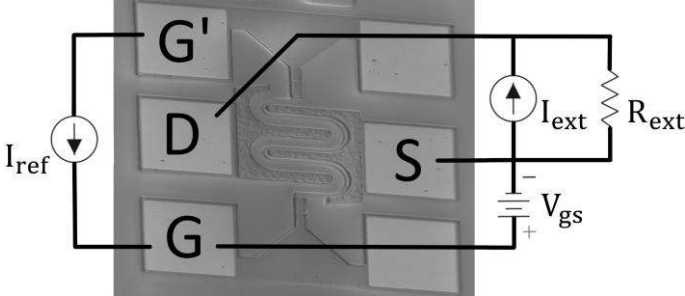


Fig. 1. SEM image of a common-gate GaN HEMT under test with configuration of voltage and current sources. Annotated contacts: G (Gate access n¹), G' (Gate access n²), D (Drain access) and S (Source access).

B. Measurement Setup

The setup is described in figure 1. A DC current source injects a current (I_{ref}) along the gate to measure gate resistance (R_g). Gate-source voltage is controlled with a V_{gs} bias while a Keithley 6221 source applies a DC and AC external current (I_{ext}) with an external resistance (R_{ext}) permitting to control V_{ds} . Considering a static drain current I_{d0} and a drain-source voltage V_{ds0} with alternative variations $I_d(f)$ and $V_{ds}(f)$, the HEMT dissipated power (P) in frequency domain is as follows:

$$P(f) = V_{ds}(f) \cdot I_{d0} + V_{ds0} \cdot I_d(f) \quad (1)$$

$$P(2f) = \frac{1}{2} \cdot V_{ds}(f) \cdot I_d(f) \quad (2)$$

A SR850 DSP lock-in amplifier from Stanford Research Systems permits the measurement of $V_{gg'}(f)$ and $I_d(f)$ for a frequency range of 1 mHz to 102.4 kHz. By considering the following assumptions:

- The device temperature (T) is assumed to be the highest value along the gate length axis averaged along the gate width axis.
- The gate is isotherm and its temperature is equal to T [12].
- The dependence of R_g with temperature is linear with respect to T which in turn is linear with respect to P for the range of variation.
- Values of I_{ref} are chosen sufficiently small so that $V_{gg'}$ magnitude is low enough to consider I_d constant along the gate.

The device thermal impulse response (Z_{TH}), also known as the thermal impedance, is introduced and yields:

$$Z_{TH}(f) = T(f)/P(f) = R_g(f)/\left(\frac{\partial R_g}{\partial T} \cdot P(f)\right) \quad (3)$$

The device thermal step response (Z'_{TH}), also known as transient thermal impedance, can be approximated if supposed constant over the range of temperature investigated by a simple variable change [13]:

$$Z'_{TH}(t) = |Z_{TH}(2\pi f \rightarrow 1/t)| \quad (4)$$

While gate leakage current ($\sim 10^{-8}$ A) can be neglected in comparison with I_{ref} ($\sim 10^{-4}$ A), a displacement current arising from gate-to-drain electrical coupling may account for a significant parasitic contribution on $V_{gg'}(f)$ such as:

$$V_{gg'}(f) = R_g(f) \cdot I_{ref} + j\alpha \cdot f \cdot V_{gd}(f) \quad (5)$$

Where α is a real constant accounting for the total gate-to-drain capacitance and distributed gate resistance. A de-embedding technique was introduced in [4] to cancel the effect of a parasitic gate conduction current. A similar approach is hereby introduced to cancel the effect of this displacement current using complex values:

$$R_g(f) = \left(V_{gg'}^{I_{ref}^+}(f) - V_{gg'}^{I_{ref}^-}(f) \right) / (2I_{ref}) \quad (6)$$

Where $V_{gg'}^{I_{ref}^+}(f)$ and $V_{gg'}^{I_{ref}^-}(f)$ are $V_{gg'}(f)$ measurement obtained with a positive and negative value of I_{ref} respectively.

III. MEASUREMENT AND RESULTS

A. Steady-state results

The dependence of R_g on T is investigated through on-wafer measurement using 4-wire sensing and a thermally controlled chuck while the device is unbiased. The gate access pad resistance is estimated to be less than 1 ohm and is therefore neglected. Figure 2.a shows the results for a chuck temperature ranging from 25 to 100°C. A linear dependency is acknowledged with $\frac{\partial R_g}{\partial T} = 19.4 \text{ m}\Omega \cdot \text{K}^{-1}$ and a correlation factor of 0.9996. Figure 2.b shows the $I_d(V_{ds})$ characteristic along with the extracted temperature. A maximum temperature of 87°C is extracted at $P = 0.81 \text{ W}$.

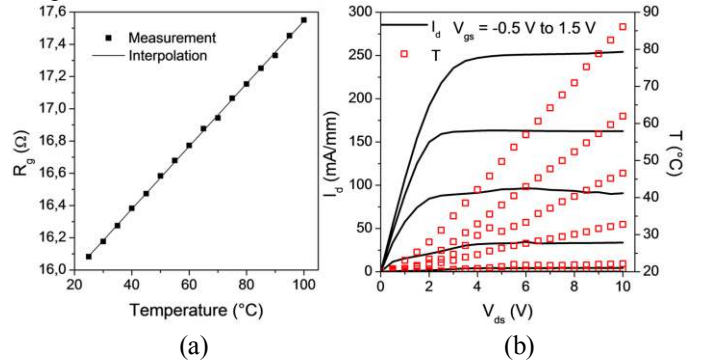


Fig. 2. (a) Gate resistance versus temperature obtained with on-wafer 4-wire sensing and thermally controlled chuck. (b) Device under test $I_d(V_{ds})$ characteristic and associated steady-state temperatures extracted for V_{gs} and V_{ds} ranging from -0.5 to 1.5 V by steps of 0.5 V and 0 to 10 V respectively.

B. Extensive results and analysis

To assess the reproducibility and validity of this thermal impedance extraction method, measurements are conducted under different experimental conditions described in table 1. Figure 3 shows $|Z_{TH}(f)|$ extraction from 1 Hz to 100 kHz. For standard and 1-4 conditions, corresponding to the transistor saturation region, (eq.1), (eq.3) and (eq.6) are used. Condition 5 consists in using the transistor in ohmic region. In that case the second harmonic term $P(2f)$ is typically higher than $P(f)$ and therefore (eq.2) and (eq.3) are used. As expected, all the experimental condition variations have no effect on the extraction giving the same values in a $\pm 3\%$ range, except for the results obtained in ohmic region for which $|Z_{TH}(f)|$ values are typically inferior. This last result is attributed to the fact that a lower proportion of electric field is located near the drain-side gate edge at low V_{ds} which enables a better local heat dissipation [14].

The results are coherent with literature [10] with $|Z_{TH}(f)|$ dropping down significantly for frequencies above 500 Hz and maintaining a quasi-constant value for frequencies below. $|Z_{TH}(f)|$ is 40 $\text{K}\cdot\text{W}^{-1}$ at 100 kHz, meaning that a higher frequency is needed to attain thermal impedance cut-off frequency, as stated in literature [10]. A slight increase of $|Z_{TH}(f)|$ is observed below 10 Hz, attributed to an imperfect contact of the sample backside to an ideal thermal mass. The values obtained at the lowest frequencies are coherent with $\partial T/\partial P$ steady-state value evaluated from III.A results ($\approx 90 \text{ K}\cdot\text{W}^{-1}$). Furthermore, the phase of $Z_{TH}(f)$ is extracted using (eq.3) and (eq.6), and is shown in figure 3 inset for frequencies above 1 kHz. The phase value is observed to decrease to attain -30° at 100 kHz as it is expected to converge toward a -90° value at cut-off frequency where the temperature variation is completely out of phase with the dissipated power variation.

In a final step, the device transient thermal impedance Z_{TH}^t is extracted using (eq.4). The results are shown in figure 3 from 1.6 μs to 160 ms. At 1.6 μs , temperature has already risen to nearly half of the steady-state value which is coherent with literature to the authors knowledge [15-16].

Conditions	Parameters
Standard	$V_{gs} = 1.0 \text{ V}$, $V_{ds0} = 5.5 \text{ V}$, $V_{ds}(f) = 1.0 \text{ V}$ and $I_{ref} = 0.50 \text{ mA}$
1	Lower R_g measurement current: $I_{ref} = 0.05 \text{ mA}$
2	Different bias: $V_{gs} = 0.5 \text{ V}$, $V_{ds0} = 7.5 \text{ V}$
3	Lower signal amplitude: $V_{ds}(f) = 0.2 \text{ V}$
4	Another HEMT from the same process batch
5	Ohmic region: $V_{ds0} = 0 \text{ V}$, $V_{ds}(f) = 0.2 \text{ V}$

Tab. 1. Sets of measurement parameters used for $Z_{TH}(f)$ extraction.

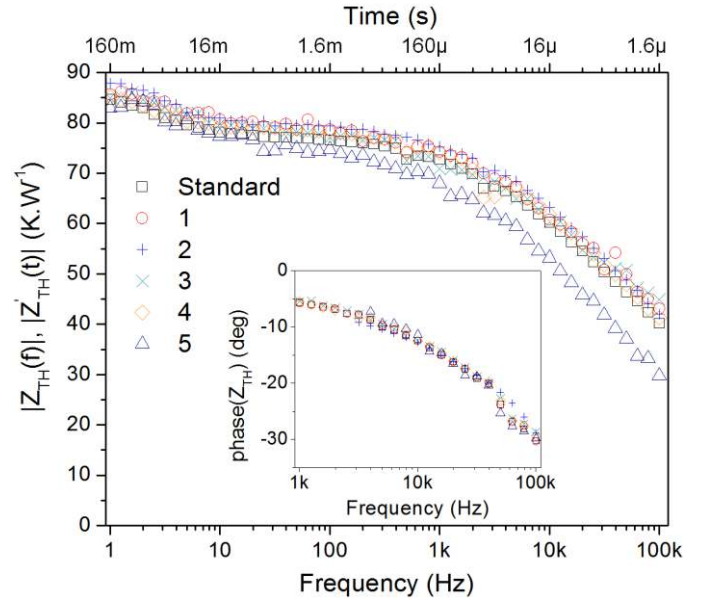


Fig. 3. HEMT thermal impedance in frequency domain and transient thermal impedance in time domain obtained under various experimental conditions. Inset: phase extraction of thermal impedance.

IV. CONCLUSION

This paper introduces an original and straightforward thermal impedance extraction method relying entirely on electrical characterization for transistors suited for direct gate resistance measurement. The theory and the experimental setup are described and tested on GaN HEMT devices. Thermal impedance extraction is conducted under various experimental conditions to assess validity and overall reliability of this new method. The results are shown to be independent of power signal amplitude, gate current resistance measurement and gate bias conditions as well as identical for another similar HEMT. This highlights the accuracy of this technique as well as its adaptability and potential for application on transistors from other technologies. Furthermore, an experimental setup capable of a maximum operation frequency up to 20 MHz would allow extracting the transient thermal impedance with a time resolution under 10 ns, which is equivalent to state of the art Micro-Raman spectroscopy performance.

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