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Ahmed Chakroun, Abdelatif Jaouad, Meriem Bouchilaoun, Osvaldo Arenas, Ali Soltani, et al.. Normally-off AlGa_N/Ga_N MOS-HEMT using ultra-thin Al_{0.45}Ga_{0.55}N barrier layer. *physica status solidi (a)*, 2017, 214 (8), 10.1002/pssa.201600836 . hal-01914374

HAL Id: hal-01914374

<https://hal.science/hal-01914374>

Submitted on 16 Nov 2018

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Normally-off AlGaN/GaN MOS-HEMT using ultra-thin Al_{0.45}Ga_{0.55}N barrier layer

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In this work, we report on the fabrication of a normally-off AlGaN/GaN Metal–Oxide–Semiconductor High Electron Mobility Transistor (MOS-HEMT) using an ultra-thin Al_{0.45}Ga_{0.55}N barrier layer. The AlGaN barrier was thinned down to 1 nm using a digital etching process (Oxidation/Etching) and was followed by a PECVD deposition technique of a 7 nm thick SiO_x layer used as gate insulator. Thanks to the thin AlGaN barrier layer (4 nm), only a few digital etching

cycles are required to shift the threshold voltage toward positive values. The fabricated normally-off device exhibits a pinch-off voltage of +1.1 V, a maximum I_{DS} current of 460 mA mm⁻¹ at $V_{GS} = +5$ V, an On-state resistance (R_{ON}) of 7.8 Ω · mm and an I_{ON}/I_{OFF} ratio higher than 10⁹. Moreover, the pulsed I_{DS} – V_{DS} and capacitance–voltage (C – V) curves versus frequency confirm that there is no damage induced by the digital etching process.

Keywords AlGaN, digital etching, GaN, high electron mobility transistors, metal–oxide–semiconductor structures, passivation

1 Introduction Thanks to its superior fundamental properties, Gallium Nitride (GaN) has received extensive attention for high power and high frequency applications. AlGaN/GaN High Electron Mobility Transistors (HEMTs) have demonstrated tremendous potential due to their high sheet carrier density and 2DEG electron mobility. Standard AlGaN/GaN HEMT structures have a negative threshold voltage (V_{TH}), giving a “normally-on” operation mode. One of the major challenges for GaN-HEMTs power devices is the achievement of an enhancement-mode device “normally-off,” required for a simpler drive circuitry and safer operation [1].

Several techniques have been reported in order to shift the threshold voltage toward positive values. The most cited ones are: fluorine (F⁻) ion implantation [1–4], AlGaN barrier recess [5–8], and p-GaN (or p-AlGaN) gated structure [9–10]. The gate recess approach by dry etching has been largely used but it suffers from a non-uniformity recess depth and a high plasma induced damage, which considerably deteriorates the electron mobility in the channel and the device reliability [11]. To avoid the plasma induced damage, some works reported

on the use of digital etching process to etch the AlGaN barrier layer. This consists of barrier oxidation using a soft oxygen-based plasma followed by a wet-chemistry removal of the formed oxide layer [12]. The major drawback of this technique is the extremely low etching rate (~5 Å/cycle). Sixty-three Oxidation/Etching cycles have been used to etch a 24 nm thick AlGaN barrier [12]. In addition, the reported MOSHEMT device exhibits a large hysteresis (~0.7 V), suggesting a deficient Al₂O₃/GaN interface with an estimated interface traps density (D_{it}) of 2.6×10^{12} eV⁻¹.cm⁻² [12].

In this work, we report on the achievement of a normally-off AlGaN/GaN MOS-HEMT by using an ultra-thin Al_{0.45}Ga_{0.55}N barrier and a digital etching process followed by an optimized PECVD-SiO_x passivation procedure. Thanks to the initially thin Al_{0.45}Ga_{0.55}N barrier (4 nm), only six Oxidation/Etching cycles are needed to shift the threshold voltage toward positive values. The fabricated device exhibits stable characteristics, with a positive pinch-off voltage of +1.1 V, an I_{DS} current of 460 mA mm⁻¹ at $V_{GS} = +5$ V and a gate leakage current below 1 nA mm⁻¹. Based on the hysteresis measurements, the extracted D_{it} was

estimated to be as low as $1.49 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. This showcases the low damage induced by the digital etching technique and the efficiency of the proposed passivation process.

2 Experimental The AlGaIn/GaN MOS-HEMTs were fabricated on commercial HEMT wafers (supplied by EpiGaN) grown by Metal-Organic Chemical Vapor Deposition (MOCVD) on a Si substrate. The epitaxial structure consists of an $\text{Al}_{0.08}\text{Ga}_{0.92}\text{N}$ back barrier layer, a 150 nm undoped GaN channel layer and a thin 4 nm $\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ barrier layer. The epitaxial structure was finally capped with a 50 nm in situ SiN layer. The fabrication process begins by dry-etching the in situ SiN layer before the e-beam evaporation of the ohmic contact metal stack (Ti/Al/Ni/Au). Rapid thermal annealing was then performed at 875 °C for 30 sec in N_2 ambient. Device isolation was achieved by nitrogen ion implantation. For the gate electrode, the 50 nm SiN cap layer was first etched using very low power (5W) SF_6 -based ICP plasma. The revealed AlGaIn layer, in the gate area, was then oxidized using an O_2 plasma asher for 2 min. The sample was then dipped in an HCl: H_2O (1:10) solution for 1 min to remove the formed oxide layer. After six digital etching cycles, the AlGaIn barrier was thinned down to near 1 nm, as confirmed by Atomic Force Microscopy (AFM) shown in Fig. 1(b). A control sample, without digital recess, was also fabricated as a reference. Both samples were then cleaned and annealed at 420 °C for 20 min under a N_2 ambient to desorb the F^- ions from the AlGaIn surface [13]. Prior to the gate dielectric layer deposition, the samples were pretreated using a KOH solution, followed by an immersion in HCl for 2 min. A 7 nm thick PECVD- SiO_x layer was then deposited as a gate insulator using the passivation process previously reported in [14]. Finally, a Ni/Au (40/600 nm) gate metal stack was deposited by e-beam evaporation. Fig. 1(a) illustrates a schematic of the fabricated MOS-HEMT device using digital etching process. The etching rate, extracted from the Atomic Force Microscopy (AFM) analyses, is about 5 Å/cycle, as can be seen in Fig. 1(b). Electrical characterizations were performed using a Keithley 4200SCS analyzer.

3 Results and discussion Figure 2 shows the DC output characteristics for the fabricated AlGaIn/GaN

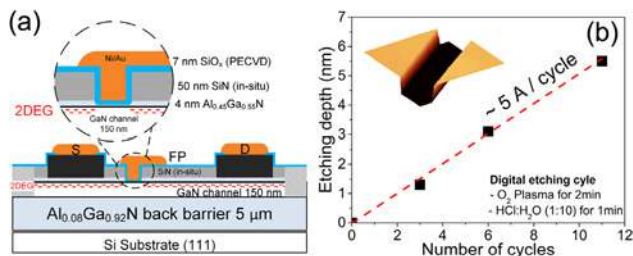


Figure 1 (a) Schematics of the fabricated MOS-HEMT and (b) digital etching depth versus digital etching cycles.

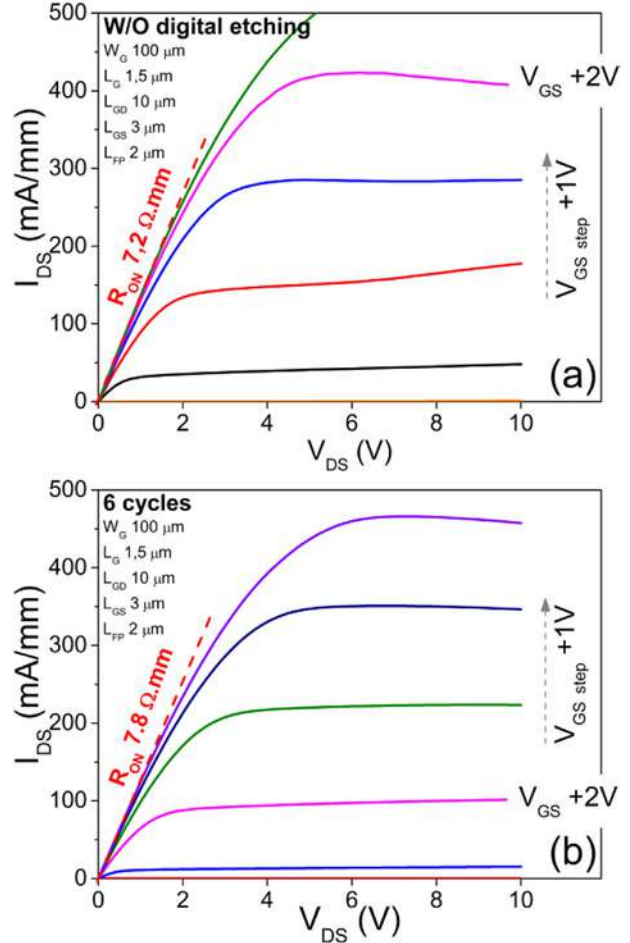


Figure 2 $I_{\text{DS}}-V_{\text{DS}}$ characteristic measured on fabricated MOS-HEMTs (a) W/O digital etching (reference) and (b) with six cycles.

MOS-HEMTs with a 1.5 μm gate length, a 10 μm gate-to-drain distance, a 3 μm gate-to-source distance, and a 2 μm field plate length. The MOS-HEMT device, fabricated on a reference sample, without digital etching (Fig. 2(a)), demonstrates a normally-on operation with a pinch-off voltage of -1.2 V and an On-state resistance (R_{ON}) of $7.2 \Omega \cdot \text{mm}$. The MOS-HEMT with six cycles of digital etching shows a normally-off operation with a drain current density of 460 mA mm^{-1} at $V_{\text{GS}} = +5 \text{ V}$ (Fig. 2(b)). The extracted R_{ON} is slightly higher, about $7.8 \Omega \cdot \text{mm}$, showing that no significant surface degradation was induced by digital etching on the device R_{ON} .

Figure 3 shows the device hysteresis transfer characteristics ($I_{\text{DS}}-V_{\text{GS}}$) at $V_{\text{DS}} = 10 \text{ V}$. The pinch-off voltage (V_{p}) was shifted from -1.2 to $+1.1 \text{ V}$ after six cycles of digital etching. The maximum G_{m} peaks, measured on both devices, were about 130 mS mm^{-1} as can be seen in Fig. 3 (a). The threshold voltage (V_{TH}) measured at $I_{\text{DS}} = 1 \text{ mA mm}^{-1}$ was shifted from -1.9 to $+0.3 \text{ V}$ after AlGaIn barrier thinning as can be seen in Fig. 3(b). A low hysteresis was observed in both samples on (a) linear and (b)

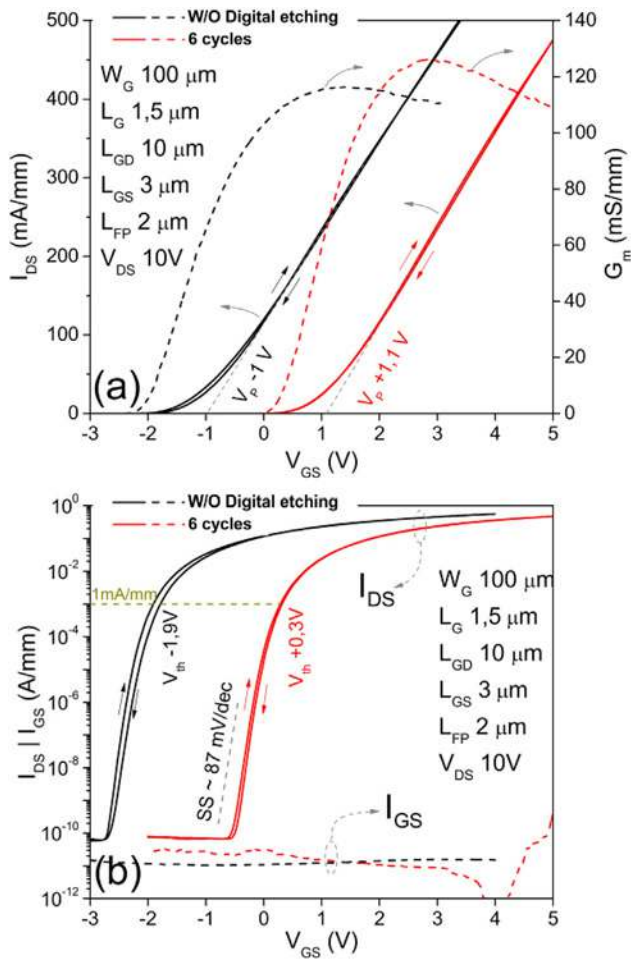


Figure 3 (a) Linear and (b) semi-logarithmic transfer characteristics $I_{DS}-V_{GS}$ of the fabricated MOS-HEMTs device.

semi-logarithmic scale $I_{DS}-V_{GS}$ curves. This demonstrates the efficiency of the gate recess and the passivation processes. Moreover, thanks to the high quality of the 7 nm PECVD-SiO_x gate insulator, the device exhibits a low gate leakage current. For the whole measurement range, the maximum gate leakage current (I_{GS}) is below 1 nA mm⁻¹. Furthermore, the off-state drain leakage current is also below 1 nA mm⁻¹, giving an I_{ON}/I_{OFF} ratio higher than 10⁹. The sub-threshold slope (SS) extracted from the transfer characteristic is about 87 mV dec⁻¹ for both devices, as can be seen in Fig. 3(b).

Circular MOS capacitors, with a 100 μm diameter, were also fabricated on both samples. Figure 4 shows the hysteresis capacitance–voltage ($C_{GS}-V_{GS}$) measurements performed at frequency ranged from 10 to 100 kHz. Both devices show good surface potential modulation with very low hysteresis. MOS capacitor fabricated on the control sample, without digital etching, shows a maximum accumulation capacitance of 460 nF.cm⁻². By thinning down the AlGa_{0.45}N barrier to near 1 nm using six oxidation/etching cycles, the threshold voltage is positively shifted and the maximum accumulation capacitance value increases

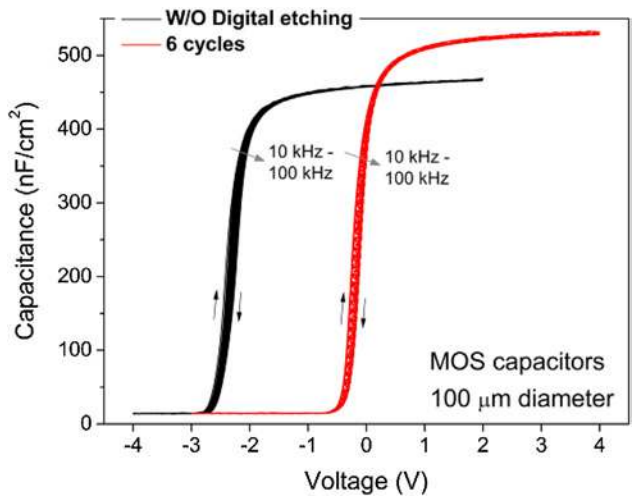


Figure 4 Capacitance–Voltage ($C_{GS}-V_{GS}$) hysteresis measurements performed on MOS capacitors at frequencies ranging from 10 to 100 kHz with a 10 kHz step.

to 530 nF.cm⁻². Using the equation: $D_{it} = C_{MOS} \cdot \Delta V_{TH}/q$ [2, 6], the extracted traps density (D_{it}) for the reference sample without digital etching is estimated to be $3.71 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. For the gate recessed sample, using six cycles of digital etching, the estimated D_{it} was as low as $1.49 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. This indicates that there is no major damage induced by the digital etching process. Due to the low thickness of the SiO_x-PECVD dielectric layer used in this study (7 nm), the $C-V$ two-step behavior, as previously reported by Yatabe et al. [15], is not observed in our reference sample, even at higher voltage (up to +6 V). Moreover, a catastrophic dielectric breakdown was observed at a voltage around +6.5 V. This dielectric breakdown was also confirmed by the large increase in the dielectric leakage current after the dielectric breakdown.

Pulsed $I_{DS}-V_{DS}$ characteristics were performed on the normally-off MOSHEMT device, achieved using AlGa_{0.45}N barrier digital etching. The measurement pulse width was 500 ns and the period was fixed to 10 ms. The results, as shown in Fig. 5, demonstrate a negligible gate lag and a low drain lag, below 8%, for a drain voltage of up to +40 V. These results strongly support the high SiO_x/AlGa_{0.45}N interface quality and that no damage was induced by the proposed digital etching process.

4 Conclusions In summary, a normally-off MOS-HEMT device with extremely low hysteresis was demonstrated by using an ultra-thin Al_{0.45}Ga_{0.55}N barrier layer. The electrical characterizations show a pinch-off voltage (V_p) of +1.1 V, a threshold voltage of +0.3 V at $I_{DS} = 1 \text{ mA mm}^{-1}$, a maximum drain current of 460 mA mm⁻¹, and a low gate and drain leakage current. The device also shows an I_{ON}/I_{OFF} ratio higher than 10⁹ and a Sub-threshold slope of 87 mV dec⁻¹. From $C-V$ and $I_{DS}-V_{GS}$ hysteresis measurements, a D_{it} value as low as $1.49 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ has been extracted for the sample

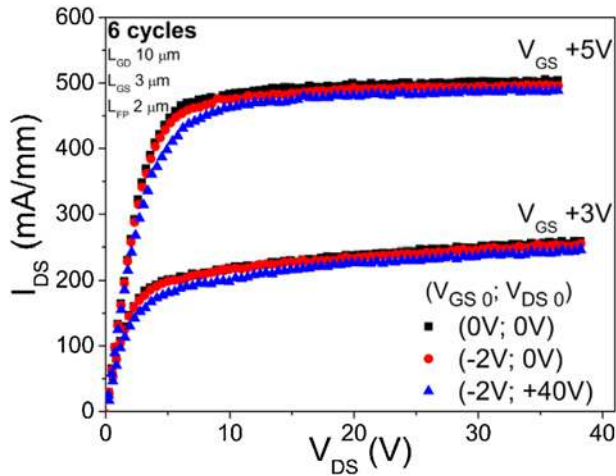


Figure 5 Pulsed I_{DS} - V_{DS} curves measured on MOSHEMT device with six cycles of digital etching. Pulse width = 500 ns, period = 10 ms.

with the gate digital etching recess. All these results confirm the low damage induced by the digital etching recess at the $\text{SiO}_x/\text{AlGaIn}$ interface. The usage of initial thin $\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ barrier reduces the recess time by digital etching required for this critical step. This approach could be used for the monolithically integration of enhancement and depletion (E/D) mode GaN devices on the same wafer, which will simplify drastically circuit design.

Acknowledgements Authors would like to acknowledge Caroline Roy, Adrien Cutivet and all LNN staff for their contributions in microfabrication process, pulsed characterizations and for fruitful discussions. LN2 is a joint International Research Laboratory (Unité Mixte Internationale UMI 3463) funded and co-operated by CNRS (France) and Université de Sherbrooke (Canada) as well as INSA Lyon, ECL, CPE, Université Grenoble Alpes (UGA), as well as the French national nanofabrication network RENATECH.

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