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# Wet Metallization of High Aspect Ratio TSV Using Electrografted Polymer Insulator to Suppress Residual Stress in Silicon

Thomas Dequivre, Gitanjali Kolhatkar, Azza Hadj Youssef, Xuan T. Le, Gessie M. Brisard, Andreas Ruediger, and Serge A. Charlebois, *Member, IEEE*

**Abstract**— Through-Silicon-Vias (TSV) are the key to 3D integrated microsystems. Their fabrication leads to reliability issues linked to the thermo-mechanical stress induced in the silicon around the vias. In this work, we propose to reduce the silicon residual stress in high aspect ratio copper TSVs (HAR TSV) using an electrografted polymer insulator, poly-4-vinylpyridine (P4VP), in replacement of the traditional silicon oxide layer. We use Raman spectroscopy to make the first investigation of the residual stress in the Si around P4VP insulated TSVs and compare it to SiO<sub>2</sub> insulated TSVs. The results show that P4VP acts as a stress buffer layer because of its particular mechanical properties as the measured residual stress in Si is significantly reduced at room temperature around the polymer insulated HAR TSVs. The potential benefits of such a technology are not only a better thermo-mechanical reliability of 3D integrated microsystem, but also a greater integration density.

**Index Terms** — Dielectric, Electronic packaging, Electrografting, Isolation technology, Microfabrication, Polymer films, Stress measurement, Three-dimensional integrated, Through Silicon Vias, Keep Out Zone.

## I. INTRODUCTION

THE development of 3D integration technologies constitutes a complementary approach to the constant effort realized on integrated circuit (IC) miniaturization. In 3D integration, dies are stacked and connected to each other using vertical interconnections, insulated from the silicon (Si) substrate, called through silicon vias (TSV). This technology allows better electrical performances, higher transistor density and advanced functionalities [1], [2].

The conductivity of a TSV depends on its filling material. Different materials have been used such as doped polysilicon

[3], tungsten [4] or copper [5]. Because of their enhanced electrical performances, Cu TSVs are receiving enormous interest from the industry. The Cu TSV metallization normally includes the deposition of an insulator (to ensure the electrical insulation of the interconnection), the deposition of a barrier layer (to prevent the Cu migration from the interconnection to the Si substrate [6]) and the electroplating of the Cu filling. A TSV therefore consists of a variety of materials with different mechanical properties deposited at different temperatures. This heterogeneous structure is a source of stress that affects the electrical and mechanical properties and reliability of the 3D interconnections during the fabrication or the operation of a microsystem. This induced stress can cause mobility shifts in the devices through piezoresistivity effects [7], Cu via protrusion, cracks and material delamination [8] until degradation of the device's performance or mechanical failure of the Cu TSV.

This is one of the main technological challenge one faces to integrate Cu TSVs in the microsystem fabrication process flow that impact significantly the layout optimization. Indeed, while transistor placement is forbidden within a significant keep-out-zone (KOZ) around each TSV, the area above the TSV is also often forbidden to interconnections for mechanical integrity reasons. The KOZ defines the minimum distance between two TSV to ensure the mechanical reliability of the microsystem, and the minimum distance between a TSV and an active device to minimize the impact on the carrier mobility. Electrical KOZ is defined based on a 7% mobility change or an equivalent stress of 100 MPa [9] (some state a 5 % mobility change [7]). Moreover, the Si stress around a TSV is proportional to the square of the TSV radius [9]. Thus, scaling down TSVs to few micrometers radius openings can significantly reduce the Si residual stress, along with a gain of real estate in the design.

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However, the metallization of narrow structures in high aspect ratio (HAR) TSVs is challenging. A lot of efforts are dedicated by the community to mitigate the stress induced by TSV. Some study the residual stress coming from the electrodeposition process and annealing of copper itself or design strategies [9]–[13].

We have been studying an innovative technology for insulating TSVs based on the electrografting of an organic polymer, poly-4-vinylpyridine (P4VP) [14]–[17]. Indeed, the P4VP electrografting process has shown promising results to insulate high aspect ratio copper TSVs in Vial-Last for the 3D integration of an imaging system [17]. This process is of interest as it provides an interesting alternative to SiO<sub>2</sub> based materials for high aspect ratio copper TSVs insulation in 3D integration process flow. Copper TSVs cannot be metallized in Via-First as the Front End Of Line requires high temperature processes that cause the copper filling to diffuse into the silicon substrate [18]. The deposition of SiO<sub>2</sub> based dielectric is thus limited to Chemical Vapor Deposition based methods, which are costly to implement to obtain a conformal and uniform layer in such deep and narrow structures. On the contrary in the same conditions of integration, the electrografted polymer film is highly conformal and uniform, easy to implement and shows similar dielectric film properties than that of SiO<sub>2</sub> [15].

In this paper, we will review the basic phenomena leading to the induced mechanical stress and demonstrate the use of an organic insulator between the silicon substrate and the Cu TSV core to overcome the problem. We report the first measurements of the stress buffering effect of the polymer in HAR Cu TSV.

## II. ORIGIN OF THE THERMOMECHANICAL STRESS

Let us recall the coefficient of thermal expansion (CTE), of Si (2.6 ppm/°C) and Cu (17.7 ppm/°C) [19]. In the hypothesis that a Cu TSV is formed at a given temperature and that the deposition process produces no stress in the Cu core, then no stress will be present in the materials at that temperature (therefore dubbed zero-stress temperature). At any other temperature, a mechanical stress is induced in the Si substrate.

The thermomechanical behavior of the TSV is closely linked to the nature of its insulating material as the stress is transmitted to the surrounding Si through the insulator. From basic principles, one can show that the main dependences of the radial stress induced in the silicon by the CTE difference of materials follows:

$$\sigma_{Si} \propto (\bar{\alpha}_{Cu,In} - \alpha_{Si}) \bar{E} \Delta T, \quad (1)$$

$$\bar{\alpha}_{Cu,In} = \frac{\alpha_{Cu} R_{Cu} + \alpha_{In} t_{In}}{R_{Cu} + t_{In}}, \quad (2)$$

$$\bar{E}_{Cu,In}^{-1} \propto \frac{1}{R_{Cu} + t_{In}} \left\{ \frac{R_{Cu}}{E_{Cu}} + \frac{t_{In}}{E_{In}} \right\}, \quad (3)$$

$$\bar{E}^{-1} \propto \frac{1}{E_{Cu,In}} + \frac{1}{E_{Si}}, \quad (4)$$

where  $\Delta T$  is the thermal excursion away from the zero-stress

temperature,  $\alpha_{Cu}$ ,  $\alpha_{In}$  and  $E_{Cu}$ ,  $E_{In}$  the CTE and Young's modulus of the materials respectively,  $R_{Cu}$  the radius of the copper core and  $t_{In}$  the thickness of the insulating layer. The radius of the hole in silicon is  $R = R_{Cu} + t_{In}$ . Three effective properties have also been defined:  $\bar{\alpha}_{Cu,In}$  and  $\bar{E}_{Cu,In}$  are effective CTE and Young's modulus for the copper core and insulating layer pair, while  $\bar{E}$  is an effective Young's modulus for the three component system. The definition of the stresses and other parameters are illustrated in Fig. 1.

In comparison to Cu or Si, the insulating SiO<sub>2</sub> has a slightly smaller Young's modulus and smaller CTE. Though favorable according to Eq. 2 and 3, this barely reduces the induced stress. Then, considering that the SiO<sub>2</sub> is very thin and that the Young's modulus of Cu is approximately that of Si, we recover the conventional limit:

$$\sigma_{Si} \rightarrow (\alpha_{Cu} - \alpha_{Si}) E_{Si} \Delta T, \quad (5)$$

However, using an insulator with a much reduced Young's modulus should lead to an important reduction of the stress. In the limit where  $E_{In}/t_{In}$  is very small, the second term would dominate in Eq. 3 leading to  $\bar{E}_{Cu,In} \sim E_{In}$ . The stress induced in silicon would tend to

$$\sigma_{Si} \rightarrow (\alpha_{Cu} - \alpha_{Si}) E_{In} \Delta T, \quad (6)$$

Considering the specific case of P4VP that has a Young's modulus  $\sim 30$  times smaller than Cu (see Table I), although its CTE is large, the use of P4VP lowers significantly the effective  $\bar{E}_{Cu,In}$  leading to a stress reduced by half.

The previous equations are given for purely elastic materials which is not the case of P4VP. They nevertheless can be used as a simple approximation to compare the insulating material. The use of the electrografted P4VP as insulator should play a key role in the reliability of the interconnections as its mechanical properties are totally different from those of SiO<sub>2</sub> based materials. Table I lists and compares the main properties.

The P4VP also undergoes a glass transition above which its Young's modulus is reduced by a factor of 1,000 to 100,000. In fact, above its glass transition temperature  $T_g$ , the polymer chains possess enough energy to slide against one another and reorganize, thus relaxing the stress. This phenomenon is known as "viscoelastic relaxation". For these reasons, the P4VP polymer could act as a buffer layer and relax the stress between the Cu filling and the surrounding Si, reducing the KOZ size and thus, increasing the integration density in microsystems.

Other studies have been realized to characterize polymer insulated Cu TSVs [9], [11]. In these studies, the SiO<sub>2</sub> dielectric layer was replaced by a parylene or benzocyclobutene (BCB) layer and finite element analysis (FEA) was used to simulate the thermo-mechanical behavior of such TSVs. It led to the conclusion that with the use of parylene to insulate TSVs, stress can be reduced by up to 50% in Cu filled TSVs.

In the following sections, we use Raman spectroscopy to investigate the stress in the Si surrounding P4VP insulated HAR Cu TSVs, and compare it to SiO<sub>2</sub> insulated Cu TSVs.

### III. RAMAN SPECTROSCOPY MEASUREMENT OF SILICON RESIDUAL STRESS

When a photon interacts with matter, an electron-hole pair can be created if the incident photon has a high enough energy. The electron will then relaxes to a lower energy state through radiative transition. In the case of Rayleigh scattering, this lower energy state is the same as the electron's initial state. However, in some cases, a phonon can be generated (Stokes) or absorbed (anti-Stokes). This phonon is caused by lattice vibrations in the system. Raman spectroscopy measures these lattice vibrations, more specifically the optical modes [20], [21].

In the case of Si, where the crystal structure is zinc-blend [22], the optical phonons are excited at the  $\Gamma$  point of the Brillouin zone. The typical Raman spectrum of Si at room temperature displays a first order peak at  $\sim 520 \text{ cm}^{-1}$  and two second order peaks at  $300 \text{ cm}^{-1}$  and  $950 \text{ cm}^{-1}$  [23]. The peak position varies with temperature at a rate between  $-0.02$  to  $-0.03 \text{ cm}^{-1}/^\circ\text{C}$  in the  $300\text{-}600^\circ\text{C}$  range [24]. The first order peak is caused by a single-phonon process and its full width at half maximum is  $\sim 5 \text{ meV}$ . In the absence of stress, it is located at  $520 \text{ cm}^{-1}$  [25], [26] and corresponds to the energy of the optical phonon at  $\Gamma$  ( $\sim 65 \text{ meV}$ ). The second order peaks at  $300 \text{ cm}^{-1}$  and  $950 \text{ cm}^{-1}$  are due to two-phonon processes [23], [26], [27]. In this work, we focus on the first order peak. Stress, whether of mechanical or thermal origin, has an impact on the position of the Raman peaks.

There are two methods to extract information on the Si stress from Raman spectroscopy. The first method allows the full interpretation of the stress components of the experimental values, but it necessitates to calculate the strain tensor elements at various points in the Si using an analytical model or a finite element analysis and to compare the results to the experimental values [28]–[32]. The second method uses a simple and more straightforward method. Although it does not allow the interpretation of the stress components, it is the most often used method in the literature to study and compare the thermomechanical behavior of a TSV [31], [33]. In this method, for the TSV configuration, we assume a biaxial stress [30], [31], [34]. It was shown that the axial stress  $\sigma_z$  is negligible near the surface of the silicon [35]. As the  $473\text{nm}$  excitation photons are absorbed in the first  $\sim 1$  to  $2 \mu\text{m}$  from the surface, it is justifiable to neglect the axial component resulting in the linear relation with the sum of the two in-plane stress normal components  $\sigma_r$  and  $\sigma_\theta$ . In the silicon surrounding TSVs, these components are known to be of comparable magnitude but of opposite signs (exact in Lamé's equations for an infinite volume of silicon). The biaxial stress ( $\sigma_r + \sigma_\theta$ ) is thus expected to be small regardless of the magnitude of the individual components. Using the deformation potentials, the wavenumber difference between the Raman peak of the material with and without stress  $\Delta\omega$  is given by

$$\Delta\omega = \frac{1}{2\omega_0} [pS_{12} + q(S_{11} + S_{12})](\sigma_r + \sigma_\theta). \quad (7)$$

where  $p$ ,  $q$ ,  $S_{11}$  and  $S_{12}$  are material constants, and  $\sigma_r$  and  $\sigma_\theta$ , the radial and tangential stress [30]. Hence, considering accepted values [34] the biaxial stress is given by

$$(\sigma_r + \sigma_\theta) = -500 \times 10^6 \Delta\omega. \quad (8)$$

where  $\Delta\omega$  is given in  $\text{cm}^{-1}$  and the stress in MPa. Note that the Raman peak shifts towards the higher wavenumbers in the case of compressive stress, and towards the lower wavenumbers in the case of tensile stress. Using Eq. 8, the Si stress surrounding the Cu TSV can be estimated using Raman spectroscopy.

### IV. EXPERIMENT

#### A. TSVs Samples Fabrication

In order to compare  $\text{SiO}_2$  insulated TSVs to P4VP insulated TSVs, two series of samples were fabricated using 8-inch  $p$ -doped Si (100) wafers. Both of them followed the fabrication process flow described in Fig. 2.

First, a DRIE Bosch process was used to etch a periodic array of HAR TSVs [36] of  $5 \mu\text{m}$  diameter by  $50 \mu\text{m}$  depths on both wafers. Then, prior to any metallization process, both wafers were prepared using the so-called RCA clean [2]. First, a Standard Clean 1 (SC-1) (a mixture of  $\text{H}_2\text{O}_2$ ,  $\text{NH}_4\text{OH}$  and  $\text{H}_2\text{O}$ ) was performed to remove organic residues and particles from the Si substrate. Then, the sample was immersed in diluted HF to remove the native  $\text{SiO}_2$  of the exposed Si surface. Finally, we did a Standard Clean 2 (SC-2), (a mixture of  $\text{HCl}$ ,  $\text{H}_2\text{O}$  and  $\text{H}_2\text{O}_2$ ) to remove the remaining metal contaminants. This process creates a thin  $\text{SiO}_2$  layer, up to  $\sim 10 \text{ \AA}$  thick [37]. Between each cleaning steps, the wafers were rinsed using DI water.

The HAR TSVs of the first wafer were insulated with electrografted P4VP. The electrografting of P4VP was realized using *aveni's eG<sup>3D</sup> Isolation solutions* [15]. This process was done in a dedicated production tool present at the MiQro Innovation Collaborative Center (C2MI). After the electrografting process, the sample was dried under  $\text{N}_2$  before annealing at  $200^\circ\text{C}$  also under  $\text{N}_2$ . The HAR TSVs of the second wafers were insulated by a thermal  $\text{SiO}_2$  layer grown at  $1,100^\circ\text{C}$ . The resulting TSVs are shown in Fig. 3.

The TSVs were then metallized (Cu diffusion barrier layer and Cu filling) using identical process also in a dedicated production tool presents at C2MI. For both wafers, a conductive NiB barrier layer was deposited by chemical grafting using *aveni's eG<sup>3D</sup> Barrier chemical solutions* [15]. This electroless process created strong chemical bonds between the dielectric (P4VP or  $\text{SiO}_2$ ) and the NiB layer with equivalent barrier properties than TiN [14], [38]. Finally, bottom-up Cu electrografting was realized using the conducting NiB barrier layer as seed layer with *aveni's eG<sup>3D</sup> fill chemical solutions* [15]. A last annealing was realized at  $250^\circ\text{C}$  under  $\text{H}_2/\text{N}_2$  for 20 minutes. At the end of the TSV metallization process, a Cu overburden layer was present on the surface. The Cu overburden was then removed from the Si surface by Chemical and Mechanical Planarization (CMP), using a  $50 \text{ nm}$  diameter colloidal silica with benzotriazole (BTA) as corrosion inhibitor and a R&D slurry.

#### B. Raman Spectroscopy Measurement

The Raman measurements were performed at room temperature using a Horiba system equipped with a modified Olympus BX-41 confocal microscope having a  $0.9 \text{ NA}$

objective 100 $\times$ , a solid-state blue Cobolt 04-01 laser (473.2 nm excitation), and a Synapse Back-Illuminated DeepDepletion 1024  $\times$  256 CCD detector. A focus spot of 0.6  $\mu\text{m}$  in diameter was obtained, giving a spatial resolution of 0.3  $\mu\text{m}$ . The laser power was varied between 10.5 mW and 1.08 mW for the laser power study. For the stress analysis, a value of 1.08 mW was used. The penetration depth of the laser radiation in the Si samples is  $\sim$ 800 nm. The scan lines on both types of sample were realized along the Si (100) crystallographic direction.

## V. MEASUREMENTS AND RESULTS

Fig. 3 presents the two types of TSVs studied after the insulation process with either a) thermal SiO<sub>2</sub> or b) and c) electrografted P4VP. The thermally grown SiO<sub>2</sub> dielectric layer is highly conformal with a thickness ranging from  $\sim$ 110 to 130 nm. Fig. 3 b) and c) show that the walls of the P4VP insulated TSV are grafted with the polymer. The electrografted P4VP follows closely the textured walls of the TSV. This excellent uniformity is due to the electro-initiated mechanism [39] of electrografting process. The top of the TSV wall is covered with  $\sim$ 100 nm of P4VP and the bottom of the TSV is covered with  $\sim$ 80 nm of P4VP, which corresponds to an excellent step coverage of 80% (ratio between the thickness of the insulator on the bottom and the top of the TSV).

At the end of the metallization process (Fig. 4 a), the TSVs are filled without any visible defect and a  $\sim$ 3  $\mu\text{m}$  thick Cu overburden is present at the surface of the samples. The CMP process successfully removed the Cu overburden, leaving the top of the TSV with a smooth Cu surface (Fig. 4 b). A thin black region is visible between the Cu and the Si substrate corresponding to the insulating material. Small scratches are present on the Si surface, and are attributed to the SiO<sub>2</sub> nanoparticles used during the CMP process.

This result attests to the capability of the *avéni* wet metallization process flow to fully metalize HAR TSVs of 5  $\mu\text{m}$  diameter and 50  $\mu\text{m}$  depths as described in the literature [15], [17]. After the CMP process, Raman spectra were taken on the Si substrate to measure the stress in induced silicon.

The first step consisted of determining the laser power to use. The laser used for the Raman measurements can induce local heating and thus shift the Raman peak. This shift cannot be differentiated from the shift induced thermomechanically and must therefore be minimized. The effect of the laser power on the Si Raman peak shift was studied, as presented in Fig. 5.

We can see that as the laser power decreases from 9.02 to 0.101 mW, the Raman peak shifts towards the higher wavenumbers by 0.23  $\text{cm}^{-1}$  corresponding to a temperature increase of  $\sim$ 10 $^{\circ}\text{C}$ . There is no important shift between the two lower laser intensity Si peak positions. Nevertheless, as the laser intensity is decreasing, the Si peak position uncertainty is increasing. For these reasons, the measurements were performed with a laser power of  $\sim$ 1 mW, to limit the thermal contribution of the laser intensity and to limit the Si peak position uncertainty. A laser power of  $\sim$ 1 mW is a common power value used for Si stress investigation [13], [40].

Fig. 6 presents a typical Si Raman spectrum centered at the expected first order Si peak ( $\sim$ 520  $\text{cm}^{-1}$ ). The measurement was taken on the bare Si substrate, far from the TSV, to serve as a

reference. Its precise position was determined using a Lorentzian function fit, with a resolution of  $\sim$ 0.05  $\text{cm}^{-1}$  inferring according to Eq. 8 a stress resolution of  $\sim$ 25 MPa. The Si peak wavenumber shift around the TSV was investigated using this method, for both SiO<sub>2</sub> insulated TSVs and P4VP insulated TSVs. Raman spectra were measured from the edge of the TSVs to the bare Si substrate. For each analyzed TSV, the reference wavenumber  $\omega_0$  was estimated from the average Si peak position far from the TSV where the stress is expected to be zero. Several devices were measured to ensure reproducibility.

Fig. 7 shows that, in the case of the SiO<sub>2</sub> insulated TSVs, the Si Raman peak shifts towards the lower wavenumbers towards the edges of the TSVs. This implies the presence of a tensile stress ( $\Delta\omega_0 < 0$ ) in the immediate vicinity of the TSV. According to equation (8), the corresponding stress was calculated for each position and is presented in Fig. 8. Note that for greater clarity the measurements of left side of the TSV are here folded onto those of the right side. To further the analysis, we also plot as grey area the 95% prediction interval considering the measurements as a sample of duplicate measurements of the zero-stress background. The interval was calculated using the data collected 3  $\mu\text{m}$  away from the TSVs edge, where the silicon is supposed to be stress free. Thus, the distribution of the data is representative of the statistical variation of the zero-stress background.

As expected, these measurements show an increase in the tensile stress as we move closer to the TSVs up to a maximum value of 180 MPa at the edges, over the 95% prediction interval. The distance over which the stress in Si relaxes ( $\sim$ 1.5  $\mu\text{m}$ ) is in the same range than that of HAR TSVs insulated using a polymeric compound, where the stress is estimated using the similar Eq. 8 [33]. As the spatial resolution of the system is  $\sim$ 0.3  $\mu\text{m}$ , it is difficult to measure with precision the evolution of the stress within 1.5  $\mu\text{m}$ . Moreover, the Raman signal becomes noisy closer to the Si/TSV interface due to the loss of the laser intensity in the Si. Interpretation of the stress values close to the TSV edge must be done with caution.

For SiO<sub>2</sub> insulated TSVs, the residual Si stress could have three possible origins. At the end of the metallization process, the last annealing (250 $^{\circ}\text{C}$ ) expands the Cu resulting in a compressive stress in the Si due to their CTE mismatch. Above 200 $^{\circ}\text{C}$ , Cu may develop plasticity reducing the stress in the TSV [7]. When cooling down, and back at room temperature, the contraction of the Cu would cause a tensile stress in the surrounding Si. Another source of the residual Si stress could be the thermal oxidation process of the TSV hole that forms the insulator. It could be due to the difference of CTE between SiO<sub>2</sub> and Si for the same reason as above. A last source is discussed in [12] where the authors gave clear evidence that residual Si stress existing around a metalized TSV is not only due to CTE mismatch between Cu and Si but also from a pre-existing stress present before the TSV Cu filling. They suspect this pre-existing stress to be originating from the thermal growth technique of the oxide insulator.

As shown in Fig. 9, the case of P4VP is significantly different. Only few measurement points, mainly close to the TSVs, stand out of what could be considered as background. We clearly see that all but 6 of the 65 measurements are inside the

95% prediction interval and thus, could be explained by the statistical dispersion of the measurements around their mean value. Moreover, the three highest measurements are located within 1.5  $\mu\text{m}$  from to the TSV edge, it is likely that they show the presence of a small stress of approximately 40 MPa. For the reasons already discussed above, such low stress close to the TSV edge must be interpreted with caution.

## VI. DISCUSSION

We conclude that, if existing, the stress close to the P4VP insulated TSV edge is considerably lower compared to  $\text{SiO}_2$  insulated TSVs. This observation is of great interest, as it clearly shows that with the use of the electrografted P4VP, the residual Si stress at the edges of the TSV is dramatically reduced compared to  $\text{SiO}_2$  insulated TSVs.

We will now discuss main phenomena leading to the reduction of the residual Si stress with the use of P4VP relating to two of its properties: 1) low Young's modulus and 2) viscoelastic relaxation.

We already mentioned that by considering the material properties of  $\text{SiO}_2$  and P4VP in Table I and the simple model of Eq. 1, we can show that the residual stress expected in P4VP insulated TSVs is reduced to half of  $\text{SiO}_2$  case. Furthermore, as the electrografting process is realized at room temperature, we expect the zero-stress temperature to be rather low (at least before the final anneal) and thus  $\Delta T$  at room temperature. We leave the discussion on the impact of the final anneal at 250°C to the next paragraph. This case of thermal  $\text{SiO}_2$  formed above 400°C is quite opposite. A quantitative agreement is likely out of reach for many reasons. As mentioned, the mechanical properties of polymers are rather peculiar. Also, their properties in confined thin films (200 nm in this case) are certainly not those of the same bulk material. Their study and characterization in these conditions are very complex [41]. Nevertheless, we believe that the large Young's modulus ratio between Si and polymers (typically more than one order of magnitude) is a dominant contribution.

The metallization process of the TSV includes a 250°C annealing step after the filling with Cu. This temperature is above the expected glass transition temperature of P4VP below 200°C, relatively close to its bulk value [42], [43]. Our hypothesis is that  $T_g$  is reached during the final annealing of the TSV. Even if the polymer is confined between the Cu filling and the Si substrate, the polymer's chains can reconfigure between reticulation points: there is a viscoelastic relaxation of the stress through self-reorganization of the P4VP chains. The polymer would therefore act as a buffer layer and reconfigure itself to absorb the stress. After cool down, once below  $T_g$ , the mechanisms that lead to stress in TSV come into play again. This occurring at a lower temperature than that common to  $\text{SiO}_2$  process, we expect the residual stress to be lower and further reduced by the low Young's modulus of P4VP.

## VII. CONCLUSION

We have fabricated two series of HAR TSV of identical geometry (5  $\mu\text{m}$  diameter by 50  $\mu\text{m}$  deep), one with polymer (P4VP) as insulator and the other with a thermal  $\text{SiO}_2$  as insulator to serve as reference. All process steps are identical except for those forming the insulator layer. We used Raman

spectroscopy to make the first measurements of the residual stress in Si around P4VP insulated HAR TSVs. While we measured stress around  $\text{SiO}_2$  insulated TSVs (>100 MPa), we were not able to measure any significant stress around P4VP. We estimate that if present, the residual stress in the latter case is below 40 MPa. Complementary Finite Element Analysis will be realized in the further experiments to give a more accurate interpretation of the measurements results. We propose that this drastic reduction is due to the very low Young's modulus of P4VP and speculate on the possible role of a low temperature glass transition and viscoelastic properties to further reduce stress. So far, it has not been possible to properly measure the glass transition temperature of P4VP and to characterize its material properties above it.

We demonstrated that the use of a polymer as insulator, P4VP in this case, nearly eliminates the residual stress in Si around HAR TSVs. We further show that the full wet metallization process flow based on electrografting to form the P4VP insulator is perfectly suited for low stress HAR TSV.

These results are promising as the process could mitigate present technical limitations in terms of thermomechanical reliability and integration density of a microsystem. In particular, we believe that the KOZ around TSV due to the thermomechanical stress only could be strongly reduced.

Finally, the electrografted P4VP layer could be used in a wide range of applications confronted to thermo-mechanical issues and where highly conformal layer is needed.

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**Table:**

TABLE I  
COMPARISON OF MECHANICAL PROPERTIES BETWEEN P4VP [16],  
SiO<sub>2</sub> BASED MATERIALS AND COPPER

Parameters	SiO <sub>2</sub>	P4VP[16]	Cu
Mechanical behavior	Elastic	Viscoelastic	Elastic
$E @ T = 20\text{ }^{\circ}\text{C}$	75-120 GPa	3.4 GPa	120 GPa
$E @ T > T_{g, P4VP}$		$100-1 \times 10^{-3}$ GPa	
CTE	0.5 ppm/ $^{\circ}\text{C}$	30 ppm/ $^{\circ}\text{C}$	17.7 ppm/ $^{\circ}\text{C}$
Residual Stress @ 200nm	100 MPa	10 MPa	

Figures:

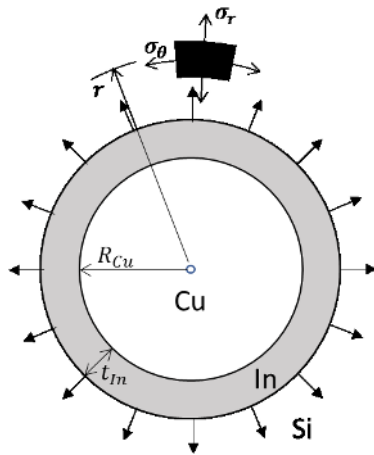


Fig. 1. Definition of the axes, stress components and geometrical parameters.

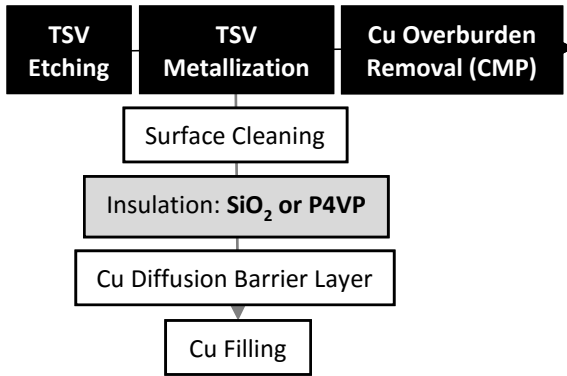


Fig. 2. Sample fabrication process flow prior to Raman spectroscopy measurements.

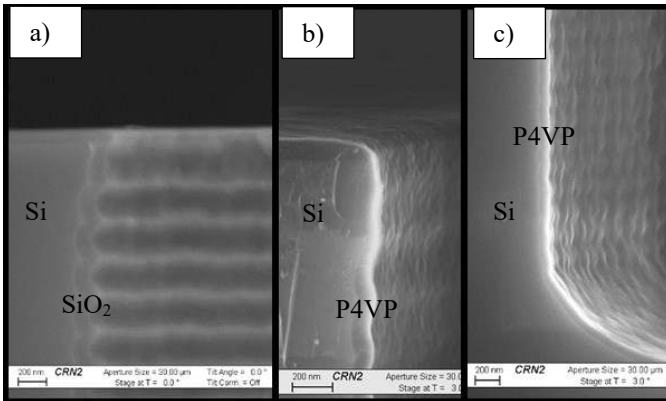


Fig. 3. SEM cross section of TSVs with insulator material: a) SiO<sub>2</sub> and b-c) P4VP. Top b) and bottom c) of the TSV with P4VP.

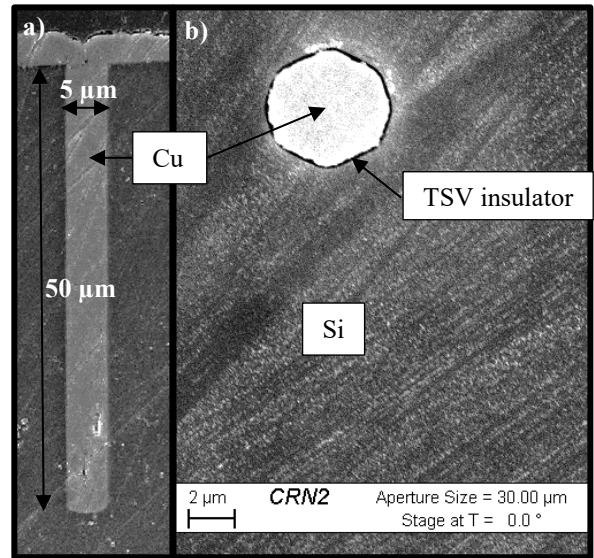


Fig. 4. a), cross section SEM picture of a 5 μm diameter and 50 μm depth TSV after the wet metallization process using P4VP as an insulator. b), top view SEM picture of a 5 μm diameter and 50 μm depth TSV after Cu overburden CMP.

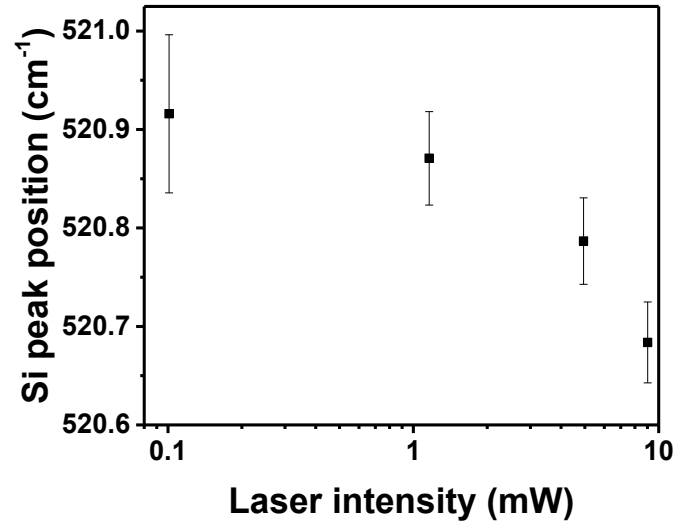


Fig. 5. Si peak position as a function of laser power. Measures taken after 3s exposition to the laser.

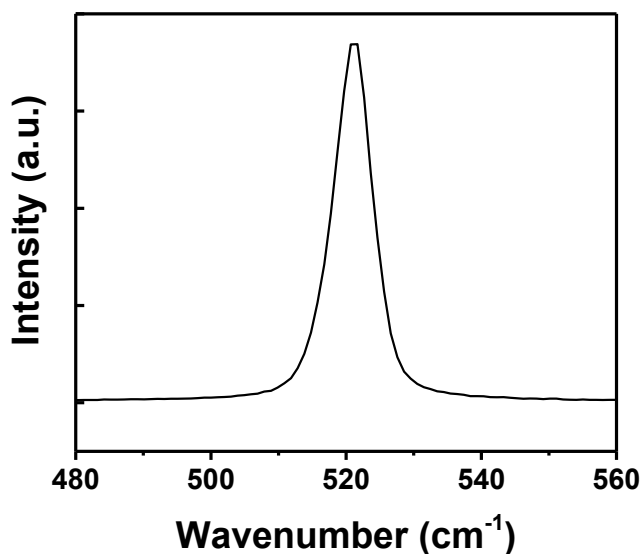


Fig. 6. Typical Raman spectrum obtained on the Si sample.

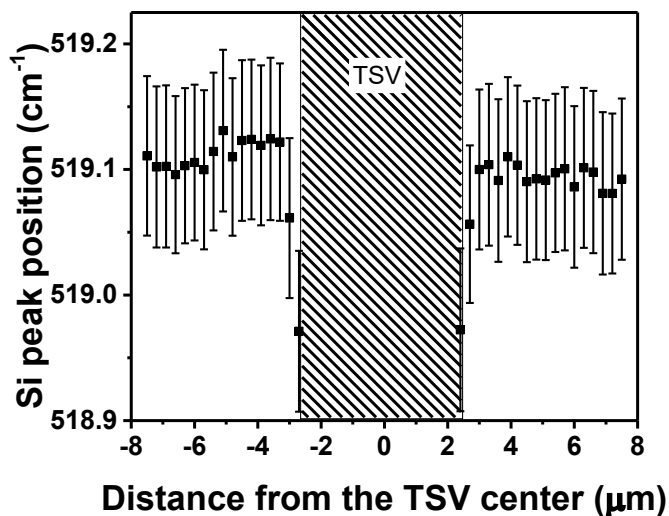


Fig. 7. Typical evolution of the Si peak shift around a SiO<sub>2</sub> insulated TSV.

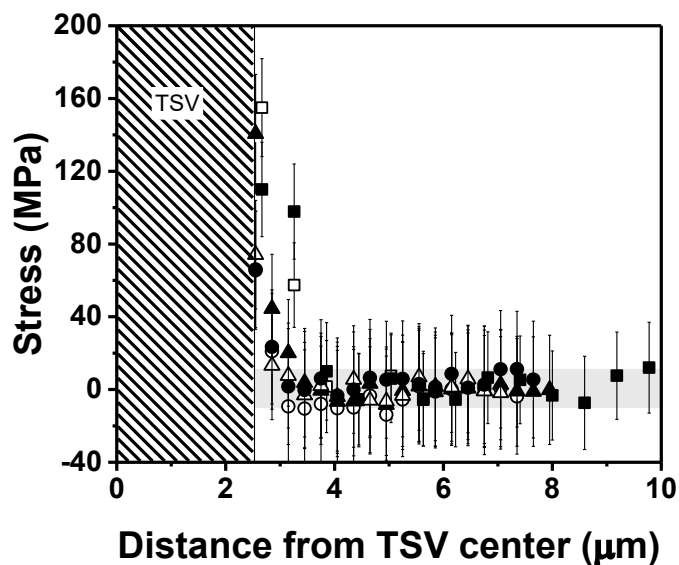


Fig. 8. Residual Si stress ( $\sigma_r + \sigma_\theta$ ) measurements around SiO<sub>2</sub> insulated TSV of 5  $\mu\text{m}$  diameter. Square, circle and triangle symbols are used for three different TSVs. Empty and filled symbols are used to differentiate measurements taken at two opposite sides of the TSV. The horizontal grey area defines the 95 % prediction interval.

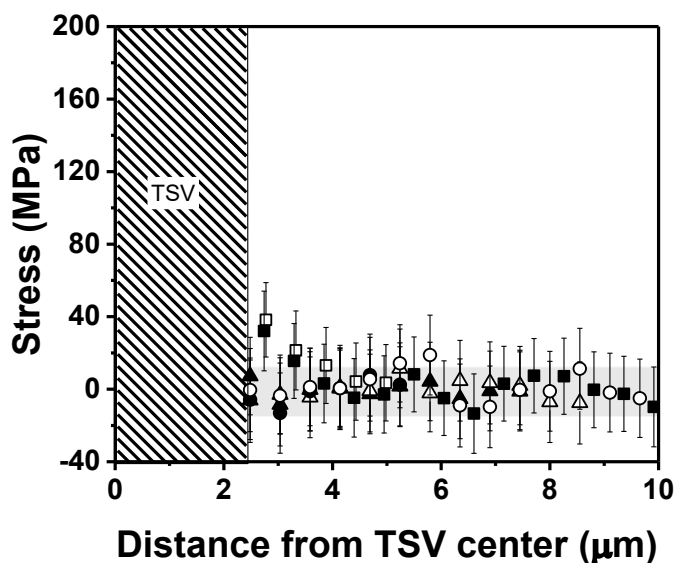


Fig. 9. Residual Si stress ( $\sigma_r + \sigma_\theta$ ) measurement around electrografted P4VP insulated 5  $\mu\text{m}$  diameter TSVs. Square, circle and triangle symbols are used for three different TSVs. Empty and filled symbols are used to differentiate measurements taken at two opposite edges of a TSV. The horizontal grey area defines the 95 % prediction interval.