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Monte Carlo Analysis of the dynamic behavior of III-V MOSFETs for Low-Noise RF Applications

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Abstract:

III-V Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with a high- κ dielectric gate stack are investigated as a possible route to enhance the performance of either microwave or logic circuits with low supply voltage (V_{DD}). The intrinsic performance of III-V MOSFETs in both static and dynamic regimes under low V_{DD} is estimated using device Monte Carlo simulation. The characteristics of a Bulk-like and XOI-like III-V MOSFETs are quantitatively assessed and compared in terms of DC transconductance, high frequency performance and noise behavior. Finally, the comparison with Si-based devices shows the potential of III-V nano-MOSFET architectures for high-frequency and low noise application under low operating power.

Keywords:

Semiconductor Device Modelling, III-V materials, Dynamic Monte Carlo simulation, Ballistic transport, RF performance, noise figure, low supply voltage.

I. INTRODUCTION

In the last decade, the radiofrequency (RF) front-end circuits have been widely developed to produce highly integrated digital RF communication terminals using Silicon-based technologies [1]. Wireless applications require more and more high-speed and autonomous capabilities for ambient intelligent functions [2][3]. Circuits able to reach the GHz range while consuming about 1mW will allow increasing drastically the autonomy of communicating systems. The key issue of current Si technology is the limitation of the optimal frequency-performance/power-consumption trade-off resulting from the poor carrier mobility and relatively large supply voltage required for circuit operation [4]. In contrast, III-V-based technology is very attractive in the multi-gigahertz range. A possible approach is the use of III-V HEMT (High Electron Mobility Transistor) [5][6] which, with InGaAs channel material, have demonstrated not only very high microwave performance but also a good potential for logic applications [7][8]. HEMTs are also widely used to design Low Noise Amplifiers (LNA) [9][10][11] [12] [13][14] for very sensitive receivers. However, due to high gate leakage current inducing high DC power consumption, they tend to reach their scaling limits in terms of gate length and layer structure. Additionally, the HEMT footprint size significantly limits the potential of this device in terms of large scale integration (VLSI) circuits [15]. MOS topologies with high- κ dielectric gate stack compatible with III-V channel [16] are expected to improve the electrostatic gate control, to drastically reduce the gate leakage [17] and to enhance the device scaling potential [18]. Very promising

microwave and noise performance for long-channel devices (1 μm) has been demonstrated by the pioneering work of Ref.[19] [20].

By using an ensemble Monte Carlo simulation, the present work aims at assessing the ability of III-V MOSFETs to deliver low noise RF performance under low supply voltage of 0.2 V. The MC method allows estimating accurately both the RF performance [21] and the noise behavior as it naturally accounts for the instantaneous current fluctuations directly related to the electron velocity fluctuations induced by microscopic scattering mechanisms [22]. This powerful tool can be used to investigate the microscopic origins of noise sources and their correlations [23].

This type of semi-classical Monte Carlo model ignores the quantum effects occurring at the nanoscale [24], but it has the strong advantage of being able to include the realistic description of both all relevant scattering mechanisms and the time evolution of the system. This is not yet possible with quantum simulators [25]. Besides, the ability of the Monte Carlo technique to provide useful information on the small signal and noise behavior in nano-MOSFET has been demonstrated in previous works [22][27][30][31][32][34][35][36][38][42]. Such investigations have already been performed for Si MOSFETs and III-V HEMTs but not for III-V MOSFETs yet.

Hence, here we propose a numerical assessment of design optimization of III-V-based MOSFET in terms of (i) intrinsic high frequency behavior, through Y parameters, cutoff frequency f_T and small-signal equivalent circuit (SSEC), extracted without considering gate access resistance and fringing capacitances and (ii) noise properties, including NF_{min} , F_{opt} , R_n and G_a . These device parameters are the important factors of merit of microwave devices for low-noise applications. The results obtained for III-V MOSFETs are compared with that obtained for Si-based transistors.

II. SIMULATED DEVICES

The simulated reference device is a 50 nm-long conventional bulk-like MOSFET, schematized in Fig. 1, with $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel and self-aligned $\text{Al}_2\text{O}_3/\text{TaN}$ gate stack. The performance of this type of device is known to be affected by roughness scattering at channel/dielectric interface, interface traps and doping impurities in the channel. The alternative structure COMB-MOS is inspired by a combination of the Thin-Body III-V On Insulator (III-VOI or XOI) structure and HEMT structure with a wide bandgap III-V spacer between the channel and the gate dielectric. With an appropriate gate stack design, this structure has been shown to provide improved transport properties and good gate charge control efficiency [26]. These III-V structures are benchmarked here with their Si-based BULK-MOSFET counterpart. This simulated Si device has exactly the same structure as the ‘‘Bulk MOS’’ presented in Fig. 1, but the InGaAs alloy is replaced by Silicon. All devices were designed with the same equivalent oxide thickness (EOT). In the case of COMB-MOS structure the high bandgap spacer is assumed to play the role of an additional insulating layer with negligible carrier charge density. It is thus included in the insulator stack for the EOT determination.

III. PHYSICAL MODELS

The MC model used in this work is a semi-classical ensemble simulator self-consistently coupled with a 2-D Poisson solver [28]. For Silicon, the conduction band is described through an analytic non-parabolic model for the six ellipsoidal Δ valleys located along the [100] directions at 85% of the Brillouin zone edge. All details of the band structure and the scattering parameters for acoustic phonon, intervalley phonon, ionized impurity and oxide interface roughness scattering may be found in [29]. For InGaAs and InAlAs, Γ , L and X valleys are considered within a spherical non-parabolic approximation. Standard band structure and scattering parameters are used [27] [30] including acoustic phonon, polar and

non-polar optical phonon, intervalley phonon, surface roughness and impurity scattering. Surface roughness scattering is treated with the widely used technique for 3D electron gas which consists of an empirical combination of diffusive and specular reflections at oxide interface. To assess an ideal case, the roughness parameters of highly mature Si/SiO₂ interface are considered also for III-V/Oxide interface. Degeneracy effects and quantum corrections were not taken into account. In a previous work [30], the current MC model and parasitic series resistance have been carefully calibrated on static experimental characteristics of III-V FET devices. In this work, we focus on the intrinsic dynamic performance of the transistor. The interface trap effects, which are basically slow parasitic phenomena, were neglected likely leading to slight overestimation of ballisticity. All simulations were performed at room temperature. Among the numerous advantages of semi-classical MC simulation, the transient analysis of the device allows advanced investigation of the intrinsic frequency response, which is useful to benchmark the different architectures. However, it should be mentioned that the experimental measurement of RF and noise parameters are strongly degraded by external parasitic elements due to Ohmic contacts, external circuit elements and packaging. In this respect, we assume that the conclusions on the comparison of devices are not affected by the fact that parasitics are neglected.

IV. TRANSIENT PARAMETERS

The instantaneous terminal currents were calculated on the basis of the Ramo-Shockley theorem for time-varying terminal potentials using the technique described in [32], i.e.

$$I_{j_tot}(t) = -\sum_{k=1}^N q \mathbf{v}_k(t) \cdot \nabla \varphi(\mathbf{r}_k, t) + C_{ij} \frac{\Delta V_i(t)}{\Delta t}. \quad (1)$$

In this approach, the transient current at electrode j is decomposed into two contributions. The first one results from the movement of all charged particles within the device, where N is the number of particles, $\mathbf{v}_k(t)$ is the velocity of k^{th} particle at time t at position \mathbf{r}_k , $\varphi(\mathbf{r}_k, t)$ is the space-dependent potential which is obtained from the solution of the Laplace equation when 1V is applied on electrode k . The MC method is very appropriate to determine the two previous quantities at each time step. The second part in (1) is due to the time-varying electrode potentials $\Delta V_i(t)$ via the capacitive inter-electrode coupling C_{ij} . More details on the transient current calculation can be found elsewhere [32][35].

Complex frequency-dependent two-port admittance parameters $Y_{ij}(j\omega)$ can be evaluated by Fourier Transform (FT) of the transient currents after application of a perturbation step on a terminal voltage. For a given DC bias, a steady-state condition is first established by running the simulation for a time long enough to reach a steady state regime with average drain current $I_D(0)$. Then small step perturbations ΔV_j are applied successively to the gate ($\Delta V_1 = 0.1$ V) and drain ($\Delta V_2 = 0.2$ V) electrodes and the transient currents $I_i(t)$ are recorded as a function of time. $I_i(\infty)$ is the final steady-state current after the step perturbation. Finally, the parameters $Y_{ij}(j\omega)$ can be computed as

$$Y_{ij}(j\omega) = \frac{I_i(\infty) - I_i(0)}{\Delta V_j} + \frac{j\omega}{\Delta V_j} \text{FT}\{I_i(t) - I_i(\infty)\}. \quad (2)$$

Each simulation has been performed during more than 1 000 000 time steps of 0.1 fs each to reach a wide frequency range, with about 100 000 particles. The use of the Ramo-Shockley theorem for the determination of terminal currents gives accurate noise results weakly dependent of the number of simulated particles.

To characterize the frequency response, the current gain $|h_{21}|$ in common-source configuration is calculated as

$$h_{21}(\omega) = \frac{|Y_{21}(j\omega)|}{|Y_{11}(j\omega)|}. \quad (3)$$

The intrinsic cut-off frequency f_T is defined as the frequency for which $|h_{21}| = 1$.

V. RESULTS AND DISCUSSION

a) DC characteristics

The intrinsic transconductance G_m is an important parameter to be optimized for microwave performance of transistors. The intrinsic G_m is plotted in figure 2 as a function of drain current at low V_{DS} (0.2 V), i.e. in quasi linear regime. All structures have almost the same performance at low current level. However, for drain currents higher than 50 A/m, the performance is strongly improved in III-V-based devices, especially in COMB-MOS structure. G_m reaches 0.35 mS/ μm at 110 $\mu\text{A}/\mu\text{m}$ for Si-based BULK-MOS, 1.7 mS/ μm at 700 $\mu\text{A}/\mu\text{m}$ for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -based BULK-MOS and 4.0 mS/ μm at 2000 $\mu\text{A}/\mu\text{m}$ for COMB-MOS. Due to strong influence of interface roughness scattering at high effective field, G_m decreases at high current level. The high drive current and transconductance reached at low V_{DS} in COMB-MOS is actually the consequence of quasi-ballistic transport regime. To quantify the contribution of ballistic and/or quasi-ballistic effect to the current, we have extracted the number of scattering events N_{scatt} experienced by each carrier crossing the gated region of the channel (see inset of figure 2). This technique has been described in Ref [33]. The fraction of fully ballistic electrons at the drain-end of the channel is limited to 3% for BULK-MOS (almost the same for both Si- and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -based structures) while it reaches 60% for COMB-MOS. Thanks to quasi ballistic behavior, the III-V COMB-MOS structure delivers high performance even at low V_{DS} . For the AC and noise analysis presented below, all selected DC biases correspond to the maximum value of G_m at $V_{DS} = 0.2$ V.

b) AC responses

To assess the dynamic behavior of devices, the Y parameters are extracted directly from the transient current of the gate and drain terminals. The real parts of Y_{21} and Y_{22} are plotted in figure 3 over a wide frequency range 10 GHz – 1 THz. At low frequency, they represent the transconductance G_m and the output conductance G_D , respectively. We can see that they do not vary as a function of the frequency below 100 GHz. Actually, the dynamic performance can be analytically predicted from a simple small-signal equivalent circuit for frequencies below 100 GHz [34] and the corresponding values of the small signal elements are reported in Table 1. The use of such equivalent circuit for frequencies higher than 200 GHz is questionable because of non-quasi-static-effects which modify the evolution of Y_{21} and Y_{22} . The G_m values at low frequency (< 100 GHz) match well those obtained in DC regime. A significant enhancement is observed in COMB-MOS with respect to other devices. High G_m values have a direct impact on the current gain as well as the cutoff frequency f_T . However, under low supply voltage ($V_{DS} = 0.2$ V) the devices operate in the linear regime, i.e. with high output conductance G_D , which is conflicting with high frequency performance, namely the maximum frequency of oscillation f_{max} . Moreover, short channel effects, likely to occur particularly in structures with low channel doping, tend to reinforce this limitation. Indeed, a large value of G_D increases the sensitivity to parasitic elements, in particular to contact resistances. Nevertheless, even if the voltage gain G_m/G_D in open circuit configuration is not better than in Si device, the power gain, proportional to G_m^2/G_D , is much higher thanks to very high G_m . This analysis is summarized in Table 1.

The resulting current gain performance is shown in Figure 4-a. III-V structures, particularly COMB-MOS, exhibit much better high frequency behavior than their Si counterpart thanks to higher current gain achieved in a wide frequency range.

The cutoff frequency f_T can be extracted directly from the crossing point of the computed $|h_{21}(f)|$ curve with the 0dB axis. Experimentally, the current gain cannot be measured at very high frequency. Hence, experimental f_T is evaluated by extrapolating the low frequency gain with a slope of 20 dB per decade. As seen in Table 2, this extrapolation method applied to the computed $h_{21}(f)$ provides results significantly different from that extracted directly, especially in the case of very high values of f_T as in COMB-MOS structure. Indeed, for frequency in the order of magnitude of, or higher than, the characteristic rates of electron-phonon scattering (THz), non-stationary effects are predominant and the method based on the extrapolation of the quasi-static data is actually questionable.

The scalability of RF performance of COMB-MOS is assessed in figure 4-b. The classical (quasi-static) $1/L_G$ trend corresponds to the extrapolated value while the accurate direct extraction predict a much slower (almost linear) variation against the gate length L_G , which results in an f_T limited to about 1 THz at $L_G = 20$ nm.

c) Noise behavior

In this section, we analyze the noise behavior in the frequency range 10 GHz-200 GHz, in which the non-stationary effects are not yet predominant.

A noisy two-port device in common source configuration may be represented by means of the intrinsic noiseless device together with two correlated noise current generators, one at the input (gate) and the other at the output (drain) of the device [22]. These noise sources are characterized by the power spectral densities (PSD) of current fluctuations. The noiseless device is represented by the Y parameters. We calculated the equivalent noise sources together with their correlation through the analysis of the current fluctuations at the gate S_G and drain S_D terminals and their correlation S_{DG} . Here the sample frequency f_{sample} is 10^4 THz.

The high-frequency intrinsic noise parameters were calculated using the normalized Pucel parameter P , R and C [37]. They characterize the noise behavior weighted by the dynamic response of the transistor and are defined as [23]

$$P = \frac{S_D}{4k_B T |Y_{21}|}, \quad R = \frac{S_G |Y_{21}|}{4k_B T |Y_{11}|^2}, \quad C = \frac{|S_{DG}|}{\sqrt{S_D S_G}}. \quad (4)$$

P , R and C are bias-dependent and nearly frequency-independent in the frequency range for which the noise parameters have been extracted, that is, lower than 200 GHz)

Finally, the four noise parameters i.e. the noise resistance R_n , the optimum input reflection coefficient Γ_{opt} , the minimum noise figure NF_{min} and the associated available power gain G_a in minimum noise matching conditions could be estimated using the following formula [38][39]:

$$\begin{aligned} R_n &= P/G_m \\ \Gamma_{opt} &= \frac{1 - Z_o Y_{opt}}{1 + Z_o Y_{opt}}, \quad \text{with } Z_o = 50 \Omega \\ Y_{opt} &= G_{opt} + j \cdot B_{opt} \\ &= \omega (C_{GS} + C_{GD}) (C \sqrt{R/P} - 1) + j \cdot \omega (C_{GS} + C_{GD}) \sqrt{R/P} \sqrt{1 - C^2} \\ NF_{min} &= 1 + 2 \cdot \frac{f}{f_T} \sqrt{P \cdot R (1 - C^2)} \\ G_{ass} &= \frac{\Re(Y_{opt})}{\Re\left(Y_{22} - \frac{Y_{21} Y_{12}}{Y_{opt} + Y_{11}}\right)} \left| \frac{Y_{21}}{Y_{opt} + Y_{11}} \right|^2, \end{aligned} \quad (5)$$

where Y_{opt} is the parallel optimum matching admittance for satisfying minimum noise conditions. It is expressed in terms of Pucel parameter and small-signal equivalent circuit elements. In this work, Γ_{opt} was calculated considering a characteristic impedance of 50 Ω . Once the minimum noise matching conditions are met, the input reflection coefficient is equal to Γ_{opt} . The gate capacitance components C_{GS} and C_{GD} were extracted at 20 GHz through the Y parameters.

The power spectral densities (PSD) of current fluctuations in gate and drain terminals are plotted in figure 5. The PSD of drain current fluctuations S_D is almost independent of frequency, which corresponds to a "white" thermal noise source due to the carrier velocity fluctuations in the channel. This kind of noise is more important in COMB-MOS structure and much lower in Si device. In fact, S_D is proportional to G_m even in the linear regime [40], which is strongly related to the ballistic transport behavior. The noise source induced in the gate S_G is related to the intrinsic capacitance in the semiconductor, i.e. to the charge density fluctuations in the channel. This type of noise is higher in Si MOS-BULK than in III-V devices. The density of states (DOS) is about 150 times greater in Si than in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ devices, which may generate more charge density fluctuations in the channel. At 20GHz, S_G of Si device is almost 15 times higher than S_G of both InGaAs devices. A transistor can be considered as a distributed RC network consisting in a distributed gate capacitance and distributed resistance along the channel. This leads to a correlation S_{DG} between the two noise sources S_D and S_G . This correlation is stronger in COMB-MOS structure than in BULK-like devices. With the same gate capacitance, the less resistive the channel is, the stronger the correlation is. It is a consequence of the higher fraction of quasi-ballistic transport in InGaAs, which makes the scattering mechanisms unable to break fully the correlation between these two noise sources.

The noise resistance R_n and the optimum input reflection coefficient Γ_{opt} are plotted in figure 6. In the frequency range, R_n varies slightly as a function of frequency (see figure 6-a). This parameter determines the amount of which the actual noise figure will differ from NF_{min} in case of mismatching (that is $\Gamma_s \neq \Gamma_{opt}$) and can be considered as a sensitivity gauge of the difference between input admittance and its optimum value [41]. In III-V BULK-MOS R_n is about 155 Ω at 20 GHz, which is in the same order of magnitude as what is measured in SOI transistors. In Si BULK-MOS, R_n is equal to 900 Ω at 20 GHz, i.e. the optimum matching conditions of noise are thus very difficult to achieve. This value is significantly reduced in COMB-MOS: 55 Ω at 20 GHz, which is comparable to that reported in a HEMT structure [42]. Figure 6-b shows the magnitude and phase variation of Γ_{opt} as a function of the frequency. For $f < 100$ GHz, $|\Gamma_{opt}|$ and $\arg(\Gamma_{opt})$ are close to unity and 0° , respectively. In a range of a few tens GHz, they vary almost linearly with frequency as predicted by the model proposed by Pospieszalski [43]. Furthermore, when the magnitude of Γ_{opt} is close to the unity, the low loss matching condition is very difficult to reach. COMB-MOS and Si BULK-MOS are also promising from this point of view.

The noise figure NF quantifies the noise added by the device itself. NF and associated transducer power gain in the minimum noise matching conditions are shown in figure 7. The performance is compared with that reported in Ref.[42][37] where a HEMT structure was studied numerically and experimentally. The best performance is obtained in COMB-MOS with $NF_{min} = 0.2$ dB and $G_a = 15$ dB at 20 GHz for an intrinsic DC drain current I_D of 2090 $\mu\text{A}/\mu\text{m}$. In the III-V BULK-MOS $NF_{min} = 0.3$ dB and $G_a = 8.8$ dB at 20 GHz for $I_D = 700$ $\mu\text{A}/\mu\text{m}$, respectively. This noise performance is dramatically less in Si BULK-MOS: NF_{min} is significantly higher (2 dB) and the bandwidth of transducer power gain is strongly reduced in this matching conditions, G_a is only 4 dB at 20 GHz for $I_D = 110$ $\mu\text{A}/\mu\text{m}$. It should be mentioned that

these poor performance for Si-device are achieved at low V_{DS} and could be improved at nominal power supply of 1.2 V but at the cost of a strong increase of the power consumption. All these noise performances are reported in Table 2 together with results from experiments [45] and from other numerical investigations on several FET architectures: HEMT [42][38], LAC (Laterally Asymmetric Channel) [44] and FDSOI (Fully depleted SOI) [46]. The comparison with results from the literature is not obvious since all devices do not operate at the same bias point. Nevertheless, III-V MOSFETs exhibit significantly better RF and noise figure than other MOS architecture designed to achieve low noise performance. The performance of COMB-MOS is comparable to that of a HEMT with 100 nm long gate ($NF_{min} = 0.4$ dB and $G_a = 18$ dB at 20 GHz).

VI. CONCLUSION

In this work, intrinsic DC and AC performance of different structures of III-V MOSFETs have been investigated using an Ensemble Monte Carlo simulation. III-V devices have been benchmarked against their silicon counterparts. The combination of high mobility III-V materials, MOS insulated gate topology with enhancement mode and III-VOS (XOI) architecture design leads to very good intrinsic DC performance and excellent dynamic performance at low V_{DS} . Besides, state-of-the-art noise performance in quasi-ballistic III-V devices makes the optimum matching condition of noise more easily fulfilled. These properties may be a strong advantage for low power and low noise analog applications.

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Figure captions:

Figure. 1. Cross section of the two III-V MOSFET structures under investigation (nid: non intentionally doped), with $L_G = 50$ nm et $T_{OX} = 8$ nm.

Figure. 2. Comparison between $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and Si MOSFETs: Intrinsic transconductance G_m as function of intrinsic drain current at $V_{DS} = 0.2$ V. Inset: fraction of electrons crossing the channel as a function of the number of scattering events. DC bias corresponds to maximum of G_m .

Figure. 3. Calculated real part of admittance parameters Y_{21} and Y_{22} as a function of frequency at the chosen DC operating point.

Figure. 4. a): Current gain in common-source configuration as a function of frequency. b) Cut-off frequency f_T for COMB-MOS, directly extracted from (a) or obtained from the extrapolation method, as a function of gate length L_G . Linear and $1/L_G$ trends are also shown.

Figure. 5. Spectral densities of current fluctuations and their cross-correlation as a function of frequency at the chosen DC biases.

Figure. 6. a) Noise resistance and b) Magnitude and phase of optimum input reflection coefficient as function of frequency at the DC bias which corresponds to maximum of G_m at $V_{DS} = 0.2$ V.

Figure. 7. a) Minimum noise figure NF_{min} (in double scale) and b) The available associated power gain G_a as a function of the frequency at the DC bias which corresponds to maximum of G_m at $V_{DS} = 0.2$ V. Comparison with III-V HEMT from [34].

Tables:

SSEC @ 20 GHz	MOS-Bulk <i>InGaAs</i>	MOS-COMB <i>InGaAs</i>	MOS-Bulk <i>Si</i>
C_{GS} (pF/m)	360	380	369
C_{GD} (pF/m)	180	160	180
C_{DS} (pF/m)	160	120	89
G_m (S/m)	1703	4137	328
G_d (S/m)	1047	1580	126
R_i (Ω .m)	0,0022	0,0014	0,0027
τ (ps)	1,5	0,85	1,6

G_m/G_d	1.6	2.6	2.6
G_m^2/G_d	$\times 3.3$	$\times 12.7$	Rèf.

Table. 1. Extracted G_m , G_d and their ratio at 20 GHz.

		L_G (nm)	f_T (GHz) Direct	f_T (GHz) Extrap.	P	R	C	NF_{min} (dB)	G_a (dB)
Si (Bulk)	This work	50	100	100	3.3	0.6	0.08	2.0@20 GHz	4.0
In _{0.53} Ga _{0.47} As (Bulk)	This work	50	500	550	2.7	0.3	0.2	0.3@20 GHz	8.8
In _{0.53} Ga _{0.47} As (COMB)	This work	50	750	1250	2.7	0.5	0.3	0.2@20 GHz	15.0
Si-Bulk MOSFET	Exp [45]	65		210				1.5@20 GHz	14.5

Si-LAC MOSFET	Simul. [44]	100						0.4@12GHz	
HEMT	Exp./Simul. [37][42]	100		260				0.4@20GHz	18
FDSOI	Simul.[46]	250						2.2@16GHz	

Table. 2. Intrinsic AC and noise performance.