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► **To cite this version:**

Youcef A. Bioud, Abderraouf Boucherif, Etienne Paradis, Dominique Drouin, Richard Arès. Defect-free, heteroepitaxy through electrochemical etching of germanium for multijunction solar cells applications. Porous Semiconductors - Science and Technology (PSST) and related Conferences 2018, Mar 2018, La grande Motte, France. hal-01908833

HAL Id: hal-01908833

<https://hal.science/hal-01908833v1>

Submitted on 30 Oct 2018

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DEFECT-FREE, HETERO-EPITAXY THROUGH ELECTROCHEMICAL ETCHING OF GERMANIUM FOR MULTI-JUNCTION SOLAR CELLS APPLICATIONS

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SUMMARY

A low-cost method to reduce the threading dislocations density (TDD) in relaxed germanium (Ge) epilayers grown on silicon (Si) substrates is presented. Ge/Si substrate was treated with post epitaxial process to create a region with a high density of nano-voids. The nano-voids are formed by a selective electrochemical porosification through dislocations followed by thermal annealing which act as a free surface for inhibiting dislocation propagation. The TD density is reduced significantly which will be crucial in cutting manufacturing costs of III-V multi-junction solar cells, if the bulk Ge substrates can be replaced with our engineered substrate.

1. INTRODUCTION

Multi-junction III-V concentrator cells have the most important energy conversion efficiency, competing with any other solar cell technology. Germanium appears to be the material of choice for the bottom cell to cover the IR part of the solar spectrum. A high efficiency of 40.7% was measured for a metamorphic three junctions GaInP/GaInAs/Ge cell at 240 suns. This architecture has achieved system efficiency of 30%. A road map based on the integration of Ge on Si wafers can be a solution to replace bulk Ge substrates and would result in a significant cost reduction. However, due to the important 4.2% lattice mismatch between Si and Ge, strain is introduced in epitaxial Ge layers on Si which leads to the generation of a high density of misfit dislocations. Dislocations act as recombination centers for carriers and strongly degrade the solar cell performance. Several techniques of dislocation reduction were reported in recent years such as graded SiGe buffer layers, cyclic annealing, aspect-ratio-trapping (ART), selective area depositions (SAD) and deep substrate patterning (DSP) [1]. However, the threading dislocations density (TDD) in the Ge layer remains higher than 10^6 cm^{-1} , reducing its usefulness for many device applications. In this talk, we will discuss a new strategy for making cost effective Ge/Si virtual substrate which is based on a simple and cost effective technique that uses nano-voids as a barrier for dislocation propagation. Then, we will present detailed optimization of the porosification and the annealing of Ge on Si and study the effect of different process parameters on TDD and on surface roughness.

2. EXPERIMENTAL RESULTS AND DISCUSSIONS

Approach:

As sketched in Fig 1, Ge/Si substrate was treated with post epitaxial process to create a region with a high density of nano-voids within the Ge layer on Si is expected to act as a barrier for threading dislocations propagation. Nano-voids are formed by electrochemical porosification followed by thermal annealing. The process is completed by CMP (chemical mechanical planarization) step to obtain an epi-ready virtual substrate [2].

Electrochemical etching of dislocated Ge/Si layer:

The porous morphologies obtained from the electrochemical etching of Ge/Si layer are quite different from that of the bulk Ge. For bulk Ge, the layer structure shows uniformly distributed meso-pores with controllable nanostructure and size [3]–[7]. However, for dislocated Ge/Si, non-uniformly distributed meso-pores are obtained (see Fig 2a and 4b). The porous layer consists of two zones: (i) a thin PGe layer formed at the surface, (ii) a thick PGe layer with weakly branched pores that trend to follow threading dislocation cores. Calibration of etching rates has been done by varying the current density in the electrochemical process. Fig 2c illustrates the dependence of the etching rate on the current density of bulk and dislocated Ge. The etch rate ratio between dislocated and bulk regions shows very high values up to 6. The preferential etching via dislocations can be explained by their high electrical conduction and their role in the transport properties with the electrolyte.

Nanovoid layer formation:

The morphological change of porous Ge during annealing is based on thermally activated jumps of surface atoms to stable positions following to the mass transport mechanism, for which atoms have a maximum of covalent bonds until their

outer energy level is full. In terms of geometry, atoms diffuse from the larger curvature surface toward the lower curvature surface down a gradient potential. Therefore, the pores in the volume are enlarged and the pores on the surface are closed. This reveals the formation of a crystalline region in the top surface and a voided region in the volume.

Dislocation-void interactions

Fig. 3 revealed that threading dislocations in relaxed Ge epilayer grown on Si were pinned and bent towards the nano-void area. Similar effect was observed by Myers et al. he suggests that this overlap is due to an attractive force created by a population of nano-voids with a binding energy that depends up-on the surface tension of the void and the relative positions of the interacting dislocation [8]. Also, during thermal annealing, TDs were stopped moving at the void probably because their gliding distance to the voids side-walls were very short. Therefore, the formation of surface-free regions located between the top surface of Ge and Ge/Si interface could be an effective tool to reduce significantly the TDD in Ge/Si layer. The TD free top layers offer a unique potential and a technologically attractive path for overgrowth of high quality Ge based optical devices.

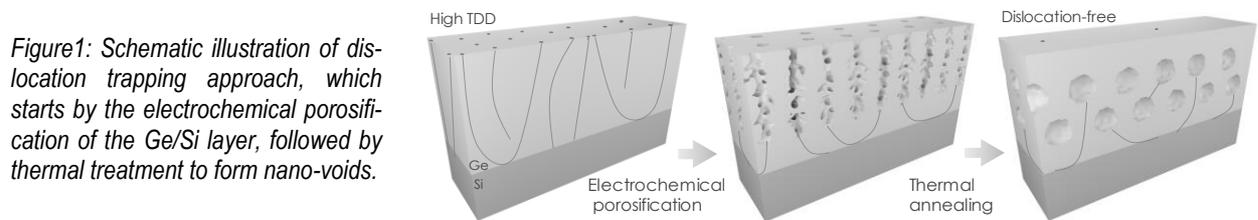


Figure1: Schematic illustration of dislocation trapping approach, which starts by the electrochemical porosification of the Ge/Si layer, followed by thermal treatment to form nano-voids.

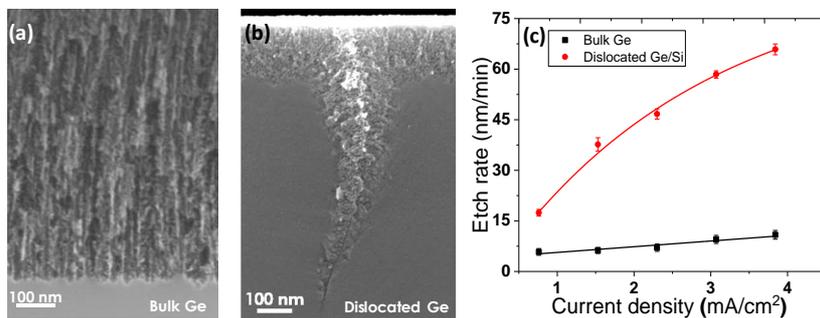
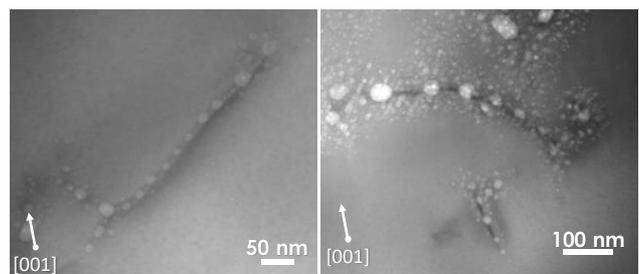


Figure2: Etching rate evolution versus the current density of bulk Ge and dislocated Ge/Si layer (a) and their cross-section SEM view (b,c) showing the preferential etching via dislocations.

Figure3: TEM images shows gliding dislocations pinned by nano-voids.



3. CONCLUSIONS

In this work, we proposed a new architecture of low cost virtual substrate engineering. This concept is promising for the fabrication of dislocation-free Ge on Si substrate. The resulting epi-ready surface will be used as the starting point for the deposition of the III-V junctions in the 3J PV cell. Using a simple, inexpensive process through electrochemical etching and thermal annealing will be crucial in cutting manufacturing costs and enabling market penetration of Ge based devices.

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