

High-quality Ge/Si virtual substrates fabricated by a low cost and scalable process

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1. Summary

In this presentation, we propose a new defect engineering strategy in highly mismatched hetero-epitaxy to simultaneously achieve low dislocation density and epi-ready Ge/Si virtual substrate using a highly scalable process. By self-assembling nanovoids around the Ge/Si interface from both sides through dislocation-selective electrochemical deep etching and thermal annealing, a continuous Ge layer is obtained, in which, a large portion of the original threading dislocations are pinned and annihilated close to a free surface (see Fig. 1), giving a new configuration so-called "Nanovoids-based Ge/Si Virtual Substrate (NVS)".

2. Introduction

Developing inexpensive, high-performance epitaxial devices with the hope of achieving widespread market adoption, depends critically on production costs and ultimate material quality. Any process that meets these challenges successfully provides solutions for a wide range of leading-edge applications. Due to the large difference in the lattice constant between the epitaxial materials and hetero-substrates, strain is introduced in epitaxial layer, which leads to the generation of a high density of misfit dislocations. Dislocations act as recombination centers for carriers and have a detrimental effect on device performance. Devices like photodetectors, multi-junction solar cells, transistors, modulators, based on Ge-on-Si (001) technology are facing these issues. To this end, several approaches have been proposed for reducing the TD density. However, many of these techniques are limited to small-scale processes and require the use of expensive and complex processing technologies. In addition, the TD density remains high for many device applications [1].

3. Results

Ge/Si (001) samples with high TDD are anodically porosified by the bipolar electrochemical etching technique [2]–[4]. The layer structure shows selectively distributed mesopores obtained by selective dislocations deep etching. The porosification front reaches the Ge/Si heterointerface, forming a porous layer in the Si substrate, as shown in Fig. 2. The resulting mesoporous Ge/Si structure is transformed into quasi-monocrystalline voided Ge on

voided Si during thermal annealing [5]–[7].

Fig. 3a. indicates the location where a dislocation segment ends at the nanovoid with no propagation beyond. A reasonable explanation for the TD reduction is that two dislocations with opposite Burgers vectors having the same magnitude have reached the void, according to fusions, complete and half annihilation reactions (See Fig. 3b-d). In such structure, the TDs have an interaction radius higher than the interaction radius in the conventional structure without voids, which in turn increases their recombination probability.

Fig. 4 ab. shows TEM micrographs from the Ge/Si reference and the NVS, respectively. A high defect density region, extending from the heterointerface towards the surface may be observed for the Ge/Si reference. A dense dislocation network confined in a region of 50 nm close to the Ge/Si interface of the NVS, and almost nonexistent defects within the Ge layer. In the NVS configuration, TDs bend towards the voids in Si onto the glide plane in order to minimize their length, causing their elimination at the nearest free surface. The averaged TDD is reduced significantly from $\sim 10^7 \text{ cm}^{-2}$ to $\sim 10^4 \text{ cm}^{-2}$ for 1.5 μm thick Ge layers, which is considered low for such a thin epitaxial layer (see Fig. 4a).

4. Conclusion

Ultra-low TDD in mismatched Ge on Si films is produced by a simple and inexpensive process, which consists on tuning the dislocation motion by self-assembling nanovoids close to the Ge/Si interface. It shows that introducing nanovoids favors recombination of dislocations by increasing their interaction radius. The voids located at the Si substrate act as a free surface for inhibiting threading dislocation propagation towards the active layer of the device, leading to the creation of an almost defect free Ge layer on Si.

References

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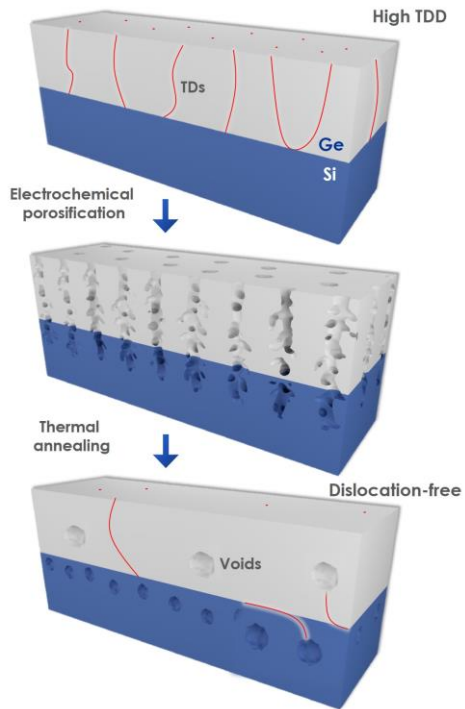


Fig. 1. Schematic illustration of the nanovoid based Ge/Si virtual substrate architecture.

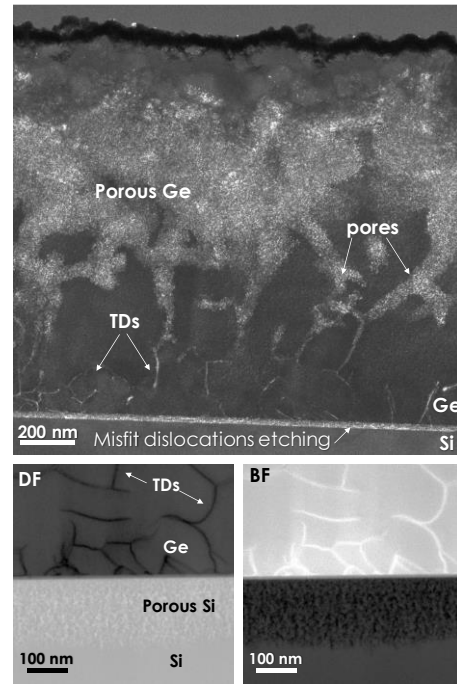


Fig. 2. TEM image of porous Ge/Si formed using a current density of 4 mA/cm^2 during 30 min shows a thick porous Ge layer with weakly branched pores crossing threading dislocation cores up to full uprooting of misfit dislocations.

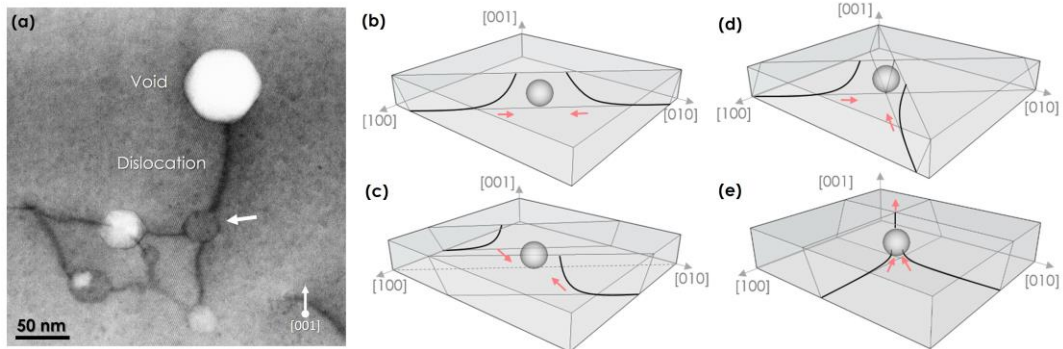


Fig. 3. BF-STEM image shows gliding dislocations in the Ge layer join the void area until its complete annihilation (a). Possible processes for annihilation of TDs at the void surface by interaction of several threading segments from: the same slip system (b), the parallel slip system (c), by a combination of glide and slip motion (d) and by fusion (e).

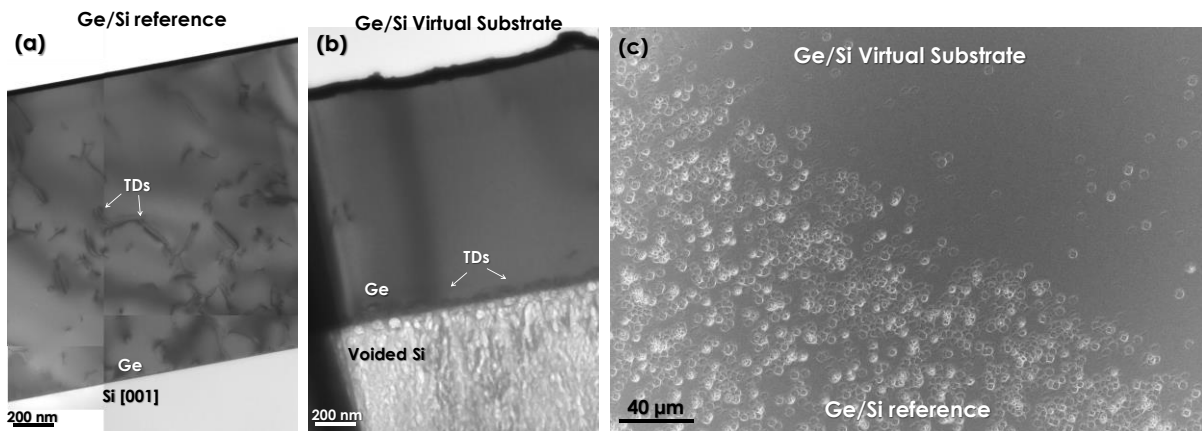


Fig. 4. TEM images of the Ge/Si reference substrate (a) and the nanovoid based Ge/Si virtual substrate (b) show the annihilation of dislocation segments coming from the Ge/Si interface at the void located in the Si substrate. (c) Etch-pit density taken from the edge of the NVS shows the TDD reducing from $\sim 10^7 \text{ cm}^{-2}$ to $\sim 10^4 \text{ cm}^{-2}$ for 1.5 μm thick Ge layer.