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► **To cite this version:**

Weiqun Liu, Adrien Badel, Fabien Formosa, Caiyou Zhao, Qiao Zhu, et al.. Comparative Case Study on the Self-Powered Synchronous Switching Harvesting Circuits With BJT or MOSFET Switches. IEEE Transactions on Power Electronics, 2018, 33 (11), pp.9506 - 9519. 10.1109/tpel.2018.2790965 . hal-01901537

HAL Id: hal-01901537

<https://hal.science/hal-01901537>

Submitted on 23 Oct 2018

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Comparative case study on the self-powered synchronous switching harvesting circuits with BJT or MOSFET switches

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Abstract: Self-powered realization for synchronous switching circuits is a hot spot for piezoelectric vibration energy harvesting. Two typical kinds of switches, bi-polar junction transistor (BJT) or metal oxide semiconductor field effect transistor (MOSFET) are popularly used without a clear understanding about the performance difference. In this paper, comparative investigations about adopting these two types of switches based on a case study are performed. It is analyzed that the performance difference comes from three aspects: the gate parasitic capacitance, the turning-on threshold and the driven mechanism. In particular, the third one imposes a critical influence on the performance. Investigations are performed on the self-powered synchronous switching circuit of two possible methods: with electronic breakers or with external control units. The results from simulations and experiments show that the current-driven mechanism limits the available performance in the case of the BJT switch in comparison with the case of the MOSFET switch. The difference is especially obvious for the cases of large piezoelectric capacitance and open-circuit voltage. A preliminary design guideline is concluded that the MOSFET is probably a better choice with the same voltage and current ratings in most cases.

Keywords: Piezoelectric generator; Synchronous switching circuit; BJT; MOSFET; Current-driven; Voltage-driven

1. Introduction

As one of the promising techniques for sustainable power source, piezoelectric generator can scavenge energy from ambient vibrations [1]. The researches about piezoelectric energy harvesting generally focus on two subjects: (1) the improvement on the mechanical structure to increase power density [2] or operation bandwidth [3-5] and (2) the study about the electronic interface

circuits of high performance to get the most power for the generator.

Generally, the interface circuit is used for regulating the alternative current (AC) from the generator to direct current (DC) and delivering the extracted power to the load. For this purpose, the standard circuit simply composed of a rectifier and a capacitor was firstly proposed [6]. However, a great part of energy is not extracted but returned to the dynamic system due to the limitation of the rectifier. This energy return phenomenon [7] makes its performance not good in low electromechanical coupling cases [8]. To increase the harvested power, many nonlinear synchronous switching harvesting techniques were developed, for instance, synchronized switch harvesting on inductor (SSHI) [9-11] and synchronous electric charge extraction (SECE) [12]. These circuits can significantly increase the harvested power in comparison with the standard circuit, especially in the case of low electromechanical coupling level. Moreover, as another desired property for the interface circuit, low load dependence is also observed. Further improvements were proposed on SSHI such as double synchronized switch harvesting (DSSH) [13], SSHI with magnetic rectifier (SSHI-MR) [14], enhanced SSHI [15] etc. or on SECE such as optimized SECE (OSECE) [16], tunable SECE [17] etc. Different features, such as better power or bandwidth etc. are provided with these circuits.

For these synchronous switching circuits, a critical issue in the way is the self-powered realization for the switching control. A variety of approaches have been studied, including mechanical switches [18-21], velocity control [22], integrated circuits [23-25] or electronic breakers [26-28]. Among them, the mechanical switch relies on the structure's dynamic motion to connect and disconnect, and it has the advantage of simplicity and fewer electronic components requirements. However, it is sometimes not so reliable because the switching position is not so adaptive and accurate. The velocity control utilizes an additional piezoelectric element as the sensing unit and drives the switches with an analog comparator, implying special fabrication requirements on the generator and slightly complex circuit [22]. The integrated circuit is the smartest with the possible realization of advanced control strategy but the most complex. The switch is controlled by either a clock divider [23] or a microcontroller [25] etc. Generally, the velocity control and the integrated circuit can be viewed together as the self-powered switching circuits with external control units. For this case, the switching instant can be precisely controlled with negligible phase lag. Compared with the former methods, the electronic breaker composed of an envelope and a comparator receives great interests due to its simplicity and reliability. It was firstly proposed for SSHI [26] and subsequently extended for other synchronous switching circuits [28]. In the self-powered

switching circuits, the electronic breakers powered by the piezoelectric source automatically detects the piezoelectric voltage maxima or minima and takes action to turn the switch on or off properly. The harvested power is strongly related to the available open-circuit voltage magnitude and the phase lag between the switching actions and the corresponding piezoelectric extrema in the self-powered circuits [27, 31]. In order to find out the relationship between the self-powered circuit's performance and the used components, an early analysis was conducted by Lallart and Guyomar including the voltage drop on the diode and the transistor [26]. Nevertheless, other components in the circuit were not accounted and the phase lag was assumed to be constant. Liang and Liao proposed a model with an improved analysis which contains the influence of the envelope capacitor and the leakage resistance of the piezoelectric element [27]. The phase lag induced by the diode and the transistor in the electronic breaker is analyzed. However, the RC delay introduced by the envelope detector's resistor and capacitor is neglected. The phase lag effect induced by charging the switch's parasitic capacitance with the envelope capacitance to turn on the switch is not studied either. More recently, a comprehensive modeling and analysis has been performed to take these two factors in consideration with more accurate results obtained [29].

Easy to find, as one of the most important components of the self-powered circuit, the switch plays a critical role in the circuit performance in the self-powered switching circuits with electronics. Even for the velocity control method and the integrated circuit approach in which the switching operations are controlled by external control units with phase lag negligible, the switches still affects circuit efficiency. However, few investigations have been performed to detail the switch's influence and the design guideline of the switch type selection from two typical available options: bi-polar junction transistor (BJT) or metal oxide semiconductor field effect transistor (MOSFET). Both of them have been popularly used, for instance, BJT in [26-27] and MOSFET in [22-25, 28]. It is interesting to investigate when BJT or MOSFET is better.

Due to the distinguished working principle, there are mainly three different aspects between BJT and MOSFET to be considered when used as switches in the self-powered synchronous switching harvesting circuits: the parasitic capacitance, the turning-on threshold and the driven mechanism. The former two will significantly affect the phase lag in the approach of electronic breakers. Meanwhile, the current-driven BJT and the voltage-driven MOSFET imposes variations in the circuit's energy transfer efficiency with electronic switches. They will together affect the selection of other circuit components and performance

discrepancy is expected to use the two type switches respectively. Consequently, comparison investigations about adopting these two types of switches are necessary and useful for the circuit design. For this purpose, a case study has been performed in this paper using the BJT TIP31C and the MOSFET Si2392ads which have comparable voltage and current ratings.

This paper is organized as follow: section 2 presents the introduction on the principle and operation of the self-powered OSECE (SP-OSECE) circuit with the electronic breaker. The SP-OSECE circuit is selected here for investigations as a representative of the synchronous switching circuits due to the easy feasibility and low load dependence [16]. It facilitates the discussion by choosing a constant load without affecting the generality. Section 3 presents the comparative investigations about the two switches types in the SP-OSECE circuit with electronic breakers and section 4 further performs the comparison of the two switches in the SP-OSECE circuit with other switching control approaches instead of electronic breakers. In the end, some conclusions are given in section 5.

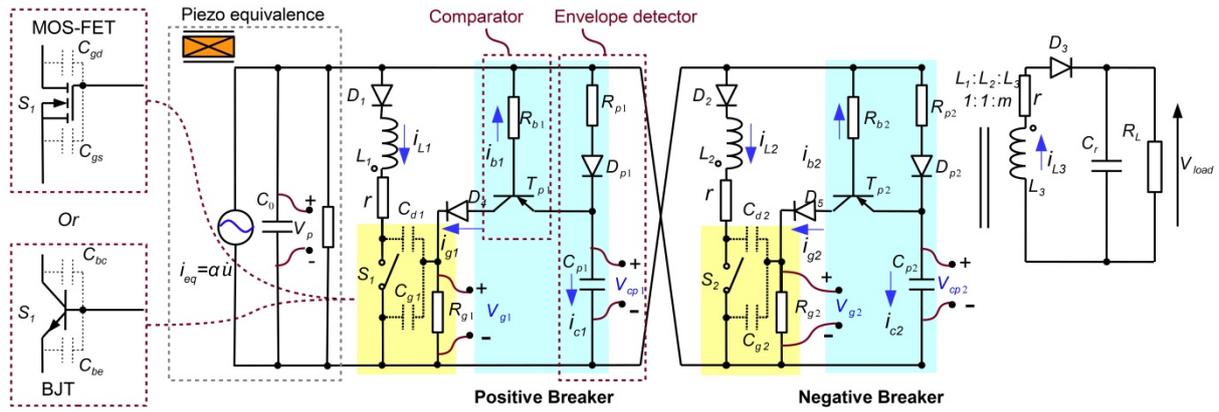


Fig. 1. SP-OSECE circuit with two possible switch types of MOSFET and BJT.

2. Principle of the SP-OSECE circuit with electronic breakers

Considering that the analysis about the SP-OSECE circuits is fully described in [28, 29], the principle will be briefly reminded for the readability. Fig. 1 presents the SP-OSECE circuit which mainly consists of two identical electronic breakers, two switches and a fly-back transformer composed of three windings L_1 , L_2 and L_3 with a 1:1:m turn ratio. The electronic breaker including an envelope detector and a comparator is used to produce the desired switching control signal at the piezoelectric voltage extreme position while the fly-back transformer is deployed for transferring the energy to the load. Regarding the switches S_1 and S_2 , they can be implemented with MOSFETs or BJTs with other components unvaried. Two capacitors C_{gi} ($i=1, 2$) and C_{di} for each switch are introduced to represent the parasitic capacitance of the MOSFET (C_{gs} , C_{gd}) and the BJT (C_{be} , C_{bc}) for the

consideration that C_{gs} or C_{be} plays an important role in the circuit performance [29]. C_{gd} or C_{bc} is also plotted for the completeness despite the insignificant effect on the circuit. Besides, two gate resistors R_{g1} are used at the control end of the switches. The usage of R_{g1} (R_{g2}) is based on two reasons: (1) discharging the reversely accumulated charge on C_{g1} (C_{g2}) last half period and (2) discharging C_{g1} (C_{g2}) to zero to turn off the switch S_1 (S_2) before the operation of S_2 (S_1). In this way, the switching operation is facilitated without the needs for additional neutralization charge from C_{pi} . Notably, a frictional resistor r is introduced in each inductor branch to stand for the parasitic serial resistance loss on the transformer and the diodes.

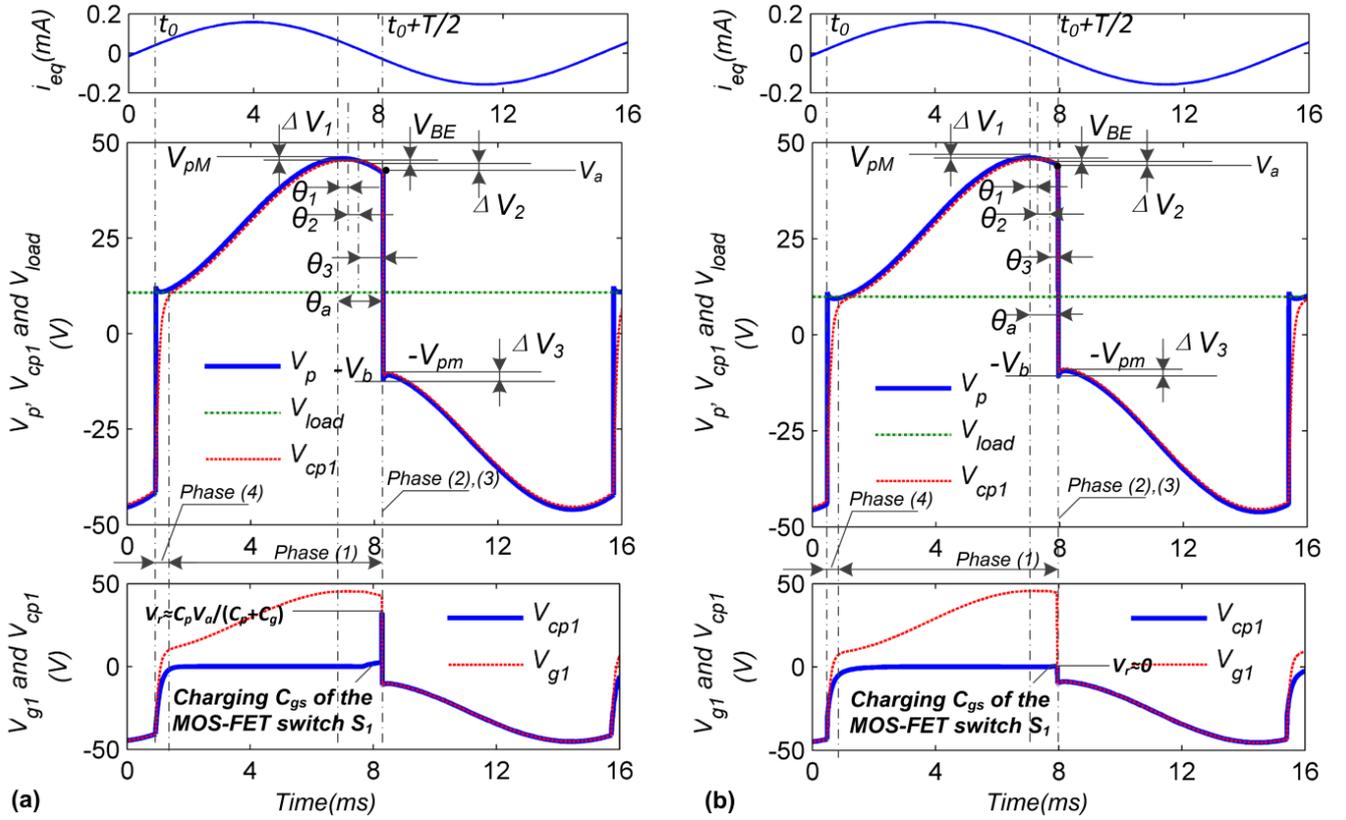


Fig. 2. Simulated voltage waveforms of the SP-OSECE circuit with two different switches and other components identical: (a) MOSFET Si2392; (b) BJT TIP31C.

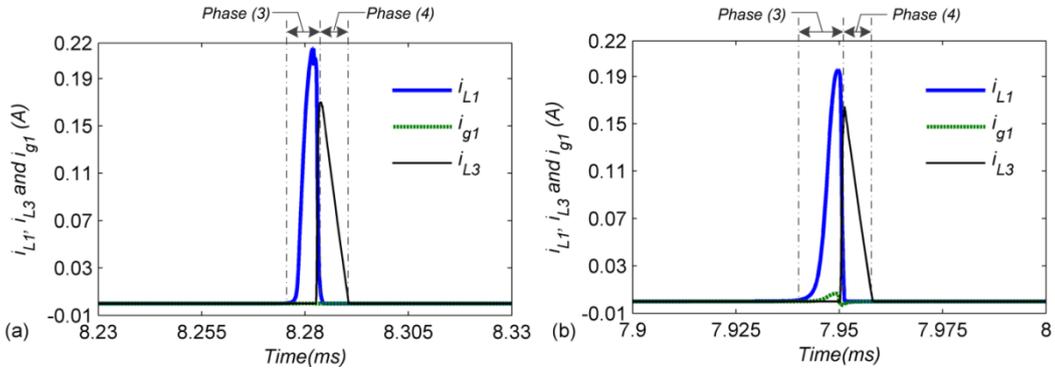


Fig. 3. Simulated current waveforms of the SP-OSECE circuit: (a) MOSFET Si2392; (b) BJT TIP31C.

In the circuit, the piezoelectric element is equivalent to a current source i_{eq} in parallel with an intrinsic capacitance C_0 and a leakage resistor R_0 . Considering that this paper is devoted to the circuit investigation, the piezoelectric generator is assumed to be

subjected to a sinusoidal motion of constant displacement amplitude u_M and $u=u_M \sin \omega t$ and we have

$$i_{eq} = \alpha \dot{u} = \alpha \omega u_M \cos \omega t \quad (1)$$

according to the piezoelectric constitutive equation. Here, α is the force-factor of the piezoelectric generator, ω is the vibration frequency and u is the displacement. Then the analysis about the piezoelectric generator with the SP-OSECE circuit can be performed completely from the electric aspect. Therefore, the current source i_{eq} is determined and a numerical model can be constructed in the LT-Spice© software. For comparison purpose, the waveforms of the SP-OSECE circuit in Fig. 2 and Fig. 3 are obtained with LT-Spice© software using the MOSFET Si2392ads and the BJT TIP31C as switches for $R_{p1}=R_{p2}=R_p=200\text{k}\Omega$ and $C_{p1}=C_{p2}=C_p=0.5\text{nF}$ with other components listed in Table 3.

As indicated in Fig. 2 and Fig. 3, the operation of the SP-OSECE circuit can be divided into four phases for each half-period between two switching operations: (1) natural charging; (2) voltage inversion; (3) energy transfer; (4) charge neutralization. Considering the positive half-period $t_0 \rightarrow t_0 + T/2$ ($T=2\pi/\omega$ is the period) as shown in Fig. 2, S_1 and S_2 are opened at the beginning of the natural charging phase. Both LC branches are blocked and the current i_{eq} charges C_0 with V_p increasing. At the meantime, the detector capacitor C_{p1} is also charged through R_{p1} and D_1 while C_{p2} and C_{g2} are charged through T_{p2} and the base resistor R_{b2} . As V_p reaches the extreme V_{pM} , V_{cp1} reaches the peak value $V_{pM} - \Delta V_1$ subsequently with some delay due to the RC circuit composed of R_{p1} and C_{p1} . The peak is then preserved by the envelope detector and V_p starts to decline. When V_p goes smaller than $V_{pM} - \Delta V_1 - V_{BE}$ (V_{BE} is the base-emitter voltage of T_{p1} and ΔV_1 is the voltage drop on R_{p1} and D_1), the comparator T_{p1} turns on and the current from C_{p1} charges C_{g1} to make V_{g1} greater than the threshold voltage V_{th} (V_{gs-th} for MOSFET and V_{BE} for BJT). During this process of turning on the switch, V_p further decreases to $V_{pM} - \Delta V_1 - V_{BE} - \Delta V_2$ and the nature charging phase (1) ends. Then the voltage inversion phase (2) starts in the form of LC oscillation (L_1 and C_0). Due to the configuration of the fly-back transformer, the energy stored in the LC circuit is not transferred at the first quarter of the LC oscillation due to the reversed bias of D_3 because the induced voltage on L_3 is negative. As the LC oscillation continues and V_p is reversely charged to $-(V_{load} + V_D)/m$ (V_D is the voltage drop on the diode), the voltage on L_3 at the secondary side becomes larger than $V_{load} + V_D$. The SP-OSECE circuit enters phase (3) with the energy stored in the transformer transferred to the load. Afterwards, the charge neutralization phase (4) begins due to the voltage difference between C_0 , C_{p1} , C_{p2} and C_{g1} . The current from C_0 starts to reversely charge C_{p1} , C_{g1} through (T_{p1}, R_{b1}) , and C_{p2} through

(R_{p2} , D_2). As a result, V_{g1} becomes negative and S_1 is closed. It is represented by RC process as indicated in Fig. 2 corresponding to the time constant τ_1 and τ_2 respectively. As a result, a voltage retreat towards zero for V_p due to the charge neutralization process can be observed in Fig. 2. At the meantime, the accumulated charge on C_{g2} with the positive V_{g2} (S_2 is closed when V_{g2} is negative and lower than the threshold) begins to discharge through R_{g2} . It facilitates the switching on of S_2 since the charge from C_{p2} is only required to charge C_{g2} to $-V_{gs-th}$ from zero instead of a relatively large positive value. With the positive half-period ending, the SP-OSECE circuit starts to operate similarly for the subsequent negative half-period.

3. Comparative investigations on the SP-OSECE circuit with electronic breakers

3.1 Analysis

In spite of the similar operations of the SP-OSECE circuit with the two different switches, it is noticed that the circuit performance represented by the load voltage V_{load} with the same R_L in Fig. 2 is different, 10.8V for the MOSFET and 9.9V for the BJT. The maximum piezoelectric voltage V_{pM} and the switching voltage V_{g1} in two cases differs as well. It implies that the switch type plays an important role on the circuit performance, thus it is meaningful to perform studies about the switch's influence for the improvement of the circuit design.

Using the model derived in [29], the SP-OSECE power performance can be written as

$$P_{SP-OSECE} = \frac{V_{load}^2}{R_L} \approx \frac{\eta f C_0 m^2 V_a^2}{(\eta f C_0 R_L + m^2)} \quad (2)$$

in which $f = \omega/2\pi$, η is the energy transfer efficiency of the circuit related to the circuit quality relies on the used components (diodes, switches, transformer, transistors etc.) and the working conditions such as the excitation level and the load situation etc. [30], m is the turn ratio and V_a is the piezoelectric voltage at the start of the voltage inversion phase:

$$V_a \approx V_{pm} + 2V_{oc} \cos \theta_a \approx \frac{V_{load}}{m} - \Delta V_3 + 2V_{oc} \cos \theta_a \quad (3)$$

where θ_a is the phase lag between the switching instant and the peak position V_{pM} , ΔV_3 is the voltage retreat variation due to the charge neutralization as indicated in Fig. 2 and V_{oc} is the generator's open-circuit voltage magnitude. Using eq. (2), we have

$$V_a = \frac{-\Delta V_3 + 2V_{oc} \cos \theta_a}{1 - \sqrt{\frac{\eta f C_0 R_L}{\eta f C_0 R_L + m^2}}} \quad (4)$$

and the open-circuit voltage magnitude can be expressed as

$$V_{oc} = \frac{V_{oc,org} \omega C_0}{\sqrt{V_{Re}^2 + V_{Im}^2}} \quad \text{and} \quad \varphi = \tan^{-1} \left| \frac{V_{Im}}{V_{Re}} \right| \quad (5)$$

with

$$\begin{aligned} V_{oc,org} &= \frac{\alpha u_M}{C_0} \\ V_{Re} &= \omega C_0 + \frac{\omega(C_g + C_p)}{1 + \omega^2(C_g + C_p)^2 R_b^2} + \frac{\omega C_p}{\omega^2 C_p^2 R_p^2 + 1} \\ V_{Im} &= \frac{1}{R_0} + \frac{\omega^2(C_g + C_p)^2 R_b}{1 + \omega^2(C_g + C_p)^2 R_b^2} + \frac{\omega^2 C_p^2 R_p}{\omega^2 C_p^2 R_p^2 + 1} \end{aligned}$$

Here, $V_{oc,org}$ represents the generator's original open-circuit voltage with R_0 neglected and the SP-OSECE circuit disconnected, $R_{b1}=R_{b2}=R_b$ is the base resistance of the comparator transistor T_{pi} and φ is the phase difference between $V_p=V_{pM}$ and $i_{eq}=0$. Eq. (4) is obtained on the basement that the SP-OSECE can be simplified as a RC network composed of R_{p1} , C_{p1} , C_{gs1} , C_{gs2} , C_{p2} and R_{b2} in the natural charging phase. This can be deduced from the circuit's operation principle in Fig. 1. When $\omega R_p C_p \ll 1$ and $\omega R_b(C_p + C_g) \ll 1$ are satisfied for the usual case, eq. (5) can be further simplified as

$$V_{oc} \approx \frac{C_0 V_{oc,org}}{C_0 + 2C_p + C_g} \quad (6)$$

As shown in Fig. 2, θ_a can be further divided into three parts: θ_1 from the envelope detector's RC circuit delay (R_{pi} and C_{pi}), θ_2 from the voltage drop to make the comparator turn on, and θ_3 from the charging process to turn on the switch. It holds

$$\begin{aligned} \theta_1 + \theta_2 &= \cos^{-1} \left(1 - \frac{\Delta V_1 + V_{BE}}{V_{oc}} \right) = \cos^{-1} \left(\frac{1 - V_D / V_{oc}}{\sqrt{1 + \omega^2 R_p C_p}} - \frac{V_{BE}}{V_{oc}} \right) \\ \theta_3 &= \theta_a - (\theta_1 + \theta_2) = \cos^{-1} \left(\frac{1 - V_D / V_{oc}}{\sqrt{1 + \omega^2 R_p C_p}} - \frac{V_{BE}}{V_{oc}} - \frac{\Delta V_2}{V_{oc}} \right) - \cos^{-1} \left(\frac{1 - V_D / V_{oc}}{\sqrt{1 + \omega^2 R_p C_p}} - \frac{V_{BE}}{V_{oc}} \right) \end{aligned} \quad (7)$$

in which ΔV_1 is the voltage drop on the diode D_{pi} and the envelope detector resistor R_{pi} , and

$$\Delta V_2 \approx C_g V_{th} / C_p + V_{th} \theta_3 / (\omega R_g) \quad (8)$$

is the voltage drop of V_p during the charging of C_{gi} until the corresponding switch is turned on. Obviously, θ_1 and θ_2 are almost not affected by C_g and V_{th} except the slight and indirect influence by V_{oc} . However, θ_3 is directly related to C_g and V_{th} as seen in eq. (7) and eq. (8) since it determines the time to charge C_g over V_{th} and the voltage drop ΔV_2 . In particular, the last term at the right side of eq. (8) accounts for the leakage current through the gate resistor $R_{gi}=R_g$ for this duration, implying that V_{th} imposes more influence than C_g .

With the same components except the switches, the values of m , R_p , R_b , C_0 , R_L , f and C_p are identical for both cases of

MOSFET and BJT switches. By carefully observing eq. (2) and (4), it can be deduced that the performance difference is only related to V_{oc} , ΔV_3 , θ_a and η . Analysis is thus performed on these variables for the two cases of BJT and MOSFET in order to understand the influence of the switch type. Before conducting the comparison, three pairs of BJT and MOSFET switches which have similar max allowed V_{DS} (or V_{CE}) / I_D (or I_C) are chosen to obtain a preliminary knowledge about the difference of the two switch types and the parameters are listed in Table 1. The ratings vary from 100V/3A, 60V/2A to 20V/1A in the around. Considering the power electronics applications, the switches with the current rating below 1A are not considered here. However, due to the difficulty to find the BJT and MOSFET switch with the exactly same rating, the MOSFET switch Si2392ads has a current rating of 3.1A for 100V grade and Si2308bds has a current rating of 1.9A for the 60V grade with the ambient temperature $T_A=25^\circ\text{C}$. It is assumed that the slight difference would not affect the investigations hereafter.

Table 1. Parameters for the selected BJT and MOSFET switches of three different ratings

Switches	Type	Ratings (V_{DS}/I_D or V_{CE}/I_C)	V_{th} (V)	C_g (nF)	$C_g V_{th}$ (nC)
Si2392ads [32]	MOSFET	100V / 3.1A	1.2~3, typically 2.3	0.1345	0.31
TIP31C [33, 34]	BJT	100V/3A	<1.8, typically 0.636	0.477	0.303
Si2308bds [35]	MOSFET	60V/1.9A	1~3, typically 1.9	0.133	0.253
PZT651T1 [36]	BJT	60V/2A	<1, typically 0.582	0.0745	0.043
SiUD402ed [37]	MOSFET	20V/1A	0.4~0.9, typically 0.62	0.01	0.006
BCP68T1 [38]	BJT	20V/1A	<1, typically 0.582	0.0745	0.043

Beside the ratings, Table 1 also shows the parameters of the switches in different aspects: the parasitic capacitance C_g (C_{gs} for MOSFET and C_{be} for BJT), the turning-on threshold V_{th} (V_{gs-th} for MOSFET and V_{BE-th} for BJT), and the product of the two $C_g V_{th}$. Since the parameters are not specifically given in the datasheet, the values used here are obtained from the Spice model provided by the manufacturer [32, 33] or the LTspice© library [34]. Moreover, the BJT's turning-on threshold V_{BE-th} adopts the base-emitter junction voltage V_{je} which is considered to be a reasonable estimation. It is close to the base-emitter voltage value with $I_B=1\text{mA}$. Besides, the base-emitter capacitance C_{be} adopts the junction capacitance C_{je} as well. From table 1, it is found that

V_{th} and C_g decreases with the maximum voltage and current ratings. Moreover, the MOSFET has larger V_{th} than the BJT does for higher ratings (100V/3A, 60V/2A) and the difference diminishes as the rating decreases (20V/1A). In contrast, C_g does not show a specific trend that the MOSFET or BJT has larger values than the other. It seems more likely dependent on the specific devices. In this paper, the comparison pair Si2392ads/TIP31C is used for following investigations due to the proper voltage rating, and more importantly, the close $C_g V_{th}$ values as seen in Table 1.

Table 2. Brief comparison summary between BJT and MOSFET switches

Definition	MOSFET	BJT	Preferred
Gate parasitic capacitance C_g	Depending on specific components	Depending on specific components	-
Turning-on threshold V_{th}	Relatively Larger for high ratings	Relatively Small for high ratings	BJT
Driving mechanism	Voltage-driven mechanism	Current-driven mechanism	MOSFET
C_g and V_{th} 's influence	(1) Introduce more phase lag;	(1) Introduce less phase lag;	BJT
	(2) Induce higher start voltage V_{start}	(2) Induce smaller start voltage V_{start}	
	(3) Decrease V_{oc} and V_a	(3) Decrease V_{oc} and V_a	
Driving mechanism's influence	(1) No requirement on C_p	(1) Minimum requirement on C_p to ensure the saturation working region	MOSFET
	(2) Slightly affect the energy transfer efficiency η by the drain-source resistance related to the gate-source voltage	(2) Significantly affect the efficiency η in the amplification region;	
		(3) High C_p decreases V_a , V_{oc} and increase the phase lag due to RC delay	

Among the parameters, C_g and V_{th} affects the open-circuit voltage V_{oc} and θ_a . Easy to find from eq. (6), V_{oc} decreases with C_g so that V_a gets smaller accordingly as indicated by eq. (2). Considering that C_g is usually much smaller than C_0 , V_{oc} won't vary much for both switch types. In contrast, a more notable influence on the phase lag θ_a is exerted by C_g and V_{th} together. Since the BJT and the MOSFET shows no obvious trend about C_g , the turning-on threshold V_{th} is mainly considered here.

An additional effect related to C_g and V_{th} is about the start voltage of the SP-OSECE circuit. In order to properly start the SP-OSECE, it requires the open-circuit voltage V_{oc} to be capable of turning on the switches. It implies that

$$V_{oc} - \Delta V_1 - V_{BE} = \frac{V_{oc} - V_D}{\sqrt{1 + \omega^2 R_p C_p}} - V_{BE} > \Delta V_2 \approx \frac{C_g V_{th}}{C_p} + \frac{V_{th} \theta_3}{\omega R_g} > \frac{C_g V_{th}}{C_p} \quad (9)$$

according to eq. (7) and eq. (8). When $\omega^2 R_p C_p \ll 1$ is satisfied, it yields

$$V_{oc} > C_g V_{th} / C_p + V_D + V_{BE} \quad \text{or} \quad C_p > C_g V_{th} / (V_{oc} - V_D - V_{BE}) \quad (10)$$

It can be drawn that a minimum V_{oc} , called as the start voltage V_{start} , is required to start the SP-OSECE circuit for the given C_p and the selected switches. In turn, a minimum requirement on C_p also exists for a given V_{oc} and selected switches. Due to relatively larger V_{th} , a higher V_{start} is needed for the MOSFET switch.

Beside C_g and V_{th} , the switch driven mechanism is another important factor of the SP-OSECE circuit performance. For MOSFET, the conduction of the switch is determined by the condition whether the gate-source voltage is larger than the threshold V_{gs-th} . As indicated by the waveform i_{g1} in Fig. 3 (a) that no visible current is required at the gate, the MOSFET is a voltage-driven device and its performance is related to the drain-source resistance R_{ds-on} , which is weakly dependent on the gate-source voltage as well. Here, for the Si2392ads in our case, R_{ds-on} differs from $0.1\Omega \sim 0.4\Omega$ with the gate-source voltage varying from $10V \sim 4.5V$ according to the datasheet [32]. High gate-source voltage leads to relatively low R_{ds-on} , thus slightly improved circuit quality factor and energy transfer efficiency η . Distinguished from the MOSFET with the voltage-driven mechanism, the BJT switch is a current-driven device, which means that continual base current is necessary to keep on the conduction of the BJT switch even though the base-collector voltage is greater than the threshold voltage V_{BE-th} . It is clearly seen in Fig. 3 (b) that a non-zero i_{g1} is injected into the base of the BJT. Depending on the base current, the BJT switch has three working regions: the amplification region with high DC current gain β of the order of hundreds, the saturation region with low DC current gain β of the order of dozens, and the cut-off region with ultra-low base current. When used as switches in the SP-OSECE circuit, the BJT is meant to work in the saturation region with small collector-emitter voltage V_{CE} so that the power dissipation on the BJT switch is small for the purpose of high efficiency. It requires the base current I_B is large enough to satisfy the following DC gain condition:

$$\frac{I_B}{I_C} > \frac{1}{\beta_c} \quad (11)$$

in which I_C is the collector current and β_c represents the assumed critical DC gain between the amplification region and the saturation region. To be noted, β_c might vary with the BJT's working condition and not have a fixed value. Then, using the integration of I_B and I_C over the time of the whole voltage-inversion process, we can deduce the following equation

$$C_p(V_a - V_{BE-th}) > Q_B > \frac{1}{\beta_c} Q_C \approx \frac{1}{\beta_c} C_0(V_a + V_{load} / m) \quad (12)$$

where Q_B is the total charge into the base during the voltage inversion phase, Q_C is the total charge into the collector. The last term at the right in eq. (12) represents the minimum charge on C_{pi} to ensure that the BJT switch operates in the saturation region while the first term at the left represents the maximal charge available on C_{pi} for the base current I_B . Especially, when both $V_a \gg V_{BE-th}$ and $V_a \gg V_{load}$ are satisfied (which corresponds to most cases), we have

$$C_p > \frac{1}{\beta_c} C_0 \quad (13)$$

It hints that a second minimum limit on C_p beside eq. (8) exists for a given C_0 to ensure the working point of the selected BJT switch to be in the saturation region. In particular, this minimum limit is inversely proportional to the BJT critical DC gain β_c and increases with C_0 . On the one hand, the dissatisfaction of eq. (13) will lead to the shift of the BJT switch's working point into the amplification region with high collector-emitter voltage V_{CE} so that the circuit energy transfer efficiency η will significantly decrease. On the other hand, the increase of C_p with respect to C_0 to satisfy eq. (13) decreases V_{oc} with a factor of $2C_p$ and increases $\theta_1 + \theta_2$ simultaneously, resulting in smaller $V_{oc} \cos \theta_a$ in eq. (4). A trade-off on the determination of the optimal C_p has to be made and the optimal C_p is inclined to show strong correlation with C_0 . It is especially unfavorable for large C_0 cases, in which a larger C_p has to be used with the BJT switch while a smaller C_p can be selected with the MOSFET with better performance in this point.

However, the current-driven mechanism of the BJT switch brings additional benefit on reducing the voltage retreatment ΔV_3 as implied in Fig. 2, which is favorable to the performance according to eq. (3). In the MOSFET case, during the process of turning on the switch S_i , the voltage between C_{pi} and C_{gi} is almost balanced around $V_i \approx C_p V_a / (C_p + C_g)$ (denoted in Fig. 2 (a)) and the remaining charge on C_{pi} to be neutralized can be calculated as $C_p^2 V_a / (C_p + C_g)$ while the remaining charge of the other envelope capacitance is estimated as $C_p V_{pM}$. Then the voltage retreatment ΔV_3 can be calculated according to the final voltage equilibrium between C_0 and the two capacitors C_{pi} ($i=1, 2$) after voltage inversion and we have

$$\Delta V_{3_MOS} \approx \frac{V_{load}}{m} - \frac{C_0 V_{load} / m - C_p^2 V_a / (C_p + C_g) - C_p V_{pM}}{C_0 + 2C_p + C_g} = \frac{C_p^2 V_a / (C_p + C_g) + C_p V_{pM} + (2C_p + C_g) V_{load} / m}{C_0 + 2C_p + C_g} \quad (14)$$

In the BJT case, after turning on the switches, the charge on C_{pi} is totally injected to the base due to the current-driven mechanism and the remaining voltage V_r and charge on C_{pi} to be neutralized is zero as seen in Fig. 3 (b). Only the remaining charge on the other envelope detector capacitance $C_p V_{pM}$ is to be neutralized. Consequently, the voltage retreatment ΔV_3 is calculated as

$$\Delta V_{3_BJT} \approx \frac{V_{load}}{m} - \frac{C_0 V_{load} / m - C_p V_{pM}}{C_0 + 2C_p + C_g} = \frac{C_p V_{pM} + (2C_p + C_g) V_{load} / m}{C_0 + 2C_p + C_g} \quad (15)$$

which is much smaller than the value in the case of MOSFET. It can be also observed from the waveforms in Fig. 3 that the voltage on C_{pi} after inversion is zero for the case of BJT switch and a large non-zero value of V_r is found for the case of MOSFET.

From the above analysis, it is found that the switch type affects the circuit performance from various aspects and different features are found for both types respectively. The BJT's low V_{BE-th} promises both lower phase lag θ_a and smaller start voltage V_{start} while the MOSFET can be used with smaller C_p for large C_0 which is favorable to the circuit performance. However, it is interesting to find from Fig. 2 and Fig. 3 that, although the BJT switch possesses benefits of smaller phase lag θ_a and voltage retreatment ΔV_3 , the circuit performance is still not as good as the MOSFET case. It implies that the current-driven mechanism of the BJT presents more critical limitations on the performance in this simulated case. In order to clarify the benefits and deficits of the two switch types and their influence on the circuit performance, further studies based on experiments and simulations have been performed and presented hereafter.

3.2 Results

To fulfil the comparative investigations about the two types of switches, a piezoelectric generator connected to the SP-OSECE circuit is prepared for experimental tests as shown in Fig. 4. It is composed of a steel cantilever beam (20mm×100mm×0.6mm) and a piezoelectric ceramic patch (20mm×30mm×0.4mm) attached to the beam top at the clamped end. A specially designed fixture is fabricated to fix the generator on a shaker (2075E-HT, The Modal Shop©), which is driven by a signal source (DG1032, Rigol©) through a power amplifier with a sinusoidal excitation of 67Hz around the generator's resonant frequency. With the laser displacement sensor (HL-C203BE, SUNX©) adopted, the displacement amplitude of the beam tip is controlled to be constant as $u_M=1.25\text{mm}$ by tuning the excitation level. Meanwhile, the voltage V_p and V_{load} are acquired by an oscilloscope.

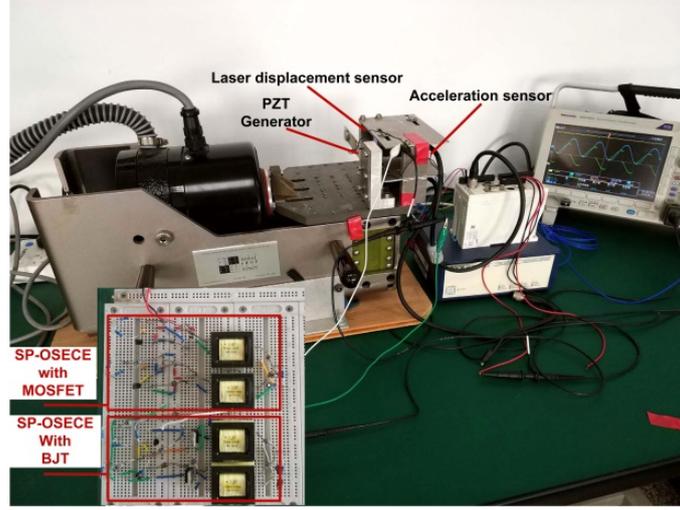


Fig. 4. Experimental set-up.

Table 3. Components and Parameters

Definition	Value	Definition	Value
MOSFET (S_i)	Si2392ads	BJT(S_i)	TIP31C
Transformer T_1	WE750811290 ($m=1$)	Transistor (T_{pi})	2N5401
Diodes(D_i, D_{pi})	BYV28-100	C_0	13.75nF
R_0	5M Ω	R_L	200 k Ω
α	0.0003 N/V	R_{pi}	200k Ω
R_{bi}	3.3 k Ω	R_{gi}	1 M Ω
f	67 Hz	u_M	1.25 mm

Parameter identifications are firstly performed on the piezoelectric generator. With C_0 measured by a multi-meter, α and R_0 are determined through the original open-circuit voltage response without circuit and the phase difference between the displacement and the voltage. Table 3 lists the parameter values as well as the electronic components used in the SP-OSCECE circuit. With the equivalent current source determined using eq. (1), two simulation models using the MOSFET Si2392ads and the BJT TIP31C as switches are then established using the LT-Spice© software. In the circuit, the resistor R_{pi} in the envelope detector is selected to 200k Ω for the purpose of avoiding misjudgment on the voltage extreme while the load resistor R_L is fixed to be 200k Ω for simplifying the investigations. However, it is thought that the load value wouldn't affect the comparison results with the same components since the load imposes identical effects on both cases according to eq. (1) and won't induce performance

difference, especially considering the low load dependence of the SP-OSECE circuit [18]. Notably, the serial resistance r is determined by fitting the simulations with experiments due to the difficulty of direct measurement.

As analyzed before, the SP-OSECE circuit's performance is closely related to the detector capacitance C_p . In view of that, multiple experiments and simulations with different C_p have been performed for the circuit with the MOSFET and BJT switches respectively. Fig. 5 shows the results for these two cases. As seen in Fig. 5 (a), the obtained open-circuit voltage values V_{oc} using two various switches are close to each other without obvious discrepancy and both decrease with the increasing C_p values. It is logic according to eq. (6) since the parasitic capacitance C_g is much smaller than C_0 with little effect on V_{oc} .

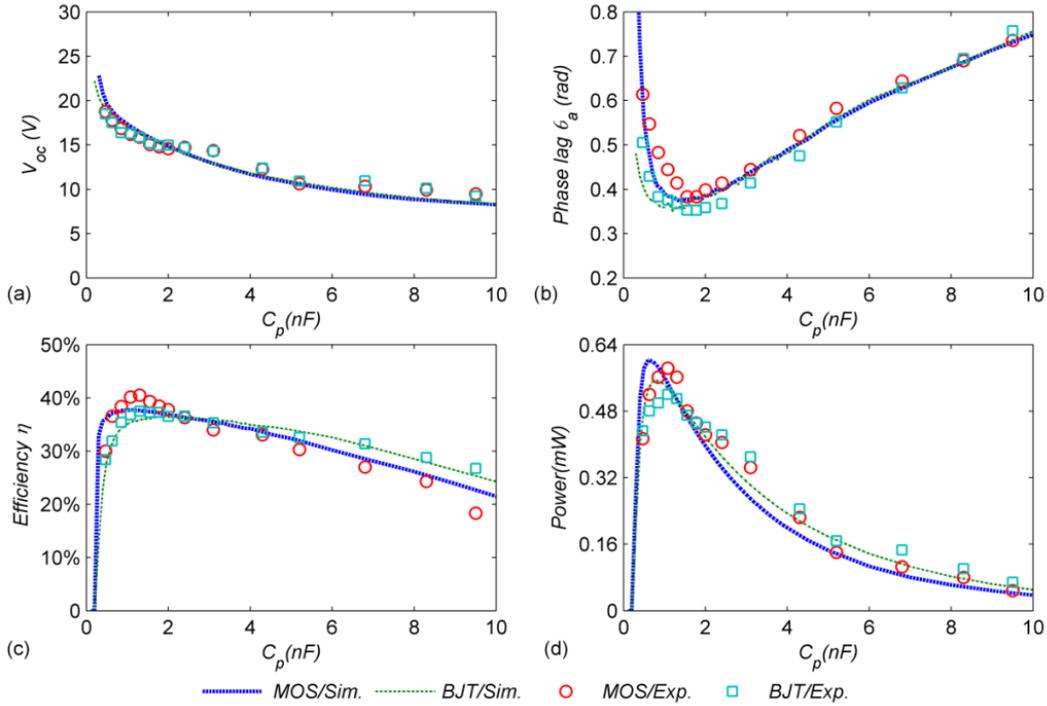


Fig. 5. Experimental and simulated results of the generator with SP-OSECE circuit using MOFFET Si2392ads and BJT TIP31C by varying C_p : (a) open-circuit voltage V_{oc} ; (b) phase lag θ_a ; (c) energy transfer efficiency η ; (d) harvested power.

In contrast, obvious discrepancy is observed for the phase lag θ_a in the two cases as shown in Fig. 5 (b), especially for small C_p values. The reason is that the MOSFET Si2392ads possesses larger V_{th} than the BJT TIP31C despite of similar product value of $C_g V_{th}$. According to eq. (7) and eq. (8), a larger voltage drop ΔV_2 is induced to turn on the switch Si2392ads, thus leading to the increase of θ_3 and θ_a . As C_p increases, ΔV_2 gets smaller according to eq. (8) and the proportion of θ_3 in the total phase lag θ_a decreases while the phase lag θ_a is dominated by $\theta_1 + \theta_2$ by virtue of the increased RC phase delay and the decreased V_{oc} according to eq. (7). The close results of θ_a for large C_p hint similar $\theta_1 + \theta_2$ with the two different switches, in accordance with the

aforementioned analysis. The same trend that the phase lag θ_a first decreases and then increases is found for both cases. It can be understood with eq. (7) and eq. (8) that, as C_p increases, the dominant θ_3 in θ_a for small C_p cases decreases to the secondary position while the sum $\theta_1 + \theta_2$ increases and begins to occupy the dominant position in θ_a for large C_p values. Therefore, an optimal C_p exists to obtain the smallest phase lag θ_a as shown in Fig. 5 (b).

As another important factor of the SP-OSECE circuit performance, the energy transfer efficiency η is also plotted in Fig. 5 (c). Higher efficiency is obtained in the case of the MOSFET switch Si2392ads in comparison with the case of the BJT switch TIP31C for small C_p values from 0.2nF to 2nF and the maximum efficiency in the MOSFET case is also higher than the one in the BJT case. It is because small C_p values are not able to provide the required current to let the BJT switch work in the optimal saturation region. Consequently, larger power dissipation on the BJT switch decreases the energy transfer efficiency. As C_p continually increases, the BJT works in the saturation region and better efficiency is found for BJT. The reason is that the BJT's benefit of reducing the voltage retreatment ΔV_3 becomes obvious for large C_p values with more charge to be neutralized.

Notably, the efficiency first increases then decreases with C_p in both cases while the power performance shows the same trend as seen in Fig. 5 (d). It is partly due to the C_p 's influence on the switch's conduction properties in the way of varying the working point of BJT or R_{ds-on} of MOSFET, and also partly due to the interaction between the load voltage and the efficiency itself. The power performance is related to the open-circuit voltage V_{oc} , the phase lag θ_a and the efficiency η at the same time. As seen in Fig. 5 (a) and (b), too small C_p introduces large phase lag (see Fig. 5 (b)) while too large C_p decreases V_{oc} and introduces more phase lag θ_a as well (see Fig. 5 (b) and (c)), leading to smaller V_a for both small and large C_p values according to eq. (3). The power performance would become worse correspondingly, implying smaller load voltage V_{load} as well. When the voltage drop on the diodes, the serial resistance r and the switches is comparable to V_{load} , the ratio of the energy consumed by these components during the voltage inversion and the energy transfer phases gets larger, leading to lower efficiency. In turn, the power performance is affected by the efficiency until the equilibrium achieves. Consequently, the efficiency η shows the trend similar to the power performance in Fig. 5 (d).

By inspecting the power performance in Fig. 5 (d), it is found that the circuit using the MOSFET switch case obtains higher max performance, about 112% of the one with the BJT switch. Considering the larger phase lag introduced by the MOSFET

Si2392ads and the similar V_{oc} in both cases, it shows that the efficiency plays a critical role in the performance. More specifically, the current-driven mechanism decreases the available maximum power due to the trade-off between $V_{oc}\cos\theta_a$ and η . As C_p continually increases, the BJT in the saturation region brings superior power performance due to the less neutralized charge.

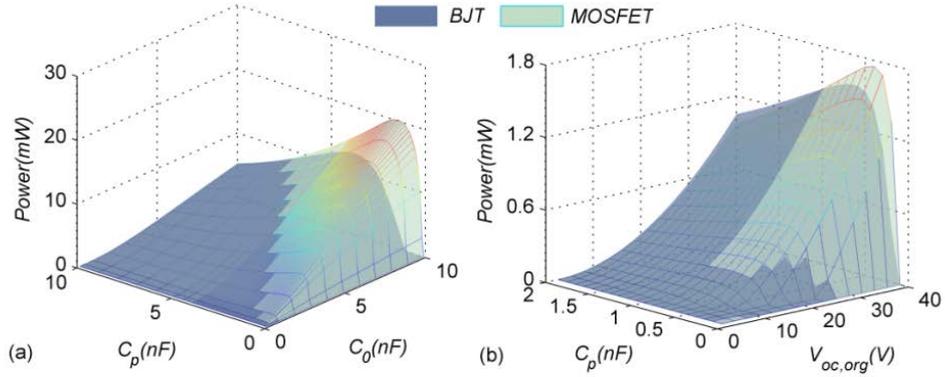


Fig. 6. Simulated power performance of the SP-OSECE circuit: (a) varying C_0 and C_p with constant original open-circuit voltage $V_{oc,org}$; (b) Varying $V_{oc,org}$ and C_p with C_0 constant.

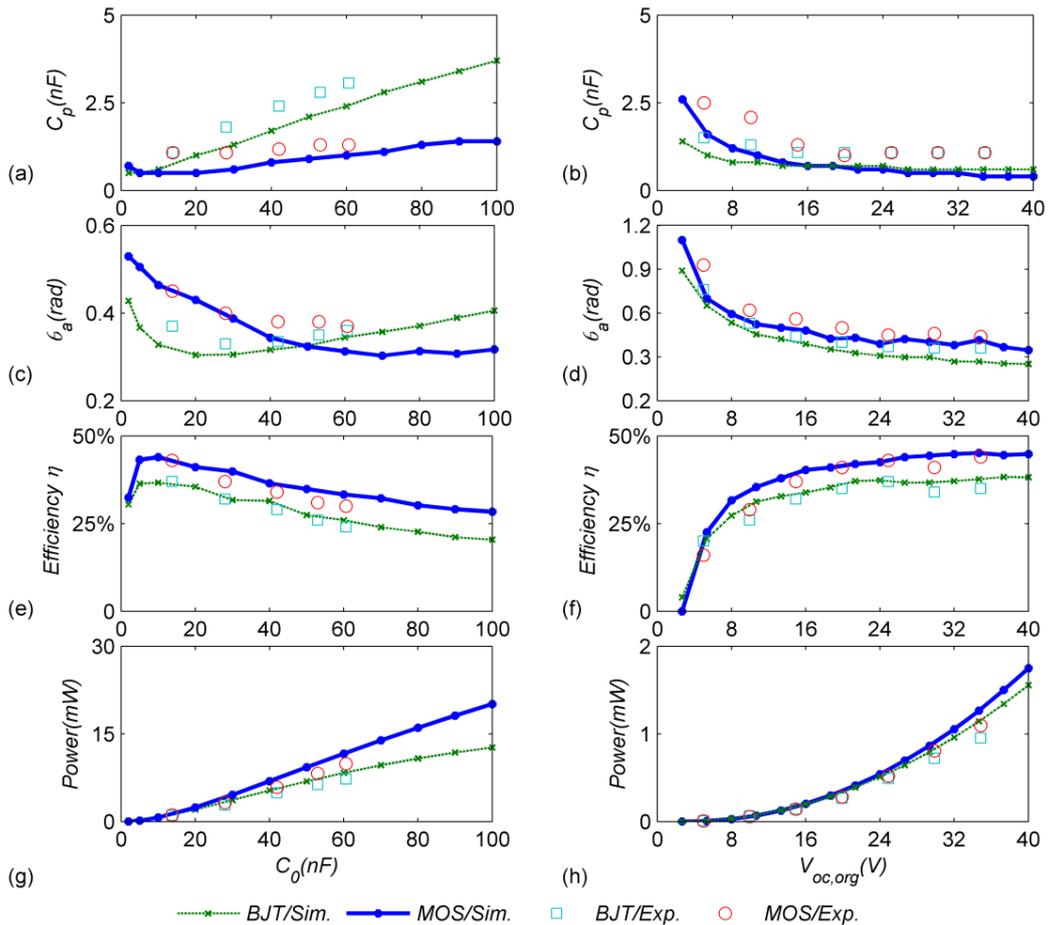


Fig. 7. The optimal power performance of the SP-OSECE circuit and the corresponding values of C_p , θ_a and η : left column (a, c, e, g) varying C_0 with constant $V_{oc,org}$; right column (b, d, e, f) varying $V_{oc,org}$ with constant C_0 .

Since a minimum C_p is required to ensure the proper working region of the BJT switch for better efficiency and performance, it can be inferred that this minimum C_p for BJT switches determined by eq. (13) increases with C_0 . The effects of decreasing

$V_{oc}\cos\theta_a$ will become more obvious making the obtained V_a values smaller according to eq. (3). As a result, the available optimal performance using the BJT switch is inclined to be even worse in comparison with the case of using the MOSFET switch as C_0 increases. In addition, the performance comparison for different original open-circuit voltage $V_{oc,org}$ corresponding to different excitation levels is also meaningful to obtain a more complete and better understanding about the influence of the two different switch types. For these reasons, additional studies are performed for two typical cases: (a) generators with C_0 from small to large values with the same original open-circuit voltage $V_{oc,org}$; (b) the same generator (C_0 constant) with $V_{oc,org}$ from small to large values. Consequently, a more complete comparison can be made for the two switch types. Considering that good agreements between experiment and simulation are validated in Fig. 5, the LT-Spice© models are further used for the followed investigations.

Fig. 6 (a) shows the comparison results of the power performance when the generator's intrinsic capacitance C_0 varies from 2nF to 100nF with $V_{oc,org}$ constant as 37.5V and C_p varying from 0.1nF to 10nF for each C_0 case. It is shown the BJT switch brings almost the same optimal power as the MOSFET switch only in very small C_0 cases (no more than 5nF). As C_0 increases, the MOSFET switch case outperforms the BJT switch case with much better power. However, for large C_p values deviating from the optimal region of the power performance, the BJT brings slightly better performance than the MOSFET due to the benefit of less charge neutralization as analyzed in last section. Fig. 6 (b) presents the comparison results in the other case that the generator's original open-circuit voltage $V_{oc,org}$ varies from 2.7V to 40 V with C_0 constant as 13.75nF. It is seen that the BJT brings slightly better optimal performance for low $V_{oc,org}$ values while the MOSFET outperforms for large $V_{oc,org}$ values. The reason is that the phase lag introduced by BJT is smaller than the one introduced by MOSFET for small $V_{oc,org}$ values and it imposes more positive effects with the negative effects of the current-driven mechanism compensated.

In order to have a detailed view about the comparison, the optimal results in these two cases are plotted with the corresponding C_p , θ_a and η depicted for the variable C_0 case (left column) and the variable $V_{oc,org}$ case (right column) in Fig. 7. The following facts can be found that:

(1) As C_0 increases, the optimal C_p increases correspondingly in the BJT case but stays almost stable in the MOSFET case as indicated in Fig. 7 (a). It is consistent with eq. (13) for the BJT case due to the current-driven mechanism. The very slight increase of the optimal C_p in the voltage-driven MOSFET case is attributed to the lower phase lag (see Fig. 7 (c)) since increasing C_p

slightly will effectively decrease ΔV_2 for relatively large C_0 values. Meanwhile, except the same decreasing trend for both cases at the beginning, the opposite trend is observed for the phase lag θ_a which increases with C_0 for the BJT case but decreases for the MOSFET case for relatively large C_0 case as shown in Fig. 7 (c). In the BJT case, the increasing optimal C_p enlarges both the phase lag θ_1 by introducing additional RC delay and the phase lag θ_2 by lowering V_{oc} so that θ_a increases. In the MOSFET case, with $V_{oc,org}$ constant and C_p almost unvaried for the increasing C_0 , the obtained open-circuit voltage V_{oc} will increase according to eq. (4), leading to the decrease of θ_2 and θ_a as well. Regarding the efficiency η in Fig. 7 (e), the efficiency decreases with C_p for both cases due to the circuit quality factor reduced with the increase of C_0 . However, the decline speed of the efficiency in the BJT case is slightly faster than the speed in the MOSFET case. It is also attributed to the decrease of V_{oc} induced by the larger optimal C_p for the BJT switch. With the analysis above, it can be explained that the BJT switch brings similar performance for small C_0 but much worse performance for large C_0 in comparison with the MOSFET switch as indicated in Fig. 6 (a) and Fig. 7 (g), which is in accordance with the previous analysis in section 3.1. The optimal power with the MOSFET switch is 158.52% of the power with the BJT switch in the case of $C_0=100\text{nF}$.

(2) As seen in Fig. 7 (b), the optimal C_p with the MOSFET is higher than the one with the BJT for small $V_{oc,org}$ cases since larger ΔV_2 is required due to the higher V_{th} of Si2392ads. However, as $V_{oc,org}$ increases, the optimal C_p decreases in both cases. Notably, the optimal C_p with the MOSFET switch continues getting smaller and becomes lower than the one with the BJT switch which approaches to the minimum requirement of C_p according to eq. (13). Meanwhile, the increasing $V_{oc,org}$ makes the phase lag induced by ΔV_2 become smaller and negligible. Consequently, the phase lag θ_a decreases as $V_{oc,org}$ increases and approaches a constant value and the MOSFET always brings larger phase lag as shown in Fig. 7 (d). In contrast, the efficiency increases in both cases to a stable value as indicated in Fig. 7 (f) since the dissipation on diodes becomes negligible for high $V_{oc,org}$ cases and the efficiency is mainly determined by the circuit quality factor related to the transformer and the switch. Due to the trade-off between the optimal C_p and the efficiency induced by the current-driven mechanism, the BJT presents lower efficiency than the MOSFET for most cases and the difference is enlarged for large $V_{oc,org}$ cases. As a result, the optimal power in both cases is similar without obvious difference for small $V_{oc,org}$ while better results are found with the MOSFET switch for large $V_{oc,org}$ values. The power with the MOSFET switch is 112.41% of the power with the BJT switch for $V_{oc,org}=40\text{V}$.

For the purpose of validating the simulation results, experimental tests are performed on a generator with four piezoelectric patches. By varying the connected piezoelectric patch number and connecting an additional capacitance in parallel, the capacitance C_0 of the generator can be changed while the original open-circuit voltage is set to 37.5V as simulation for the case of left column in Fig. 7. However, in order to avoid damage of the generator, the maximum capacitance tested in Fig. 7 is around 60nF since high displacement amplitude is required to obtain the open-circuit voltage of 37.5V as C_0 increases. For the right column, a single piezoelectric patch is still used with the original open-circuit voltage changed by displacement amplitude. By checking the experimental results with the simulation, it is clear that the experimental results shows similar trend as the simulation and confirm the analysis well.

Experimental investigations are also performed about the SP-OSECE circuit's start voltage V_{start} , which is considered as an important figure about the circuit performance. It reflects when the circuit will start to work. Lower start voltage means the circuit can harvest energy from lower displacement amplitude u_M , corresponding to lower vibration level. Fig. 8 presents the experimental results of the SP-OSECE circuit with the two various types of switches. In both cases, V_{start} decreases with C_p as expected from eq. (10) since the voltage drop ΔV_2 to turn on the switch become smaller. In particular, V_{start} in the case of using the BJT switch is always smaller than the corresponding value in the case of using the MOSFET switch.

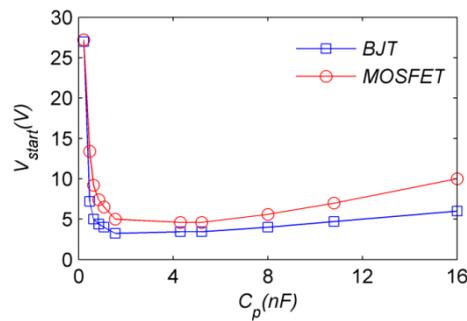


Fig. 8. Experimental start voltage of the SP-OSECE circuit with two different types of switches.

From the analysis above, it is shown that, due to relatively higher V_{th} , the MOSFET Si2392 brings higher start voltage V_{start} and larger phase lag than the BJT TIP31C. However, in comparison with the BJT TIP31C, similar performance is still obtained with the MOSFET Si2392 in smaller C_0 or $V_{oc,org}$ cases and much better performance is available for higher C_0 or $V_{oc,org}$ cases. It confirms that the current-driven mechanism of the BJT plays a critical role and restricts the optimal power performance to be worse than the one with the MOSFET of voltage-driven mechanism, especially for large C_0 or $V_{oc,org}$ cases. It can be further

inferred that with identical V_{th} and C_g , the MOSFET would be always superior to the BJT in the SP-OSECE circuit with electronic breakers (optimal C_p used) while V_{start} would be the same.

4. SP-OSECE circuit with external control units

Beside the electronic breaker approach, the SP-OSECE circuit can also be realized with external control units, for instance, the velocity control approach [22] or using the integrated circuits [23, 24]. It is meaningful to investigate the switch type influence in these methods to provide a more complete comparison study. Generally, the external control unit can be represented by an equivalent pulse voltage source V_s with a series resistor R_s according to Thevenin's theorem as shown in Fig. 9. For simplifications, it is assumed that the low level output of V_s is zero to turn off the switches and the high level output is V_H to turn on the switches. Considering the relatively small values of R_s (usually less than 100k Ω) and C_g (in the order of 0.1nF), the phase delay for turning on the switch is small and negligible.

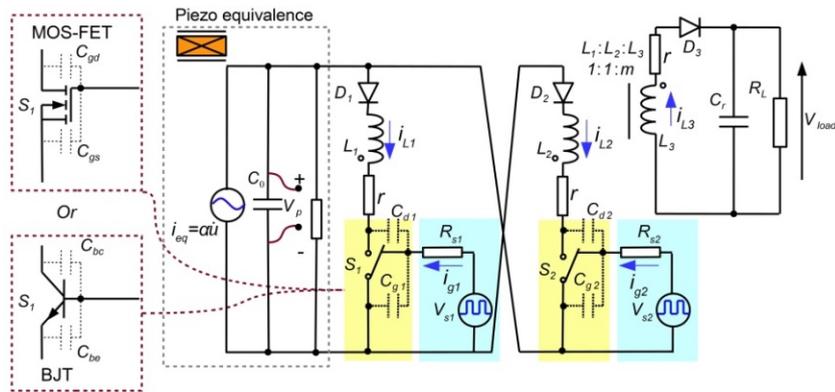


Fig. 9 Equivalent circuit for the SP-OSECE approach with external control circuit.

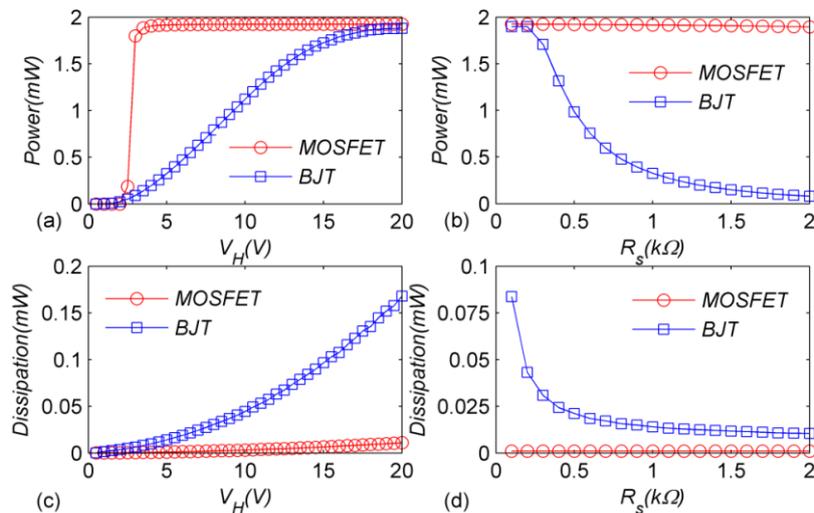


Fig. 10 Performance comparison between the SP-OSECE circuit with external control units and two different switches of the MOSFET Si2392ads and the BJT TIP31C: (a) power with $R_s=2k\Omega$ and variable V_H ; (b) power with $V_H=5V$ and variable R_s ; (c) dissipation in the variable V_s case; (d) dissipation in the variable R_s case.

Fig. 10 (a) shows the power performance for the case of $R_s=2k\Omega$ and variable V_H . This resistance value is selected according to the estimated results from the datasheet of TLV3701 [39] which was used in the velocity control method [22]. It is seen that the power output of the circuit using the BJT switch TIP31C starts for very small V_H values and gradually increases to a stable value. It can be explained by the lower turning-on threshold V_{th} and the current-driven mechanism of the BJT since the small V_H values is not enough to supply the current for the BJT in the saturation region. Therefore, the performance is limited unless V_H is large enough as indicated in Fig. 10 (a). In contrast, the power output of the circuit with the MOSFET Si2392ads starts for a slightly larger V_H value due to the higher V_{th} values but rapidly increases to the maximum value due to the voltage-driven mechanism. Fig. 10 (b) shows the performance for the other case of $V_H=5V$ and variable R_s . Clearly, the performance of the circuit with MOSFET is almost unaffected while the power of the circuit with BJT decreases gradually with R_s from a certain small value around 100Ω . It implies that the current supplied by V_s is not sufficient to provide the optimal working condition for the BJT TIP31C when R_s increases. Obviously, the current-driven mechanism of the BJT makes the performance susceptible to external control circuits and special considerations are required for design.

To be noted, the power dissipation for the operation of the switches is another important factor to be considered. When the external control circuits are powered by additional independent sources, the power dissipation might be not so relevant. However, if the external control circuits are powered by the harvested power, the dissipation for operating the switches will play an important role in the final net power. For the MOSFET, the dissipation can be estimated as:

$$P_{d_mos} = 2fC_g V_H^2 \quad (16)$$

which is used to charge C_g to V_H without continual current required. As for the BJT, it can be estimated as:

$$P_{d_BJT} = 2f \int_0^{T/2} V_s i_g dt \approx 2fV_H (C_0 V_{pM} / \beta + C_g V_{th}) \quad (17)$$

Clearly, it is composed of two parts: (1) the consumption for turning on the BJT and (2) the consumption of keeping the BJT's conduction during the voltage inversion. Here, it is assumed the BJT is turned off exactly when the voltage inversion is finished. In order to make BJT work in the saturation region, we have $\beta > \beta_c$. Considering the normal case of $C_g < C_0 / \beta_c$ and $V_H < V_{pM}$, P_{d_BJT} is inclined to be larger than P_{d_MOS} . It is verified by the results in Fig. 10 (c) and (d) with the two different switches and other parts identical. It is found that the dissipation in the BJT case is much higher than the one in the MOSFET case. Moreover, the

dissipation in the BJT case increases when V_H increases or R_s decreases. It is due to the increase of the gate current i_g . Meanwhile, dissipation in the MOSFET case increases slowly with V_H but does not vary with R_s , as indicated in eq. (16).

It can be thus concluded that the MOSFET switch is a more favorable option for the SP-OSECE circuit with external control units in comparison with the BJT switch based on two reasons: (1) the facilitation of reaching stable maximum power and (2) less power dissipation for operation.

5. Conclusion

In this paper, comparative investigations have been performed about the influence of the switch type (BJT or MOSFET) on the performance of the SP-OSECE circuit. The analysis reveals that the performance difference comes from three aspects: the gate capacitance C_g (C_{gs} for MOSFET or C_{be} for BJT), the turning-on threshold voltage V_{th} (V_{gs-th} for MOSFET or V_{BE-th} for BJT) and most importantly, the driven mechanism (the voltage-driven mechanism for MOSFET or the current-driven mechanism for BJT). Preliminary survey on the available BJTs and MOSFETs for the power purpose shows that the MOSFET usually has higher turning-on threshold with the same voltage and current ratings while the gate capacitance does not have a specific trend. Followed investigations by experiments and simulations based on the case study of adopting the BJT TIP31C and the MOSFET Si2392ads show that

- (1) For the SP-OSECE circuit with electronic breakers, the BJT switch has the advantage of lower start voltage V_{start} and less phase lag for small C_0 cases (See Fig. 7) due to the relatively lower turning-on threshold V_{th} . However, the current-driven mechanism of the BJT requires a minimum C_p which increases with C_0 at the same time. In contrast, the voltage-driven mechanism of the MOSFET only requires C_p to charge the gate capacitance C_g and turn on the switch with small phase lag in consideration of the trade-off for V_{oc} . The optimal C_p in the MOSFET case shows weak dependence on C_0 and decreases as $V_{oc,org}$ increases. Consequently, small optimal C_p values are obtained in the MOSFET case. It makes the circuit with the MOSFET switch shows much better results on the available optimal power than the one with the BJT switch for large C_0 cases. Moreover, the optimal power performance using the MOSFET switch is close to the one with the BJT switch even in the small C_0 cases.
- (2) For the SP-OSECE circuit with external control units, the BJT switch always show worse performance than the

MOSFET except smaller start voltage. The current-driven mechanism requires the external unit to provide higher driving current to let the BJT work in the saturation region. Otherwise, the performance degenerates rapidly. Meanwhile, the MOSFET shows stable performance which are less affected by external control circuits.

With the same voltage and current ratings, it can be therefore concluded that the MOSFET switch is superior to the BJT one for most aspects except the start voltage. Finally, it is reminded that the investigations are performed on the SP-OSECE circuit using the BJT or MOSFET switches, but can be extended to other self-powered synchronous circuits and other switch types of current or voltage driven mechanism with the same operations.

Acknowledgements

The authors would like to thank the support from National Natural Science Foundation of China (NSFC) under the grant No.51505395, Science & Technology department of Sichuan (2016HH0028), China Postdoctoral Science Foundation (2017T100709, 2016M600747) and the Fundamental Research Funds for the Central Universities (2682017CX26, 2682017CY05).

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