A Comprehensive Analysis and Modeling of the Self-Powered Synchronous Switching Harvesting Circuit With Electronic Breakers

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***Abstract*—Self-powered realization for synchronous switching circuits is a hot spot for piezoelectric vibration energy harvesting. As a well-known approach, the electronic breaker is widely used for its simplicity and reliability. It plays an important role on the performance of the piezoelectric generator by affecting the available open-circuit voltage and the switching phase lag. In this paper, a comprehensive model is developed for improved performance analysis with missed factors included in comparison with previous investigations. The combined influence of the envelope resistor and the capacitor on both the phase lag and the open-circuit voltage is newly considered while the additional phase lag effect induced by charging the switch parasitic capacitance with the envelope capacitance is supplemented. Experiments and simulations validate the proposed model with better accuracy and the results show that these supplemented factors are important to the generator performance, especially for the micro-power energy harvesting with small piezoelectric capacitance or displacement magnitude. Moreover, more detailed design guidelines are deduced from the proposed model.**

***Index Terms*— Piezoelectric Energy harvesting, Self-powered synchronous switching circuit; Electronic breaker.**

I. INTRODUCTION

THE rapid development of micro power circuits promotes new possibilities of scavenging energy from environment vibrations, leading to the advancement of wireless sensor network (WSN) of battery free [1]. Piezoelectric generator is one of the promising techniques that can scavenge energy from ambient vibrations. Beside the improvement on the mechanical structure to increase power density [2] or operation bandwidth [3-4], the study of electronic interface circuits is another important subject. For the purpose of regulating the alternative current (AC) to direct current (DC) from harvested electricity, the standard circuit composed of a rectifier and a capacitor was firstly proposed [5]. However, the energy return phenomenon that part of the energy without being extracted goes back to the mechanical system [6] makes its performance not good in low electromechanical coupling cases [7]. To increase the harvested power, many synchronous switching harvesting techniques were developed, for instance, synchronized switching harvesting on an inductor (SSHI) [8-10] and synchronous electric charge extraction (SECE) [11]. The advantages of performance enhancement in low electromechanical coupling cases and low load dependence were observed for these circuits. Further improvements on SSHI such as double synchronized switch harvesting (DSSH) [12], SSHI with magnetic rectifier (SSHI-MR) [13] etc. or on SECE such as optimized SECE (OSECE) [14], tunable SECE [15] etc. were proposed with different features as well.

For these synchronous switching circuits, the self-powered realization remains a hot topic. A variety of approaches have been studied, including electronic breakers [16-18], mechanical switches [19-21], velocity control [22] or integrated circuits [23-25] etc. Among them, the electronic breaker composed of an envelope and a comparator receives great interests due to its simplicity and reliability. It is firstly proposed for SSHI [16] and subsequently extended for other synchronous switching circuits [18]. In the self-powered switching circuits with electronic breakers, the switches, which are in fact powered by the piezoelectric source, automatically take actions to invert the piezoelectric voltage based on the information from the peak detectors that the maxima or minima are attained. Therefore, the harvested power is strongly related to the available open-circuit voltage magnitude and the phase lag between the switching actions and the corresponding piezoelectric extrema in the self-powered circuits [17].

Lallart and Guyomar conducted a primary analysis by including the voltage drop on the diode and the transistor [16]. Nevertheless, other components in the circuit were not accounted and the phase lag was assumed to be constant. Liang and Liao presented an improved analysis which contained the influence of the envelope capacitor and the leakage resistance of the piezoelectric element [17]. The phase lag induced by the

Manuscript received May 23, 2017; revised Sep. 10, 2017; accepted Oct. 3, 2017. Corresponding author: Weiqun Liu.
This work was supported in part by the National Natural Science Foundation of China under Grant 51505395, China Postdoctoral Science Foundation under Grant 2017T100709 and 2016M600747 and the Fundamental Research Funds for the Central Universities under Grant 2682017CX26 and 2682017CY05.
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diode and the transistor in the electronic breaker was analyzed as well. The design and optimization of the self-powered synchronous switching harvesting circuits relies on the accurate model. However, the envelope resistor and capacitor's influence is not well analyzed in existed models. In particular, the switch's parasitic capacitance and turn-on threshold are not considered either. In this paper, a comprehensive modeling and analysis taking these two factors into consideration are proposed. Investigations show that, the envelope resistor and capacitance affects the switching phase delay and the generator's open-circuit voltage while considerable additional phase lag is introduced for charging the switch's parasitic capacitance to turn on the switch. The harvested power is then greatly affected, especially for a piezoelectric generator with a small intrinsic capacitance which is usual for micro-power energy harvesting, i.e., MEMS generators. With the proposed model, better understanding and more precise suggestions on the design of the synchronous harvesting circuit can be found and more accurate performance evaluation can be performed. For instance, the performance degeneration observed with large envelope resistors or small envelope capacitances (see Fig. 9 in [17]) can be well understood, whereas it was not explained by the previous models [16-18].

This paper is organized as follows. Section 2 presents the introduction on the principle and operation of the OSECE and its self-powered realization with the electronic breaker. The Self-powered OSECE (SP-OSECE) circuit is selected here due to the easy feasibility of the self-powered circuit and low load dependence [14]. It thus facilitates the discussion by choosing a constant load without affecting the generality. Section 3 introduces the detailed investigations about the self-powered circuit based on electronic breakers. An improved model is then proposed to study the performance by a thorough analysis on the phase lag and the open circuit voltage as a function of the aforementioned parameters. Then it is validated by experiment and simulation with further discussions presented in section 4. Based on the proposed model, further discussions on the circuit design are performed with guidelines concluded in section 5.

II. Principle and Circuit

A. OSECE circuit

For a sinusoidal excitation $u=u_M sin\omega t$, the short-circuit current from the piezoelectric generator is

$$i_{eq} = \alpha\dot{u} = \alpha u_M \omega \cos\omega t \tag{1}$$

according to the piezoelectric constitution equation. Here, α is the force-factor of the piezoelectric generator and u is the displacement. As a result, the piezoelectric element can be modeled as a current source in parallel with an intrinsic capacitance C_0 and a leak resistor R_0. For the ideal case of no dielectric loss (R_0=∞), the open circuit piezoelectric voltage of the piezoelectric element is expressed as

$$V_p = \frac{1}{C_0}\int i_{eq}dt = \frac{\alpha u}{C_0} \tag{2}$$

Fig. 1 presents the OSECE approach and the corresponding typical waveforms. In this approach, a fly-back transformer composed of three windings L_1, L_2 and L_3 is used with a *1:1:m* turn ratio. Two switches S_1 and S_2 are in series with L_1 and L_2 respectively at the primary side while L_3 is connected to the energy storage element C_r and the load R_L at the secondary side.

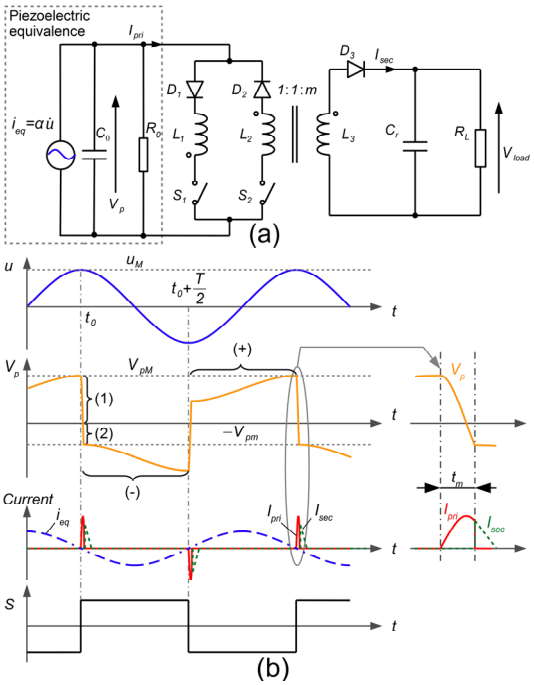

Fig. 1. (a) OSECE approach; (b) Typical waveforms.

The operation principle, detailed in [14], is briefly explained as follows. The switch signal S is applied to two switches at the same time while S_1 and S_2 are closed for positive and negative driving signal respectively. At the beginning, with S_1 opened and S_2 closed, the piezoelectric element is in the open-circuit status due to the diode D_2. The piezoelectric voltage V_p increases with the displacement from $-u_M$ to u_M. S_1 is then closed and S_2 is opened, leading a transient LC oscillation which is further divided into two processes (1) and (2) in Fig. 1. At the end of the process (1) (a quarter of LC oscillation period), most of the electric energy is stored in the transformer without going to the load because the voltage on L_3 is negative and the secondary side is blocked by D_3. At this moment, the current I_{pri} is maximum while V_p equals zero. After that, the circuit enters process (2). C_0 is charged by L_1 along the reversed direction. As soon as $V_p = -V_{pm} = (V_{load}+V_D)/m$, the secondary side is conducted and the remaining energy on the transformer is transferred to the load in the form of current I_{sec}. Next, the circuit enters the half period denoted (-) in which V_p decreases with the displacement towards the negative peak with similar operations.

For each switching, the energy transferred to load is:

$$\Delta E = C_0(V_{pM}^2 - V_{pm}^2)\eta/2 \tag{3}$$

in which the efficiency η is determined by the load and the quality factor related to the dissipative components including the transformer, the switches, the diodes etc. [18] and we have

$$V_{pM} = V_{pm} + \frac{1}{C_0}\int_{-u_M}^{u_M} \alpha\dot{u}du = \frac{V_{load}+V_D}{m} + \frac{2\alpha u_M}{C_0} \tag{4}$$

Then the transferred power is

$$P_h=\omega\Delta E/\pi=\eta f\alpha u_M(V_{load}/m+\alpha u_M/C_0) \quad (5)$$

where $f=\omega/(2\pi)$. Since the voltage is inversed at each displacement peak as shown in Fig. 1 (b), the piezoelectric voltage has the same sign as i_{eq}. Therefore, the output power converted from the vibration by the piezoelectric generator is always positive. It hints that the produced electric energy is completely extracted and not back to the mechanical dynamic system. The inverted voltage after switching is used as a bias for subsequent conversion from mechanical to electrical energy in the generator so that the performance in low coupling cases can be improved.

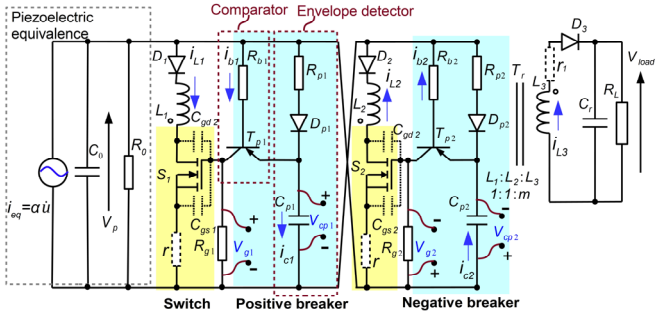

Fig. 2. SP-OSECE approach.

B. Self-powered realization with electronic breakers

In order to implement the OSECE approach for the fully self-powered purpose, the electronic breaker firstly proposed for SSHI in [16] to produce the switching signal is applied to the OSECE circuit as well. The corresponding circuit realization is shown in Fig. 2. Two identical electronic breakers which contain an envelope detector (R_{pi}, D_{pi}, C_{pi}) and a comparator T_{pi} are used for the positive and negative maxima respectively. The MOSFETs highlighted in the yellow box are used as the switches with the parasitic capacitors (C_{gsi}, C_{gdi}) plotted in dashed lines. Considering that the diode's parasitic capacitance is in the pF order and the voltage across the diode is small, it is neglected in the circuit. Different from the usual series resistor to suppress the possible MOSFET gate ringing, two parallel gate resistors R_{gi} are used in consideration of discharging the gate charge in order to turn off the MOSFET before the turning on of the other switch. Therefore, the simultaneously conducting of the two switches can be avoided so as to ensure the proper operation of the circuit. Moreover, the neutralized charge can be decreased correspondingly, which is favorable to the performance. Notably, a frictional series resistor r is added at the primary side to account for the parasitic loss of the switches (conducting resistor $R_{ds\text{-}on}$), the diodes (voltage drop V_D) and the transformer (coil resistance and magnetic loss). Meanwhile, r_1 is added for the loss at the secondary side from the transformer and the diode. The modeling of the transformer is difficult due to the strong nonlinearity. However, in our case, the transformer is assumed to work in the non-saturation region only, thus a simple model can be used with magnetic losses included by r and r_1 as well [26] while the parasitic capacitance is neglected due to the low frequency application. It is reminded that r and r_1 are used only for modeling the losses of circuit, not real components.

According to the working principle introduced before, S_1 and S_2 need to be closed and opened alternatively at the proper displacement extrema. Since the piezoelectric is in open-circuit status except during the inversion process, the breaker detects the voltage peak instead of the displacement extrema by comparing the piezoelectric voltage with the preserved peak in the envelope detector. Due to the similarity, only a half vibration period is considered here while similar results are expected for the other half period. For elaborating on the working process of the self-powered circuit, we can further divide the half vibration period into four phases as shown in Fig. 3. For each phase, the current conducting branches are underlined in black with the current direction indicated by the arrows, while the others are plotted in grey. With the variable symbols defined in Fig. 2, the simulated waveforms by LTSpice© are also presented in Fig. 4 and Fig. 5. As a reference, Fig. 4 (b) plots the experimental and simulated waveforms together, which show good consistence.

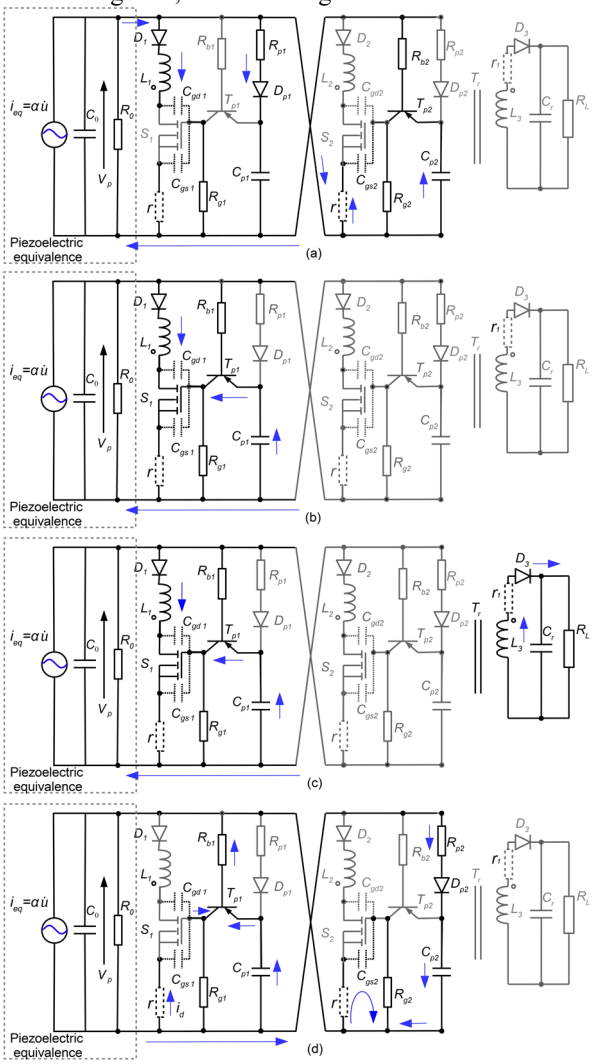

Fig. 3. Four phases of SP-OSECE approach in a half vibration period: (a) Natural charging; (b) Voltage inversion; (c) Energy transfer; (d) Charge neutralization.

Phase 1: Natural charging. The current from i_{eq} charges C_0

towards the maximum V_{pM} as shown in Fig. 3 (a). The envelope capacitor C_{p1} is also charged through R_{p1} and D_1 while C_{p2} and C_{gs2} are charged through T_{P2} and the base resistor R_{b2}. Due to the existence of R_{p1} and D_1, the peak value of V_{cp1} appears later and smaller than V_{pM} with a difference of ΔV_1 shown in Fig. 4. Afterwards, the peak value of V_{cp1} is preserved on C_{p1} while V_p and V_{cp2} start to decline until V_{pM}-ΔV_1-V_{BE} and phase 2 begins. In this phase, the MOSFET parasitic capacitors (C_{gs1}, C_{gd1}) and the gate resistor R_{gi} also bypass a little part of the current i_{eq}.

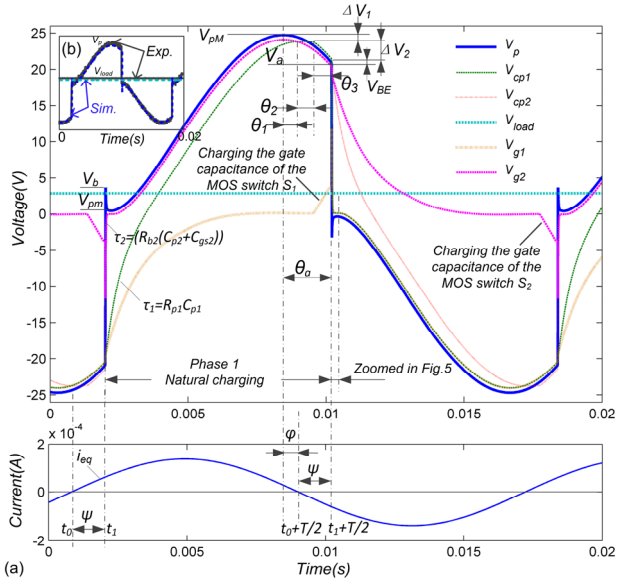

Fig. 4. (a) Simulated waveforms of the SP-OSECE circuit; (b) Comparison of experimental and simulated waveforms Solid lines: experimental; Dashed lines: simulated.

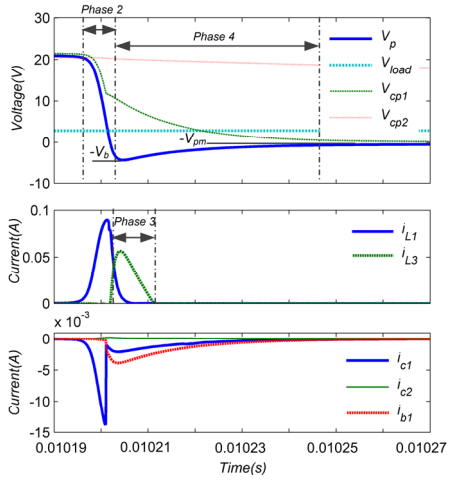

Fig. 5. Zoomed waveforms around the inversion instant.

Phase 2: Voltage inversion. As V_p declines to V_{pM}-ΔV_1-V_{BE} (V_{BE} denotes the transistor base-emitter threshold voltage), the transistor T_{p1} starts to conduct and C_{gs1} is charged by C_{p1}. A voltage drop ΔV_2 on C_{p1} is found in Fig. 4, which hints the charge transfer from C_{p1} to C_{gs1}, also indicated by the collector current i_{c1} of T_{p1} in Fig. 5. As the gate voltage V_{g1} reaches the MOSFET threshold V_{th}, the switch S_1 turns on and C_0 starts a quick discharge from the voltage V_{pM}-ΔV_1-ΔV_2-V_{BE} through the inductive path L_1 as indicated by the current i_{L1} in Fig. 5. Notably, the MOSFET switch undergoes a transition from the linear region (large $R_{ds\text{-}on}$) to the saturation region (small $R_{ds\text{-}on}$), which brings losses in this phase. However, the transition is short since the charging speed gets faster after the voltage inversion begins due to the rapidly increased voltage difference between V_{cp1} (T_{p1}'s emitter) and V_p (T_{p1}'s base). Considering the difficulty to detail the variation of $R_{ds\text{-}on}$, the loss is roughly covered by the friction resistance r.

Phase 3: Energy transfer. When the piezoelectric voltage is reversely charged to $-(V_{load}+V_D)/m$ by i_{L1}, the voltage on L_3 is larger than $V_{load}+V_D$ so that it begins to charge C_r with i_{L3} as shown in Fig. 4 and Fig. 5. Owing to the large value of C_r, V_{load} is almost unvaried so that most of the energy in the transformer goes to the load. To be noted, i_{L1} does not immediately decreases to zero due to the non-ideal transformer and the series resistance r in the circuit. As a result, the piezoelectric voltage continues to decrease until $-V_b$ as seen in Fig. 4, slighly lower than the ideal case $-(V_{load}+V_D)/m$ in Fig. 1. When i_{L1} decrease to zero, S_1 turns off and the inductive circuit is blocked by D_1.

Phase 4: Charge neutralization. After V_p reaches the local negative extreme $-V_b$, some charges are still preserved on C_{p1}, C_{p2} and C_{gs1} with positive voltage V_{cp1}, V_{cp2} and V_{g1} as shown in Fig. 4 and Fig. 5. Consequently, two current paths to balance the voltage between C_{p1}, C_{p2}, C_{gs1} and C_0 are established: (1) C_{p1} (C_{gs1}) → T_{p1}'s emitter (collector) → T_{p1}'s base → R_{b1} → C_0 and (2) C_{p2} → C_0 → R_{p2} → D_2. The waveform of i_{c1} (current from C_{p1}), i_{c2} (current from C_{p2}) and i_{b1} (base current of T_{P1}) are plotted in Fig. 5. i_{b1} has a larger value than i_{c1} due to the current from C_{gs1} flowing through the collector. By observing Fig. 4 and Fig. 5, it can be found that the RC time constant for C_{gs1}, C_{p1} and R_{b1} is small so that V_{cp1} gets close to V_p shortly while the RC time constant for R_{p2} and C_{p2} is relatively larger so that more time is spent for V_{cp2} to get close to V_p. The charge neutralization leads to the piezoelectric voltage retreat towards zero until a new local extreme $-V_{pm}$ as seen in Fig. 5. It is worthy of note that the use of a series resistance R_{p2} makes V_{cp2} changes more slowly than V_p so that the circuit will not trigger the voltage inversion immediately at the negative side. In particular, it helps to reduce the misjudgments about the maximum or minimum that could be caused by the piezoelectric voltage noise induced by high-frequency environmental vibration or switching operation. Moreover, the reversely charged C_{gs2} in the natural charging phase starts to discharge through R_{g2} until zero so that it is easy to be charged by C_{p2} to the turn-on threshold of S_2 with less charge needed.

By carefully observing the circuit and the waveforms in Figs. 3-5, some important facts can be found:

(1) The envelope detectors (R_{pi}, D_{pi}, C_{pi}) which are connected in parallel to the piezoelectric element work as a load beside the leak resistance R_0 and affects the original system bypassing the current out from the source i_{eq}, leading to the magnitude decrease of the voltage in the natural charging phase. The charge neutralization phase after the inversion consumes a part of the charges on the piezoelectric element. It will then also decrease the available piezoelectric voltage peak V_{pM}.

(2) Due to the voltage drop on R_{pi} and D_{pi}, the detected peaks on C_{pi} are lower than the real peaks V_{pM} with the difference of ΔV_1. In addition, there exists a phase lag between the detected peaks to the real peaks.

(3) In order to turn on the switches, the piezoelectric voltage $|V_p|$ is required to be lower than the preserved peak on C_{pi} in order to make T_{pi} conduct, thus C_{pi} can charge C_{gsi}, making $|V_{gi}|$ larger than the threshold V_{th} required to switch on the MOSFET. A significantly phase lag is introduced by this process as seen in Fig. 4. As a result, the voltage inversion happens much later than the ideal case corresponding to the peak piezoelectric voltage. Moreover, it is worthy of note that a minimum requirement on V_{cpi}'s magnitude ($=V_{pM}$-ΔV_1) exists so that V_{gi} are greater than V_{th} after the final balance between C_{pi} and C_{gsi}. The corresponding open-circuit piezoelectric voltage magnitude V_{pM} to trigger the switching action and let SP-OSECE work properly is called the starting voltage.

With the displacement magnitude u_M given, i_{eq} is fixed. The SP-OSECE circuit's harvested power is mainly related to the open-circuit voltage, the switching phase lag and the circuit quality factor for the selected R_L. Considering that the quality factor is mainly determined by the selected components, few efforts can be done except using highly-efficient components to enhance the quality factor as much as possible.

Therefore, the open-circuit voltage and the phase lag induced by the SP-OSECE circuit impose more critical influence on the harvested power. The studies, in which the influence of the envelop resistance R_{pi} is assumed to be negligible, have been performed for SP-SSHI by Liang et al. [17] and for SP-OSCECE by Wu et al. [18] based on the first fact. However, to reject the noises from environmental vibrations or switching operations, R_{pi} is usually selected to be relatively large. More important, the studies [17-18] on the phase lag only considered the voltage drop of the diode and the transistor while the influence of the envelop RC circuit and the charging process of C_{gsi} is probably more relevant as implied by the waveforms in Fig. 4 and Fig 5. Therefore, a thorough analysis taking all the facts into consideration is expected and performed in this study.

III. Analysis

A. Open-circuit Voltage

Without any circuit, the open-circuit voltage magnitude of the piezoelectric equivalence can be written as:

$$V_{oc,org} = \frac{\alpha u_M \omega R_0}{\sqrt{1+\omega^2 R_0^{\,2} C_0^{\,2}}} \text{ and } \varphi_{org} = \tan^{-1}\frac{1}{\omega R_0 C_0} \tag{6}$$

The leak resistance R_0 leads to a magnitude decrease compared with eq. (2) and a phase difference between V_p and u. As the SP-OSECE circuit is applied, the induced open-circuit voltage variation can be analyzed by observing the natural charging phase in Fig. 3 (a). By neglecting the voltage drop on diodes, transistors and inductors and removing the non-conducting branches, the SP-OSECE circuit can be viewed as a parallel connected RC network including R_{p1}, C_{p1}, C_{gd1}, C_{gs1}, C_{gs2}, C_{p2}, R_{b2}, R_{g1} and R_{g2}. Considering the large value of R_{gi} and the small values of C_{gd1} and C_{gs1}, the RC network can be further simplified by excluding these components. It yields:

$$i_{eq} = C_0\frac{dV_p}{dt} + \frac{V_p}{R_0} + C_{p1}\frac{dV_{cp1}}{dt} + (C_{p2}+C_{gs2})\frac{dV_{cp2}}{dt} \tag{7}$$

$$C_{p1}\frac{dV_{cp1}}{dt} = \frac{V_p - V_{cp1}}{R_{p1}} \tag{8}$$

$$(C_{p2}+C_{gs2})\frac{dV_{cp2}}{dt} = \frac{V_p - V_{cp2}}{R_b} \tag{9}$$

Here, the voltage V_{g2} is thought to be the same as V_{cp2} by neglecting the voltage drop on T_{p1}. Then the open-circuit voltage can be obtained by considering the first natural charging phase at the instant where the SP-OSECE circuit is connected to the piezoelectric element with zero initial conditions for V_p, V_{cp1} and V_{cp2}. Applying the Laplace transform leads to the open-circuit voltage V_{oc} and the phase difference φ between V_p and u as

$$V_{oc} = \frac{\alpha u_M \omega}{\sqrt{V_{\mathrm{Re}}^{\,2} + V_{\mathrm{Im}}^{\,2}}} \text{ and } \varphi = \tan^{-1}\left|\frac{V_{\mathrm{Im}}}{V_{\mathrm{Re}}}\right| \tag{10}$$

where

$$V_{\mathrm{Re}} = \omega C_0 + \frac{\omega(C_{gs}+C_p)}{1+\omega^2(C_{gs}+C_p)^2 R_b^{\,2}} + \frac{\omega C_p}{\omega^2 C_p^{\,2} R_p^{\,2}+1}$$

$$V_{\mathrm{Im}} = \frac{1}{R_0} + \frac{\omega^2(C_{gs}+C_p)^2 R_b}{1+\omega^2(C_{gs}+C_p)^2 R_b^{\,2}} + \frac{\omega^2 C_p^{\,2} R_p}{\omega^2 C_p^{\,2} R_p^{\,2}+1}$$

Here, we use the circuit symmetry: C_{p1}=C_{p2}=C_p, R_{p1}=R_{p2}=R_p, R_{b1}=R_{b2}=R_b and C_{gs1}=C_{gs2}=C_{gs}. In comparison with eq. (6), the open-circuit voltage with SP-OSECE gets smaller and the induced phase difference φ is larger as well. In particular, with $\omega(C_{gs}+C_p)R_b<<1$ and $\omega C_p R_p<<1$, we have:

$$V_{oc} \approx \frac{\alpha u_M \omega R_0}{\sqrt{1+\omega^2 R_0^{\,2}(C_0+2C_p+C_{gs})^2}} \tag{11}$$

It can be inferred that the SP-OSECE presents an equivalent effect of increasing C_0 thus decreasing the electromechanical coefficient. With α and u_M unvaried, V_{oc} decreases. Especially, the decreasing effect is more obvious in the case of small C_0 if C_p is comparable. Notably, C_{gs} is taken into consideration in comparison with previous studies [17-18]. With R_{pi} and C_{pi}, the difference between V_{pM} and V_{cpi} is

$$\Delta V_1 = V_{oc} - \frac{V_{oc}-V_D}{\sqrt{1+\omega^2 R_p^{\,2} C_p^{\,2}}} \tag{12}$$

As it has been previously pointed out, for the purpose of switching on the MOSFET, the charge transferred from C_{pi} is required to charge C_{gsi} from zero to V_{th}. Then we must have:

$$C_p(V_{oc}-\Delta V_1) = \frac{C_p(V_{oc}-V_D)}{\sqrt{1+\omega^2 R_p^{\,2} C_p^{\,2}}} > C_{gs}V_{th} + C_p(V_{th}+V_{CE}) + \frac{V_{th}}{4R_g f} \tag{13}$$

in which V_{CE} is the emitter-collector voltage of T_{pi}. It can be noted that V_{CE} will be relatively large for small C_p with weak current corresponding to T_{pi}'s amplification region and close to the saturation voltage V_{CE_sat} for larger C_p with relatively large current. The left side in eq. (13) stands for the charge stored on C_{pi} at the peak amplitude and the right side represents the minimum charge for turning on the MOSFET. The term $V_{th}/(4R_g f)$ is the estimation of the leakage charge through R_{gi} assuming the critical condition that V_{gsi} is linearly increasing to V_{th} for a whole quarter of the vibration period $T/4$. It gives the SP-OSECE's starting condition:

$$V_{oc} > \sqrt{1+\omega^2 R_p^{\,2} C_p^{\,2}}\left(\frac{4fR_g(C_{gs}+C_p)+1}{4fR_g C_p}V_{th} + V_{CE\_sat}\right) + V_D = V_{start} \tag{14}$$

In combination with eq. (11), it is found that C_p and C_{gs} will simultaneously affect both sides of eq. (14), the open circuit

voltage and the starting threshold V_{start}. Moreover, substituting eq. (10) into eq. (14) with the given MOSFETs and transistors, a minimum of displacement amplitude is obtained as the critical starting displacement u_{MC}, which is a function of C_p.

B. Phase lag analysis

Beside the open-circuit voltage, the phase lag induced by electronic breakers in the synchronous switching extracting circuits imposes critical influence on the performance of the generator. The phase lag refers to the delay of the switching action relative to the ideal position of the V_p extreme, which is unavoidable owing to the electronic breaker's principle. When analyzing the phase lag, previous researches [17-18] mainly focused on the voltage drop across the diode and the transistor V_D+V_{BE} corresponding to the conduction of the comparator transistor T_{pi}. In fact, the phase lag is induced by several different aspects. An improved analysis has been performed in this paper and the detailed information is seen in Fig. 4. The total phase lag θ_a can be further divided into θ_1, θ_2 and θ_3. θ_1 stands for the phase lag due to the envelope RC circuit (R_{pi}, C_{pi}) and θ_2 represents the phase lag induced by the well-known voltage drop V_D+V_{BE}. Furthermore, θ_1 and θ_2 can be viewed together as the phase lag induced by the necessary voltage drop ΔV_1+V_{BE} to turn on T_{pi}. After the conduction of T_{pi}, the switch S_i is not turned on until V_{gi} is greater than V_{th}. The charging of C_{gsi} brings the envelope voltage V_{cpi} down simultaneously and induces the additional phase lag of θ_3 as seen in Fig. 4. This voltage drop is estimated as:

$$\Delta V_2 \approx C_{gs}V_{th} / C_p + V_{th}\theta_3 / (\omega R_g) \tag{15}$$

The second term stands for the leakage current on R_{gi} assuming that V_{gsi} is linearly increasing to V_{th}. The total phase lag is

$$\theta_a = \cos^{-1}(1-\frac{\Delta V_1 + V_{BE}}{V_{oc}}) + \theta_3 = \cos^{-1}(1-\frac{\Delta V_1 + V_{BE} + \Delta V_2}{V_{oc}}) \tag{16}$$

Combining eq. (15) and eq. (16), ΔV_2 and θ_a can be solved. It is interesting to find that large C_p will reduce ΔV_2 and diminish the phase lag induced by the C_{gs} charging, but it will lower V_{oc} and increase the phase lag at the meantime. Reversely, small C_p increases the phase lag by higher ΔV_2 but reduces the phase lag by obtaining larger V_{oc}. It implies a complex relationship between θ_a and C_p and an optimal C_p can be found for obtaining a minimum phase lag using eq. (15) and eq. (16).

Using eq. (10) and eq. (16), the phase difference V_p and u is

$$\psi = \theta_a - \varphi \tag{17}$$

C. Efficiency

The energy transfer efficiency η is influenced by many various loss factors from the switches, diodes and the transformers etc. According to the operation principle, η is mainly related to the voltage inversion phase and the energy transfer phase, and it can be written as $\eta = \eta_1\eta_2$. η_1 is the efficiency of the voltage inversion process related to frictional resistance r from the diode, the transformer and the switches and η_2 is efficiency of the transformer's secondary side with r_1 for the transformer and the diode. According to analysis in [14], we have

$$V_b = V_a \cos\lambda e^{-\frac{\lambda}{2Q}} \approx \frac{V_{load} + V_D}{m} \tag{18}$$

for the voltage inversion process. Here, $Q = (L_1/C_0)^{-1/2}r^{-1}$ is the LC circuit quality factor to be determined with experimental identifications for L_1, C_0 and r while λ is the phase angle of the LC oscillation at the end of the voltage inversion. The corresponding current of the secondary side at this instant t_s is:

$$i_{L3(t_s)} = \frac{V_a \sin\lambda e^{-\frac{\lambda}{2Q}}}{m}\sqrt{\frac{C_0}{L_1}} \tag{19}$$

Then the efficiency η_2 can be written as:

$$\eta_2 = \frac{\int_{t_s}^{t_s+\tau} i_{L3}V_{load}dt}{\int_{t_s}^{t_s+\tau} i_{L3}(V_{load}+V_D) + {i_{L3}}^2 r_1 dt} \tag{20}$$

Here, τ is the energy transfer duration. When i_{L3} can be assumed linearly decreasing to zero as implied in Fig. 5, namely, $i_{L3} \approx i_{L3}(t_s)(t\text{-}t_s)/\tau$ for $t_s \le t \le t_s+\tau$, the efficiency can be simplified using eq. (18) and eq. (19):

$$\eta_2 \approx \frac{V_{load}}{V_{load} + V_D + \frac{2}{3}i_{L3(t_s)}r_1} \approx \frac{\kappa m^2 \cos\lambda}{m^2\cos\lambda + \frac{2}{3}\sin\lambda\sqrt{\frac{C_0}{L_1}}} \tag{21}$$

in which $\kappa = V_{load}/(V_{load}+V_D)$. Considering the energy balance and using the efficiency definition, we have

$$\frac{1}{2}C_0({V_a}^2 - {V_b}^2)\eta_1 = \frac{1}{2}L_3{i_{L3(t_s)}}^2 = \frac{1}{2}mL_1{i_{L3(t_s)}}^2 \tag{22}$$

$$\frac{1}{2}\eta_2 L_3{i_{L3(t_s)}}^2 = \frac{{V_{load}}^2}{R_L} \approx \frac{(\kappa m V_b)^2}{R_L} \tag{23}$$

Given a κ (eg., $\kappa \approx 1$ for $V_{load} >> V_D$), we can calculate λ, η_1 and η_2 using the equations (18), (22) and (23). Considering that κ is dependent on V_{load}, a trial value of κ can be firstly assumed for the calculation of η and V_{load}, then κ is updated with the calculated V_{load} and the recalculation of η and V_{load} is performed. The iteration stops with the satisfied accuracy reached. It is reminded that r and r_1 varies with the working conditions in a certain range. However, for convenience, the estimated constant r and r_1 values are often used as an approximation in most cases.

D. Power performance

The power performance of the SP-OSECE circuit is determined by the transferred energy at each switching event, which directly relies on the voltage before and after the inversion, namely, V_a and V_b in Fig. 4. In the corresponding half vibration period from t_1 to $t_1+T/2$, V_p, V_{cp1} and V_{cp2} still satisfy eqs. (7) - (9) with the following initial status:

$V_p(t_1)=V_b$; $V_{cp1}(t_1)\approx -V_a$; $V_{cp2}(t_1)=V_{g2}(t_1)\approx -(V_{pM}-\Delta V_1)C_p/(C_p+C_{gs})$

which can be deduced from Figs. 4-5. Here, the voltage drop on D_1 and R_{p1} is neglected for V_{cp1} while $V_{cp2}(t_1)$ and $V_{g2}(t_1)$ are obtained after charge balance with T_{p2}'s V_{CE} and the leaking effect of R_{g2} neglected. Moreover, V_b can be approximated as V_{load}/m since the difference induced by the non-ideal transformer and diodes is small. As a result, the piezoelectric voltage V_p can be solved directly using eqs. (7) – (9) and the phase relationship is $\omega t_1 = \psi$ for i_{eq}. However, the analytical solution is complex and some simplifications are preferred.

It is observed that the charge neutralization caused by the non-zero initial status is composed of two transient processes of RC discharging corresponding to C_{p1} and C_{p2}+C_{gs}, leading to a

retreat towards zero for V_p as shown in Fig. 4. Generally, we have $\tau_2<\tau_1<<T/2$ and the charge neutralization ends in a short time. Then the retreated extreme V_{pm} is estimated as

$$V_{pm} \approx \frac{C_0 V_b - C_p(V_a + V_{pM} - \Delta V_1)}{C_0 + 2C_p + C_{gs}} \quad (24)$$

using the balance relationship for the total charge on these capacitors. After the charge neutralization, V_p can be assumed to follow the variations of V_{oc} from V_{pm} and we have

$$V_p \approx V_{pm} + V_{oc}(\cos\theta_a - \cos(\omega t + \varphi)) \quad (\psi \le \omega t \le \pi + \psi) \quad (25)$$

Using $V_b \approx (V_{load}+V_D)/m$, it yields

$$V_{pM} = \frac{C_0(V_{load}+V_D)/m - C_p(V_a - \Delta V_1) + (C_0 + 2C_P + C_{gs})V_{oc}(1+\cos\theta_a)}{C_0 + 3C_P + C_{gs}} \quad (26)$$

$$V_a = V_{pm} + 2V_{oc}\cos\theta_a \approx V_{pM} - \Delta V_1 - \Delta V_2 \quad (27)$$

with V_{oc} given by eq. (10). We then have

$$V_{pM} = \frac{\alpha u_M \cos\varphi(1+\cos\theta_a) + C_0(V_{load}+V_D)/m + 2C_p\Delta V_1 + C_{gs}V_{th}}{C_0 + 4C_P + C_{gs}} \quad (28)$$

$$V_a = \frac{2\alpha u_M \cos\varphi\cos\theta_a + C_0(V_{load}+V_D)/m - C_{gs}V_{th}}{C_0 + 4C_P + C_{gs}} \quad (29)$$

using eq. (11) and eq. (12). Therefore, according to eq. (5), the harvested power on the load can be written as

$$P_{SP\_OSECE} \approx \eta f C_0(V_a^2 - (V_{load}+V_D)^2/m^2) \approx \eta f C_0(V_a^2 - V_{load}^2/m^2) \quad (30)$$

by neglecting V_D for the purpose of simplifying the calculation of V_a subsequently. It is logical that $V_D<<V_{load}$ and $(V_{load}+V_D)<<V_a$ are satisfied in the usual case. The ignoring of V_D will not affect the modeling accuracy. Considering $P_{SP\_OSECE}=V_{load}^2/R_L$ for energy balance, it yields

$$V_a \approx \frac{2(C_0 + 2C_P + C_{gs})V_{oc}\cos\theta_a - C_{gs}V_{th}}{C_0 + 4C_P + C_{gs} - C_0\sqrt{\dfrac{\eta f C_0 R_L}{\eta f C_0 R_L + m^2}}} \quad (31)$$

$$P_{SP\_OSECE} = \eta f C_0 m^2 V_a^2/(\eta f C_0 R_L + m^2) \quad (32)$$

Obviously, with the efficiency η, the load R_L and the piezoelectric capacitance C_0 fixed, the harvested power is only related to V_a. Comparing the V_a expression of eq. (31) with V_{pM} of eq. (5) corresponding to the ideal piezoelectric voltage before the inversion, it is found that C_p and C_{gs} increases the equivalent capacitance of the piezoelectric element as implied by the denominators in these two equations. Especially, C_p plays a more important role with a multiplied factor of 4, which differs from previous results with a factor of 2 [18]. This is because the analysis here includes the influence of the charge neutralization of C_p and C_{gs}, which leads to the foreseeable decrease of the available value of V_a. More important, the effectively produced charge in the half vibration period decreases from αu_M to $\alpha u_M\cos\varphi\cos\theta_a$ due to the phase difference between the switching action and the displacement peak (corresponding to i_{eq}=0). The factor $\cos\varphi$ represents the phase difference between u and V_p due to R_0 and the RC network of the SP-OSECE circuit while $\cos\theta_a$ stands for the phase lag induced by θ_1 the RC phase delay (R_{pi}, C_{pi}), θ_2 the voltage drop on diodes and transistors, and θ_3 the switch turning on process. Moreover, the charge $C_{gs}V_{th}$ required to switch on the MOSFET also has to be subtracted. As a result, the accumulated charge corresponding to the numerator in eq. (31) is much lower than the ideal case in eq. (5), leading to a smaller V_a as well.

From the analysis above, it is shown that R_{pi}, C_{pi}, R_{gi}, V_{th} and C_{gsi} impose important effects on V_a and the harvested power. Notably, C_{gs} is always unfavorable to the performance by decreasing V_{oc} and increasing the phase lag θ_a with V_{th} together, thus the MOSFET switches with small C_{gs} and V_{th} are preferred. Meanwhile, the leaking current on R_{gi} prolongs the turning-on time of the switches and increases θ_a as well so that it should be large enough. Yet, it should however satisfy $R_gC_{gs}<T/2$ so as to turn off the switch before the next inversion by discharging C_{gs} in half a period. Due to the more relevant effects, further investigations are focused on R_{pi}, C_{pi}, C_{gsi} and V_{th}.

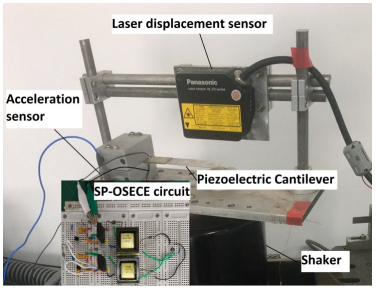

Fig. 6 Experimental set-up.

Table I. Components and Parameters

Definition	Value	Definition	Value
MOSFET (S_i)	IRFP240	R_{gi}	1 MΩ
Transistor (T_{pi})	2N5401	C_{gs}	1.25 nF
Diodes(D_i, D_{pi})	BYV28-100	R_L	100 kΩ
Transformer T_1	WE750811290	V_{th}	3.7 V
C_0	13.75nF	V_D	0.5 V
R_0	5MΩ	V_{CE_sat}	0.3 V
α	0.0003 N/V	r_1	26Ω
R_{bi}	3.3 kΩ	m	1
f	61 Hz	V_{BE}	0.2 V
r	96Ω	L_1, L_2 ,L_3	0.46 mH

IV. RESULTS

In order to validate the developed model, experimental tests are performed on a piezoelectric generator with the SP-OSECE circuit as shown in Fig. 6. The generator fixed on the shaker (2075E-HT, The Modal Shop©)) is composed of a steel cantilever (20mm×100mm×0.6mm) and a piezo ceramic patch (20mm×30mm×0.4mm). A signal generator (DG1032, Rigol©) drives the shaker through a power amplifier with a sinusoidal excitation of 61Hz around the generator's resonant frequency. A laser sensor (HL-C203BE, SUNX©) is used to measure the displacement whose amplitude is kept constant (tuning the driving signal amplitude). The used components and their characteristics are listed in Table I from experimental identifications or factory datasheet. Since the SP-OSECE circuit has low load dependence [15], R_L is fixed as 100k. Due to the difficulty of directly measuring r and r_1, it is estimated by best fitting the results with the model. The maximum efficiency η is measured to be 25.3% which is around the estimated efficiency 23.1% from the model, not so high for the elaborated circuit case in the tests. It is due to the high dissipation of the transformer, the diodes and the transistors in the low load

voltage cases. Meanwhile, the simulation is also performed with the LT-Spice© software with the Spice models obtained by the vendor for the semiconductor components. All the passive components are assumed to be ideal except a series resistance of r_1 assumed for each transformer winding to represent the transformer's losses.

Multiple experiments and simulations have been carried out varying C_p from 0.75 nF to 30.2nF and R_p from 1 kΩ to 1 MΩ while u_M is kept constant at 1.25mm. Fig. 7 presents the harvested power. As seen in Fig. 7 (a), the power first increases then decreases when C_p is increasing. This trend is consistent with the fact that low C_p introduces a significant phase lag for charging C_{gs} as shown in Fig. 8 (a) while high C_p reduces the available V_{oc} and V_a. Thus, an optimal C_p exists for the SP-OSECE circuit performance. Regarding the influence of R_p, the performance decreases as R_p increases as indicated in Fig. 7 (b). It is attributed to the increasing phase delay of the envelope's RC circuit (R_{pi} and C_{pi}) which is seen in Fig. 8 (b). Therefore, R_p always imposes adverse effects on the circuit performance and should be kept as small as possible while preserving the SP-OSECE robustness against noise. Good agreements are found between the analytical results from the proposed model and both experimental and simulated results, as shown in in Fig. 7 and Fig. 8. As a reference, the results using the model which does not consider the phase delay effects of the envelope's RC circuit and the charging of C_{gs} [17-18] are also plotted. The reference model can obviously not predict the performance of the circuit for small C_p and large R_p for which a significant deviation from experimental results is exhibited. Using the reference model, the phase delay estimation remains smaller than experiment as seen in Fig. 8, especially for small C_p and large R_p. Consequently, the power is always over optimistic in these cases as seen in Fig. 7.

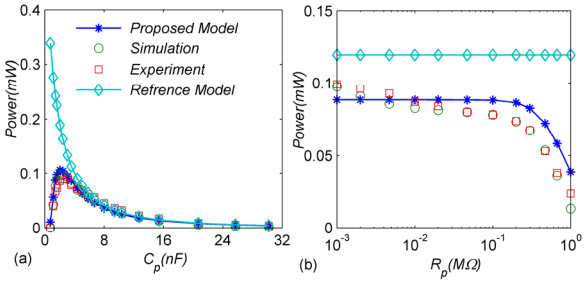

Fig. 7 (a) Power versus different C_p with R_p=4.7 k; (b) Power versus different R_p with C_p=3.4 nF.

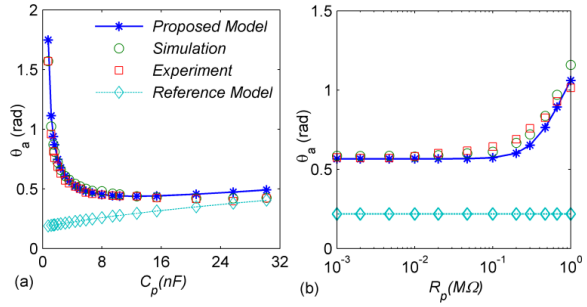

Fig. 8 Phase delay θ_a versus different (a) C_p with R_p=4.7 kΩ and (b) R_p with C_p=3.4 nF.

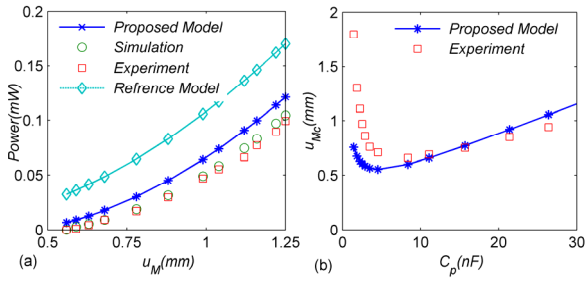

Fig. 9 (a) Power versus displacement magnitude u_M; (a) Critical starting displacement u_{Mc} versus C_p.

Additional investigations have been done to validate the proposed model for different displacement magnitude u_M as shown in Fig. 9 (a) with C_p=3.4nF and R_p=4.7kΩ. Once again, good accordance is found between the proposed model and experiment while the reference model gives overestimated results. Slight difference is observed between the proposed model and experiment for small u_M of 0.6mm where the power is zero in experiment and simulation but nonzero according to the model. The reason is that the critical start displacement u_{Mc} corresponding to the start voltage V_{start} predicted by the model is higher than the measured one for small C_p as shown in Fig. 9 (b). It is induced by using V_{CE_sat} instead of V_{CE} in eq. (14) when calculating V_{start} and u_{Mc}. For small C_p corresponding to T_{pi}'s amplification region (V_{CE}>>V_{CE_sat}), the calculated V_{start} will be smaller than the real one. For relatively large C_p corresponding to T_{pi}'s saturation region, the proposed model gives results close to experiment in Fig. 9(b).

V. Discussion

With the well validated model, further discussions can be performed to give better understanding on the design of SP-OSECE, especially about the critical MOSFET switch. Fig. 10 shows the SP-OSECE circuit's power with the MOSFET switches of varied V_{th} and C_{gs}. For each case, the optimal C_p is used to ensure the best performance while other parameters are listed in Table I. It shows that better results are obtained for the cases with smaller product values of $Q_{gs\text{-}th}$=$V_{th}C_{gs}$ which means less phase delay and smaller optimal C_p, thus higher power. Furthermore, given a constant $Q_{gs\text{-}th}$, a trade-off between V_{th} and C_{gs} is found that the optimal performance is found for moderate C_{gs} and V_{th} as shown by the three marked lines corresponding to the $Q_{gs\text{-}th}$ values of 0.5nC, 1.5nC, and 2.5nC respectively in Fig. 10. If the values of C_{gs} or V_{th} are over bias to one side, the power declines. It can be understood through eq. (15) and eq. (16) that the increase of either V_{th} or C_{gs} will enlarge the phase lag while V_{th} shows more influence. However, C_{gs} affects not only the phase lag but also V_a and V_{oc} directly. Consequently, over bias values of either V_{th} or C_{gs} decreases the power, and the circuit's best performance is obtained for a compromise configuration. Moreover, higher V_{th} imposes more obvious impact on the increase of the start voltage than C_{gs} does according to eq. (14).

In order to detail C_p's influence on the circuit performance, the harvested power by varying C_p and C_0 respectively and keeping the original open circuit voltage $V_{oc,org}$=$\alpha u_M/C_0$ (eq. (6)) constant is plotted in Fig. 11 (a) using the proposed model with the optimal C_p for each C_0 highlighted with pink lines and

circles. It is seen that the performance is strongly related to C_p for small C_0. As C_0 increases, the performance does not change too much for a relatively large C_p range since C_p is much smaller than C_0. Moreover, the optimal C_p increases with C_0 towards a constant as indicated by the pink line with circles. The explanation is that the phase lag from θ_1 the envelope's RC circuit and θ_3 the charging of C_{gs} becomes negligible while C_p affects the performance mainly by decreasing V_{oc}. Fig. 11 (b) shows the power for different C_p and $V_{oc,org}$ with C_0 constant. As $V_{oc,org}$ increases, the optimal C_p decreases towards a constant as well. The results in Fig. 11 (a) and (b) hints that, C_p imposes critical effects on the SP-OSECE circuit by decreasing V_{oc} for high $V_{oc,org}$ and C_0 cases, and by introducing additional phase lag θ_1 and θ_3 for low $V_{oc,org}$ and C_0 cases.

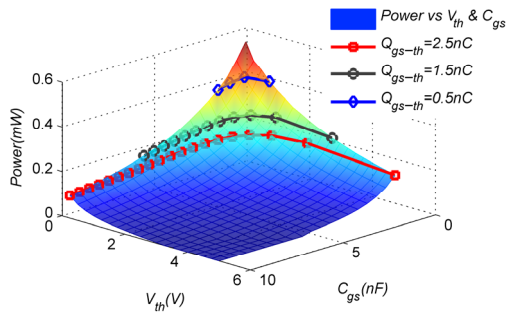

Fig. 10 Power performance versus the MOSFET switches of varied V_{th} and C_{gs}.

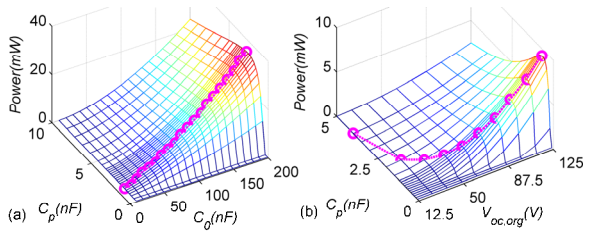

Fig. 11 (a) Power versus C_0 and C_p with $V_{oc,org}$ constant as 37.5V; (b) V_{load} versus u_M and C_p with C_0 constant as 13.75nF.

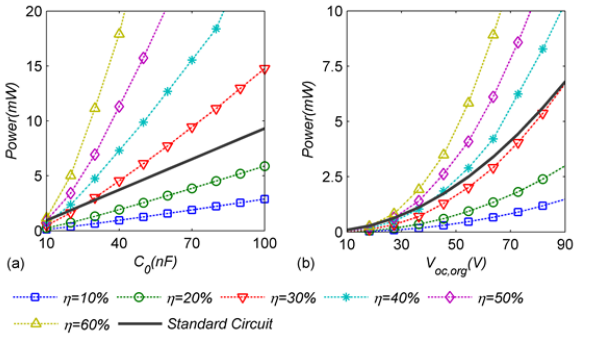

Fig. 12 Optimal power performance comparison between the SP-OSECE circuit and the standard circuit: (a) constant $V_{oc,org}$ = 37.5V; (b) constant C_0 = 13.75nF.

Comparative studies between the classic standard circuit and the SP-OSECE circuit are performed as well. Fig. 12 shows the optimal performance of the standard circuit and the SP-OSECE circuit for the constant $V_{oc,org}$ case (Fig. 12 (a)) and for the constant C_0 case (Fig. 12 (b)) respectively with both circuits well load-matched. The SP-OSECE circuit performance is plotted for six efficiency grades from 10% to 60%. It is seen that the efficiency η is necessary to be larger than a certain threshold so that the SP-OSECE circuit could outperform the standard circuit. As C_0 or $V_{oc,org}$ increases, this efficiency threshold decreases and the SP-OSECE circuit is inclined to achieve better performance easily. It reveals two facts: (1) when it is difficult to achieve the efficiency higher than the threshold, especially for the small C_0 and $V_{oc,org}$ cases, it might be better to use the standard circuit directly; (2) when the proper design for high efficiency by selecting the high quality components, such as the switches with small $R_{ds\text{-}on}$ and the transformer with low losses etc., the SP-OSECE circuit can obtain much better performance than the standard circuit, especially for large C_0 or $V_{or,org}$ cases.

Through the discussions above, it is found that the proposed model can be used as an effective tool for the SP-OSECE design. Some important design rules can be then concluded as follows: (1) adopting the MOSFET switch with small $Q_{gs\text{-}th}$ and $R_{ds\text{-}on}$ as possible while the trade-off between V_{th} and C_{gs} is to be considered with the start voltage covered as well; (2) selecting C_p around its optimal value; (3) enhancing efficiency by using proper components, such as high-quality transformer, low-loss diodes and so on. Besides, according to the former analysis, two addition points can be found: (1) using as small R_p as possible without risking misjudgment on the extreme; (2) using as large R_g as possible while ensuring the discharging requirement of C_{gs}; Moreover, the criterion of using the SP-OSECE circuit or the standard circuit has to be judged by comparing the optimal power utilizing the proposed model.

VI. Conclusion

A comprehensive model has been developed in this paper by including the influence of the electronic breaker and the gate-source capacitance. The phase lag which plays an important role in the circuit performance has been thoroughly analyzed with these factors included. Experimental and simulated studies show that more accurate results can be obtained with this model in comparison with previous studied models. It is especially relevant for micro-power level energy harvesting of the μW order with small piezoelectric capacitance and displacement magnitude, since the phase lag introduced by the envelope detector of the electronic breaker in the form of RC phase delay and the necessary charging time for the gate-source capacitance become significant in this case. In particular, an optimal envelope capacitance exists for the determined piezoelectric capacitance and displacement magnitude. More precise guidelines on the design of the SP-OSECE circuit have been discussed and summarized while the comparison between the standard circuit and the SP-OSECE circuit has been done. It shows that, the SP-OSECE circuit outperforms the standard circuit only if the efficiency is higher than a certain threshold. This threshold decreases as the piezoelectric capacitance C_0 and the original open-circuit voltage $V_{oc,org}$ increases. Finally, it can be pointed out that, despite that the SP-OSECE circuit is used in this paper, the

analysis and the model are also applicable to other self-powered synchronous switching energy harvesting circuit using the electronic breaker approach.

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