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A new method for test chip and single 40nm NOR Flash cell electrical parameters correlation using a CAST structure

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ABSTRACT

In this work we present a method to find a correlation between the measurements on single 40nm embedded Flash memory cell, and the 512kB test chip electrical results. The bridge between these two structures is the cell array stress test (CAST). We are able to simulate the behavior of a 10kb and a 1Mb CAST structures. The parasitic resistances are taken into account, as well as, the testchip distributions for the modeling. The aim is to reduce the time of test obtaining preliminary information concerning the fabrication process and the memory yield at the parametric test level and before the electrical wafer sorting.

INTRODUCTION

As reliability margins are dropping like rocks, an extrinsic approach of embedded Flash memory is compulsory to assess and validate the mission profile and its reliability requirements. To accelerate technology development, single test structure characterizations shall bring preliminary results about the memory extrinsic behaviors which would be confirmed afterward on test chip. In this paper, we propose a method to model the drain current-gate voltage (I_D - V_G) characteristics of a memory cells array using the results obtained on a 512kB test chip. The aim is to predict the distribution of memory cells inside a cell array stress test [1, 2] and its shape (intrinsic and extrinsic population as in [3] or [4]) with a single I_D - V_G characteristic. The measurement are in general impacted by the test structure design [5, 6], thus to reach the goal, we considered the contribution of the CAST access resistance. Moreover we are able to build with our model, the threshold voltage distributions, that can be used for the CAST behavior study.

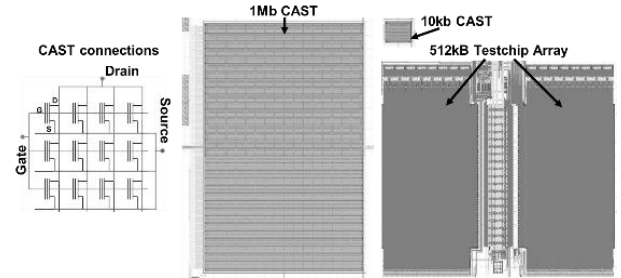


FIGURE 1. From left to right: CAST architecture, 1M cells and 10k CAST devices, and 512kB test chip memory array.

DEVICE DESCRIPTION AND EXPERIMENT

Our memory is a self-aligned polysilicon embedded Flash processed in a 40nm technology node on 300mm wafer. In the CAST structure the cells are connected in parallel and the biasing circuits are not present. Two CAST configurations are used with different size: (i) 1M cells, which represents a quarter of test chip memory capacity, and (ii) 10k cells (Fig.1). Thanks to the arrays architecture, the measurements of one of them can be separated in 4 cell populations, limiting the problem of current compliance and voltage drop during the electrical characterizations. The test chip has been already described in [7]. It contains 512kB of memory with the logic and high voltage circuits needed to access, program, erase and read the memory. Moreover it has all the functions associated to the macrocell testing such as BIST (Built-In-Self-Test), distribution, DMA (Direct Memory Access), internal voltage monitoring. The threshold voltages (V_T) are extracted from I_D - V_G of single cell measurements, while the test chip distribution is obtained by the reading with SPI protocol of a memory array and the application of an analog voltage on the control gate (V_G) of the cells. The switching of sense circuits occurs when $V_T=V_G$, this allows to achieve quickly

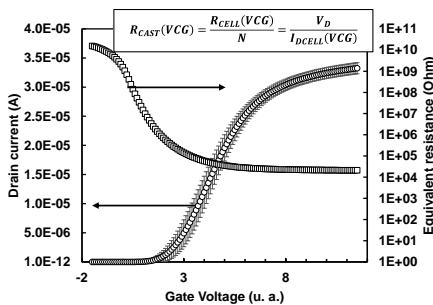


FIGURE 2. Drain current voltage characteristics of 18 single cells used for CAST model. Cell equivalent resistance is then used to compute CAST equivalent resistance depending on N, the number of memory cell in the CAST.

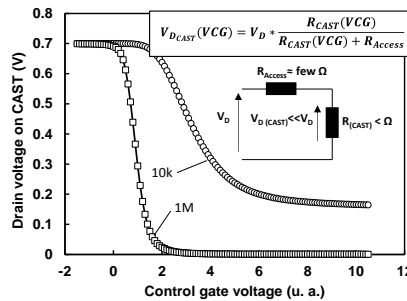


FIGURE 3. Drain voltage drop at CAST contact due to access resistance of metal line and the resulting voltage divider circuit. This result ensues from the fitting of modelled and experimental CAST I_D V_G .

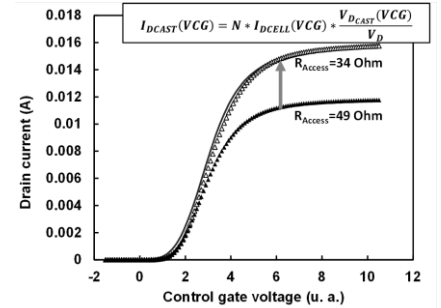


FIGURE 4. CAST drain current is computed considering the drain drop voltage evaluated in Fig.3 and that all CAST memory cell see the same drain voltage. Access resistance calculate by layout and metal lines resistivity is tuned to obtain the same I_D .

the V_T distribution for a large amount of cells.

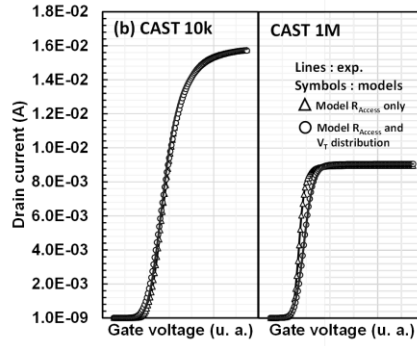
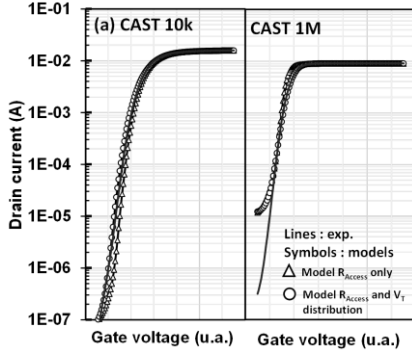


FIGURE 5. Model (symbols) and experimental (lines) drain current of 10k and 1M CAST in log (a) and linear (b) scales. Model with R_{Access} and V_T dispersion reproduce best the knee at high current for 1M and the subthreshold slope of 10k. Around 10^{-5} A, the modelled drain current split from the experiments because of the noise floor of the single cell characteristics used for the model in Fig. 2.

the one of the test chip, the modelling of 1M CAST I_D - V_G results in a distribution with a lower mean V_T and a dispersion larger than

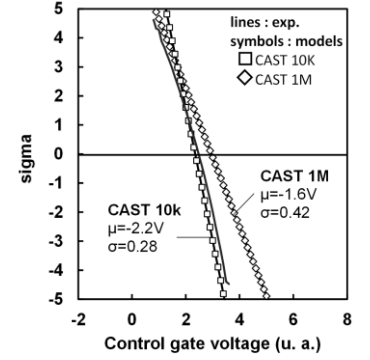


FIGURE 6. Example of V_T distribution from test chip. Gaussian distribution used for fitting 10k and 1M CAST measurements are represented with their parameters. Only 10k CAST results shows a distribution close to the experiments.

CAST CONTACT RESISTANCE MODELLING

First, the goal is to approach the I_D - V_G of CAST with a single memory cell characteristic (Fig. 2). To do that, it is necessary to estimate the internal memory matrix resistances (R_{CAST}). We used the model presented in [5, 6], in order to evaluate the voltage drop at drain and source terminals of all transistors in the array. (Fig. 3). As shown in Fig. 4, the CAST characteristic can be obtained at first approximation, tuning the metal line resistance from the drain and source pads to the memory array (R_{Access}). At this point we have a good fitting between the CAST measurements and simulated I_D - V_G . However the knee around the I_D @ V_T for 1M CAST (Fig. 5a and 5b) is too bent to be simulated by considering only I_D tuning, this effect highlights the approximation at first place of a unique threshold voltage. The same observation can be done on the subthreshold current modelling of 10k CAST (Fig. 5a and 5b).

MODEL WITH THRESHOLD VOLTAGE DISTRIBUTION

To obtain a good agreement between experimental data and simulated I_D - V_G of CAST, it is necessary to take into account the Gaussian distribution of threshold voltage in a large array of memory transistors. Erase threshold voltage distribution are extracted from testchip and modelled as a Gaussian shape distribution (Fig. 6). Then the I_D - V_G is modelled by adding the drain current of each cell V_T pondered by the occurrence of it as described in:

$$I_{DCAST}(VCG) = \sum_{VCGmin}^{VCGmax} f_{VCG=V_T}(VG) * \psi_{VCG} \quad (1)$$

Where ψ_{VCG} represents the Gaussian distribution of V_T from V_{CGmin} to V_{CGmax} and $f_{VCG=V_T}$ is the single cell I_D - V_G shifted to obtain $V_T=V_G$. The modelling gives a perfect reproduction of each region of CAST I_D - V_G without tuning much the distribution parameter as described Fig. 5a and 5b. This is clearly described in Fig. 7(a) and Fig. 7(b), where the log of simulated and experimental drain current tends to follow a linear fits. By introducing the V_T distribution, a best fitting is achieved at low current for 10k (subthreshold area) and at high current for 1M CAST (threshold voltage area). However by looking at the distribution used for fitting in Fig. 5, even if the 10k I_D - V_G modelling uses a Gaussian distribution with parameters near to

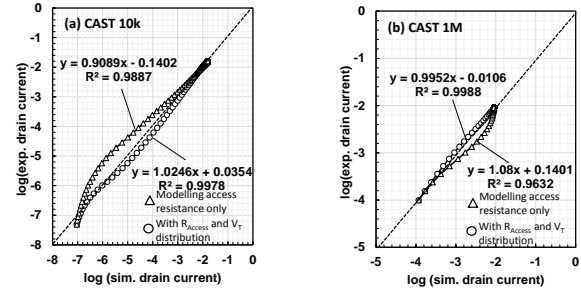


FIGURE 7. Correlation of log of drain current from model and experimental of 10k and 1M CAST device. Ideal correlation is shown in dotted lines. Model with R_A and V_T yields the best fitting for every current magnitude compared to model with R_A only.

expected. Thus, when modelling large CAST such as 1M, the voltage drop on the CAST lines has to be considered as a first-order contributor to the dispersion [6].

CONCLUSION

The Cell Array Stress Test structure is well representative to testchip array and thus it gives useful information about both intrinsic and extrinsic cells population. In this paper, we show that intrinsic erased population can easily be modelled using single cell characterization and the threshold voltage distribution from our 512kB test chip considering the access resistance. However, for large CAST (here 1M cells), the taking into account of the voltage drop inside the array is mandatory to explain the large V_T spread. The next studies will apply this methodologies to write state, CHE programming and the quantification of extrinsic cells.

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