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Low Cost Diode as Selector Device for Embedded Phase Change Memory in Advanced FD-SOI Technology

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Abstract—This paper presents a new diode selector for embedded Phase Change Memory (PCM) in advanced FD-SOI technology. It has been developed to achieve a very low cost selector device but still very efficient to meet PCM specifications. This new device takes all advantages of CMOS in FD-SOI: buried oxide (BOX), shallow trench isolation (STI) and high k metal gates to allow very low leakages between cells, thus offering great potential for designing embedded memory arrays of up to several Mbit. The selector can drive 300 μ A at 2V through the memory cell with 2.5V applied on gates together with a limited leakage current of less than 10pA/cell. The effective cell area of under 0.025 μ m² is very competitive as compared to a MOS selector, offering a size reduction of around 60% for the same driving current. Therefore, the new diode on FD-SOI devices is a great solution for a PCM selector due to its very low cost and high density.

Index Terms—Selector, Phase Change Memory, PCM, PCRAM, RRAM, Diode, FD-SOI, eNVM

I. INTRODUCTION

Since its invention [1], embedded Flash memory has led the market for semiconductor memories. But Flash is now facing increasing complexity regarding CMOS process integration especially with the development of aggressive technology nodes due to its very basic principle based on charge trapping [2]. Therefore, a growing attention in the semiconductor industry has been focused on emerging memories over the last few years, like Magnetic RAM (MRAM), Resistive RAM (RRAM), or also Phase Change Memory (PCM). Their attractiveness arises from the limited number of additional masks needed to integrate them within advanced standard CMOS processes. However, this kind of memory requires a selector to limit leakage currents through sneak paths [3]. Great attention must be given to the selector as it limits the bit cell size and thus directly affects the cost competitiveness. A compromise has to be found when developing a selector: it must be able to deliver sufficiently high programming currents

(for PCM cells, 300 μ A is required during RESET [4]), exhibit low leakage, great reliability and compact size, while keeping cost as low as possible. In this context, we present a new FD-SOI diode developed for this purpose in advanced FD-SOI process technology [5]. The process is very close to standard CMOS FD-SOI, adding only one photolithographic and implant step, limiting integration cost. It also takes advantage of buried oxide (BOX) to decrease leakage currents through bulk.

II. PROCESS INTEGRATION

Figure 1 represents a sample of a memory array architecture layout with a PN diode on FD-SOI as selector device. Along the X direction, each wordline (WL) is surrounded by two bit cells (Fig. 2). Those bit cells correspond to bitlines (BL). Along the Y direction, wordlines are laterally isolated from each other

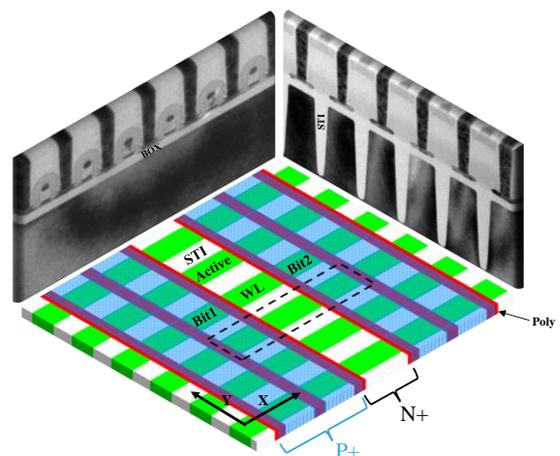


Fig. 1. Diode selector array schematic and TEMs. Cell area is less than 0.025 μ m².

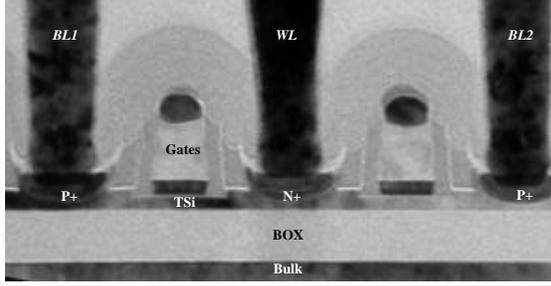


Fig. 2. TEM cross-section of two diodes on FD-SOI devices with BOX, gates and contacts. The two selectors are sharing the same wordline (N+).

by shallow trench isolation (STI). Vertically, they are isolated by the buried oxide from the standard CMOS FD-SOI. Therefore, the above process is fully compatible with a standard CMOS process flow and the memory can be integrated with logic and SRAM in an advanced FD-SOI technology node. Including the WL strap, the effective cell size is under $0.025\mu\text{m}^2$.

In the case of adjacent bitlines along the same wordline, the leakage of the reverse junction is too large for the targeted application. The solution would be to use STI also for longitudinal isolation, which is under development. To get a fully free integration and suppress the additional photo and implant step, we could consider using a specific doping implant included as a flavor of the standard CMOS FD-SOI process. This case will be further evaluated by simulation in this work.

III. POLARIZATION SCHEMES APPLIED ON ARRAYS FOR PROGRAMMING

Figure 3 represents a 4×4 memory array sample featuring 16 cells. The green diode symbol represents the selected cell, orange represents unselected cells on the selected wordline or bitline (referred to as “half-selected cells” in the following), and red represents unselected cells. When a memory cell is selected in programming mode, the diode selector has to be polarized in forward mode to deliver the maximum current through the memory point. Therefore, the selected bitline (*i.e.* the anode of the diode selector) must be polarized to a high voltage while the selected wordline (*i.e.* the cathode of the diode selector) is grounded. Unselected bitlines must be polarized to ground voltage and unselected wordlines must be polarized to high voltage accordingly. Given this polarization scheme half-selected cells are simply grounded. Unselected cells are polarized in reverse mode. As we see in figure 3, if $M \times N$ is the size of the memory array, and there is one selected cell, there are $M+N-1$ half-selected cells and $(M-1) \times (N-1)$ unselected cells. Therefore the number of unselected cells increases together with the memory array size. In this regard, careful attention must be paid to the reverse current when developing a selector for resistive-switching memories.

To determine the polarizations applied on the selector (Fig. 4), we consider that V_{ON} is the required voltage to obtain the maximum PCM programing current I_{ON} . When selected, the

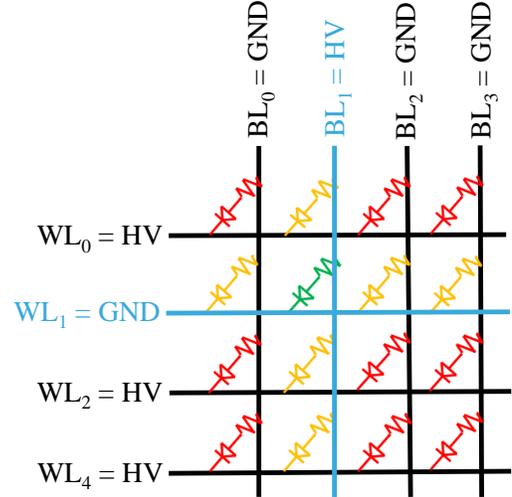


Fig. 3. Example of 4×4 diode and resistive memory array with polarization for selecting a single memory point. Current is driven through the selected cell when it is blocked in half-selected and unselected cells.

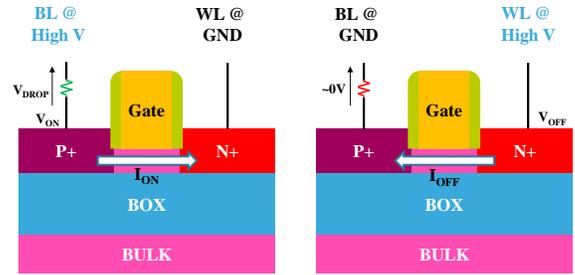


Fig. 4. Schematic illustrating the voltage application to characterize forward and reverse current of the diode selector device.

current I_{ON} generates a voltage drop V_{DROP} on the PCM memory point ($\sim 2\text{V}$ at $300\mu\text{A}$ [4]). As very little current flows through unselected cells (I_{OFF}), the voltage drop across these unselected memory points is negligible. As a consequence, reverse voltage is defined as $V_{\text{OFF}} = V_{\text{ON}} + V_{\text{DROP}}$ (1).

IV. ELECTRICAL CHARACTERISTICS

In conjunction with the buried oxide isolation, allowing for suppression of bulk leakage current, the STI vertical isolation allows bitlines to be fully isolated from each other. The remaining leakages are due to reverse PN junctions. P+ and N+ implants are standard source/drain implants from the CMOS FD-SOI process, and have not been optimized here to minimize leakage or maximize drive current in the selected point. The forward current of the diode is limited by the thickness of the top silicon (TSi). This is directly related to the TSi resistance and highlights the importance of the doping concentration of this region. To reach the $I_{\text{ON}} = 300\mu\text{A}$ required for PCM programming, only a $V_{\text{ON}} = 2\text{V}$ forward bias is required on the selector (Fig. 5). Therefore, with Eq. 1 and $V_{\text{DROP}} = 2\text{V}$, we have $V_{\text{OFF}} = 4\text{V}$. Figure 6 shows reverse current of diode for an

applied voltage from 0V to V_{OFF} . Polysilicon lines were used in the architecture to prevent bitline and wordline shorts during silicidation operation. However, applying a bias on this lines, thus polarizing gates, has been revealed to have a beneficial effect on the diode leakage currents. In figure 7, the diode is reversely biased at $V_{OFF} = 4V$. When applying a 2.5V gate bias the leakage current is reduced by more than 3 decades. It has to be noted that the gate bias doesn't degrade the forward current either (and even increases it a little) (Fig. 8) and no current leaks through gates as thick oxide (GO2 like) is used. Leakage current at this voltage is less than 10pA/cell.

Figure 9 shows the diode response to standard PCM voltage

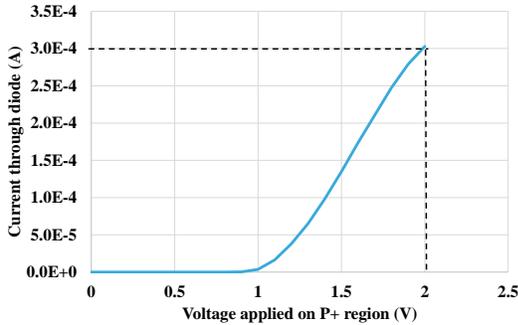


Fig. 5. Forward current through the diode with 2.5V on gate. 300μA are reached at 2V on P+ region.

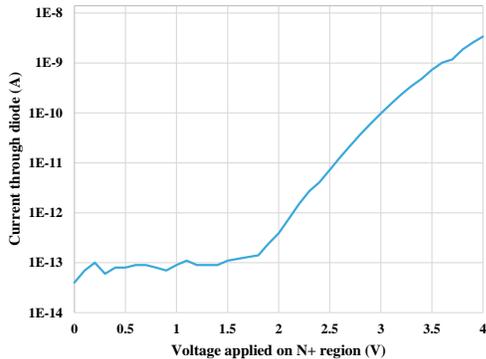


Fig. 6. Reverse current through the diode selector with floating gate. In this condition, leakage at 4V is superior to 1nA.

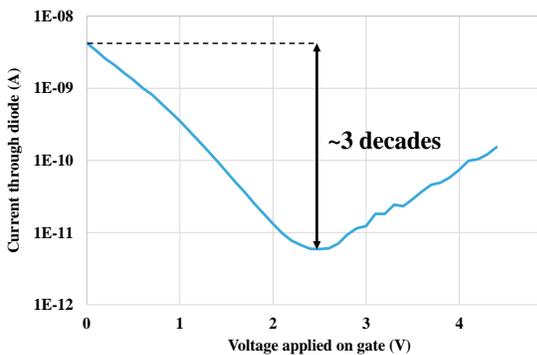


Fig. 7. Influence of gate polarization on reverse current through the diode selector with 4V applied on N+ region. At 2.5V on gate, the leakage is less than 10pA, thus reducing it by 3 decades.

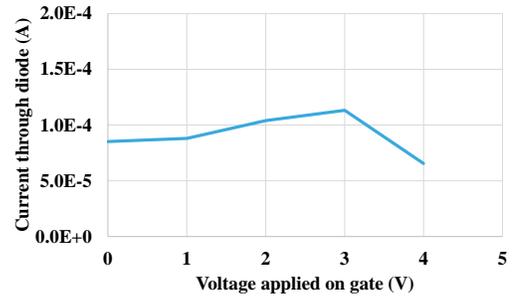


Fig. 8. Influence of gate polarization on forward current through the diode selector with 1.5V applied on P+ region.

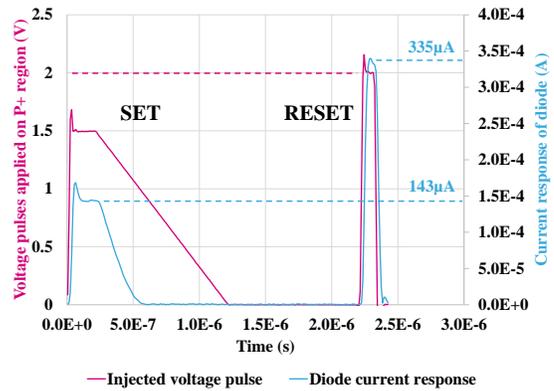


Fig. 9. Current response of the diode to a voltage pulse with PCM characteristics.

pulses applied during SET and RESET operations, and demonstrates that this selector is suitable for such technology.

V. PROCESS AND ELECTRIC SIMULATIONS TO IMPROVE PERFORMANCES AND REDUCE COST

As mentioned before, the additional photo and implant step can be replaced by a specific doping implant included in the standard CMOS FD-SOI process. This solution was evaluated by process and electrical simulations using Sentaurus© tools. Figure 10 compares simulations of the device measured in this paper, which has an additional implant that is not optimized for this device (referred to as “standard implant” bellow), and a device featuring a N-type specific doping implant from standard CMOS FD-SOI process (referred to as “enhanced implant” in the following). It is clear that the specific doping implant enables a reduction of the intrinsic resistance of TS_i. This is confirmed in Figure 11 showing the intrinsic resistance of the two devices, extracted from electric simulations of the forward current. A smaller intrinsic resistance allows for a reduction of the voltage required to reach $I_{ON} = 300\mu A$. Regarding electric simulations, 1.8V are required to obtain 300μA on the enhanced device. Therefore, as V_{OFF} is directly influenced by V_{ON} (Eq. 1), it is reduced proportionally. Furthermore, the reverse current and the optimal gate voltage are also decreased, reducing leakages by about 7% and the optimal gate voltage by about 0.2V at the same reverse voltage (Fig. 12). Finally, this solution offers a cost- and performance-

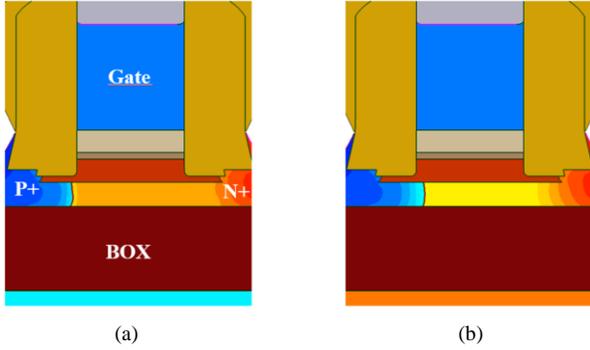


Fig. 10. Process simulation of (a) the enhanced and (b) the standard diode on FD-SOI. The TSi under gate is clearly more doped on the enhanced device, effectively reducing the intrinsic resistance.

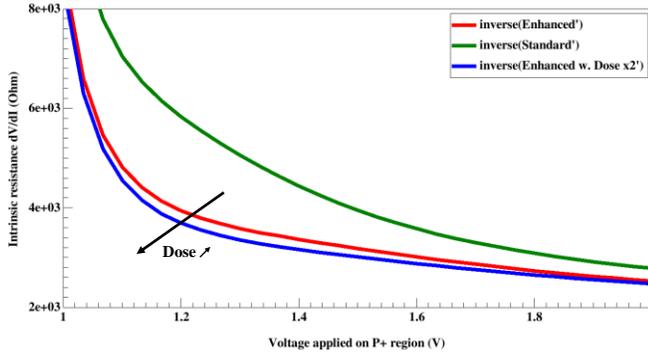


Fig. 11. Intrinsic resistance extracted from forward current simulation. Enhanced device have a smaller resistance than standard.

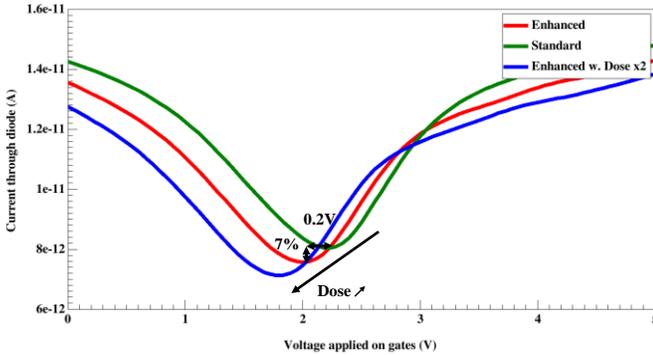


Fig. 12. Simulation of gate polarization influence on the reverse current with 4V applied on N+ region.

competitive and compact selector for embedded PCM memories with CMOS FD-SOI process without violating any design rules.

VI. SELECTOR DEVICE FEATURES SUMMARY

Table 1 reports the main features of the diode selector on FD-SOI (standard and enhanced). A comparison with a standard MOS on FD-SOI is also provided. The enhanced device is clearly more efficient than the standard one in terms of driving current and integration cost. In terms of area, on equivalent performances, the MOS transistor is around 60%

bigger than the diode. However, required voltages are higher on the diode selector but still remain compatible with embedded memory specifications. As compared to other technologies, a PCM cell with a diode on FD-SOI would benefit from smaller dimensions than recently published BEOL or Flash eNVM memories in 28nm [6, 7].

TABLE I. THIS WORK'S DIODES AND MOS ON FD-SOI TECHNOLOGY BENCHMARKING

	Diode on FD-SOI		MOS
	Standard	Enhanced	
Size	$> 0.025\mu\text{m}^2$	$> 0.025\mu\text{m}^2$	$\sim 0.04\mu\text{m}^2$
V_{ON} (@ 300 μA)	2V	1.8V	1.2V
V_{OFF}	4V	3.8V	3.2V
Integration	1 additional mask + 1 additional implant	Free	Free

VII. CONCLUSION

A new low cost, compact and high current selector, suitable for PCM or other unipolar RRAM technology, with an area of less than $0.025\mu\text{m}^2$, has been developed in standard CMOS FD-SOI process. It has been demonstrated by simulation that further improvements can be achieved by replacing an additional implant by an N type counter doping implant included in a standard CMOS FD-SOI process. In addition to the promising performances presented above, these results pave the way to the development of a cost-less selector for advanced embedded non-volatile memories.

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