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# AMS and RF Design for Reliability Methodology

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**Abstract**—The design for reliability concept is already in use on digital circuits, but not systematically in use on AMS or RF circuits. A reliable circuit design demands knowledge of the physical degradation and models to analyze the reliability in earlier stages. Also, it needs to be simple enough to be used on the redesign. In this work, we propose and validate an AMS and RF circuit design for reliability method. In order to investigate our method, we have designed a 5-3 NOR interpolative Digital Controlled Oscillator (DCO) near 1 GHz applications. This design example has presented 1.4% decrease of oscillation frequency, 0.2% decrease of phase noise for a 1 MHz off-set, and 2.1% decrease of power consumption after 10 years of degradation. According with the trends presented in Table I, we estimate that the  $f_{osc}$  ageing degradation was improved of 13 % by applying the design for reliability method.

## I. INTRODUCTION

Technology development often demands electronic products, which are driven by many circuit constraints. The ITRS indicates that reliability will be one of the most important challenges of the semiconductor industry in the following years [1]. Reliability is defined as the ability of a circuit to work in accordance with its specifications over a given period of time and under specified conditions [2].

The performance constraints are usually in terms of area, frequency, bandwidth, power consumption, noise performance, linearity and gain. The stress conditions include temperature, signal swing and bias. Design for reliability means describing the circuit performance by its stress conditions, and finding how to increase the performance and decrease the stress.

The reliability design concept is already in use in digital circuits, but has not been systematically used in AMS or RF circuits. A reliable circuit design demands knowledge of the physical degradation and models to analyze the reliability degradation in earlier stages. Also, it needs to be simple enough to be used on the redesign. In this work, we propose and validate a method of AMS and RF circuit design for reliability.

We start our work reviewing the physical phenomena that degrade the circuit performance and how we can avoid them in Section II. In Section III, we propose a synthesis methodology. This method increases the circuit robustness in terms of reliability analysis and circuit redesign. In Section IV, we explain how the reliability can be analyzed. For this purpose, we describe the performance constraint of the given circuit as a function of the stress condition. In Section V, we validate the developed method with a realistic design of a reliable DCO for near 1 GHz RF applications. In Section VI, we also check the circuit performance results against process variability and reliability trends. Finally, we present the methodology conclusions and perspectives.

## II. PHYSICAL PHENOMENA

The physical phenomena mostly responsible for the ageing degradation in active devices are:

*Hot Carrier Injection (HCI)* - the phenomenon that charges gain sufficient energy to overcome a potential barrier and then migrate to a different area of the device. Such phenomenon occurs at the end of the drain junction of a transistor in saturation, creating many interface traps, which increase the substrate leakage current and cause drain current to decrease. The HCI takes effect when the  $V_{GD}$  is greater than or equal to zero and the  $V_{GS}$  is very high [2]. Therefore, this phenomenon could be avoided if we reduce the time in which the transistors are in strong inversion, by controlling  $V_{GD}$  and  $V_{GS}$ .

*Negative Bias Temperature Instability (NBTI)* - the phenomenon that generates positive charges and interface traps. The NBTI is typically seen as a threshold voltage shift after stress [3]. The threshold voltage degradation can be recovered if the stress is stopped. It means that we can avoid the degradation phenomenon if we increase the ratio between the recovery time and stress time, and control the stress conditions (temperature and gate bias) as well.

*Time Dependent Dielectric Breakdown (TDDB)* - the phenomenon of sudden loss of the layer's insulating properties, where the soft breakdown is more likely causing the circuit to lower its performance. The control of the leakage current leads to a better way of reducing the TDDB probability. Moreover, at lower enough voltage and smaller enough area, the device will show no breakdown before ten years of lifetime [4].

Passive devices have ageing degradation caused by *Electromigration (EM)* - the phenomenon of transport of mass in metals [5]. EM can be avoided by reducing the length of connections and increasing their width. Also, design with non-passive components (e.g. inductor-less radios) is more robust.

## III. DESIGN FOR RELIABILITY METHODOLOGY

The synthesis of a reliable circuit begins with the study of the transistor degradation. The physical phenomena HCI and NBTI were chosen to be the focuses of the proposed methodology. The reason we chose such focuses is because EM can be avoided with inductor-less schematics and careful layout design, and TDDB probability can be reduced by leakage control and careful layout design. The bias and the temperature should be controlled to minimize the HCI and the NBTI degradations. However, they cannot be minimized enough to be neglected because it results in considerable loss of circuit performance. Therefore, the reliability analysis should take the HCI and the NBTI into account.

The HCI degradation can be reduced if the drain current is decreased. However, this is not always feasible, since noise and

output charge represent a more important constraint in most design cases. Regarding the NBTI, a good way to reduce its degradation is to increase the ratio between the recovery time and stress. Indeed, it is not the case of our DCO example, as time constraints are imposed by the speed needs. In order to be reliable, the circuit must follow its performance needs during all lifetime despite HCI and NBTI degradations.

The first step of the design for reliability method is to describe the circuit performance taking into consideration the features related to a chosen device behavior. After that, the maximum performance deviation should be imposed and such constraint should be propagated to behavior degradation. Then, the reliability analysis (detailed in the next section) can be used to describe the performance degradation, pointing out the sensitive devices responsible for the circuit lifetime. The problem can also be described as a minimal circuit lifetime, meaning that the same optimization methodology can be applied to find the circuit performance deviation. Therefore, the methodology considers performance and lifetime needs as constraints that can be adjusted, allowing the designer to indicate which one is more important for each circuit application.

Also, the proposed method can fit quite well the process variability issues. If we consider process variability and reliability, we basically have two different ways to degrade the performance. Both ways can be described as functions of the device parameters. In such case, Monte Carlo simulation predicts the impact of variability issues on the performance, and in the proposed analysis, the impact of reliability issues. With both performance deviations, the designer can find how robust the circuit is and how it can be improved.

The device behavior chosen to model the HCI and the NBTI degradations in this method is the transistor drain current. [2] and [3] show us a good way to represent the physical phenomena, reflecting the design constraints and issues that are relevant to this design methodology.

#### IV. RELIABILITY ANALYSIS

We believe that in near future, reliability analysis tools will be part of the design process as well as the variability tools already are. For an efficient design aiming reliability, the reliability analysis must be placed in early stages and must be connected with the design methodology.

The first analysis step consists in describing the typical environment conditions, such as temperature, signal swing and circuit frequency. After that, the circuit test bench should represent these conditions. The circuit degradation has to be measured by the behavior of the transistor drain current under HCI and NBTI degradations. We chose the transistor drain current because it represents the most important part of the degradation. Also, it is connected to the physics of the degradation phenomena mentioned and to the circuit design method.

The transistor drain current degradation ( $\Delta I_{DS}$ ) will feed the model shown in Figure 1, and such model will replace the corresponding transistor [6]. The aged transistor model is described by:

$$I_{DSaged} = (1 - \alpha)I_{DSfresh}. \quad (1)$$

The  $\alpha$  is calculated from the fresh and the aged simulations.

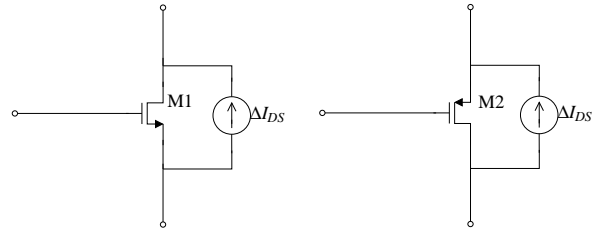


Fig. 1. NMOS and PMOS transistors reliability model for analysis purposes ( $\Delta I_{DS} = \alpha I_{DSfresh}$ ).

As earlier the designer could simulate the cell performance, the better is to evaluate  $\Delta I_{DS}$  degradation. Moreover, such degradation represents the behavior variation that the circuit should be robust to. Thus, the design methodology could predict how much robust the circuit is and if a possible redesign can increase its reliability.

In order to achieve better results, the analysis should be iterated with the design, and this is the core of the design for reliability method. In addition, the circuit performance can be predicted against variability and reliability degradations in the same way.

In this work, we go further to validate the reliability analysis method with the DCO design example. Therefore, the DCO was stressed with different ageing times (1, 5, 10 and 50 years), temperatures ( $-55$  °C,  $27$  °C and  $125$  °C) and digital control words, converted into the analog voltages. The aged DCO oscillation frequency ( $f_{OSC}$ ) was compared with our ageing model result by the error defined as:

$$e = \frac{f_{OSCaged} - f_{OSCmodel}}{f_{OSCaged}}. \quad (2)$$

The DCO was simulated for all these cases, and we found  $\bar{e} = 0.003$  and  $\sigma_e = 0.037$ .

At this point, the analysis did not evaluate the circuit lifetime. In fact, the reliability analysis pointed out the circuit ageing trends, helping the redesign. Therefore, the analysis results (which are the transistors  $\Delta I_{DS}$  degradations) are accurate enough and the reliability analysis could indicate the sensitive devices responsible for the circuit lifetime. The model validation is illustrated in the Figure 2, where  $\bar{e} = 0.004$  and  $\sigma_e = 0.008$ . The DCO was stressed at  $27$  °C during 10 years of degradation in this case.

#### V. DCO DESIGN EXAMPLE

In order to illustrate the reliability design method, we chose a DCO design for radio frequency applications near 1 GHz. The 5-3 NOR interpolative DCO [7] was chosen to generate a frequency clock between 600 MHz and 1.2 GHz. It was designed in CMOS 65 nm. The Figure 3 shows the circuit schematics, where  $V_{CT}$  and  $V_{BIAS}$  are the control words converted into bias voltages for NMOS and PMOS respectively.

For simplicity, we have not considered the variability at this moment. We assume also that only the reliability by the transconductance ( $gm$ ) degradation can change the circuit performance. Then, we iterated the process to find the desired

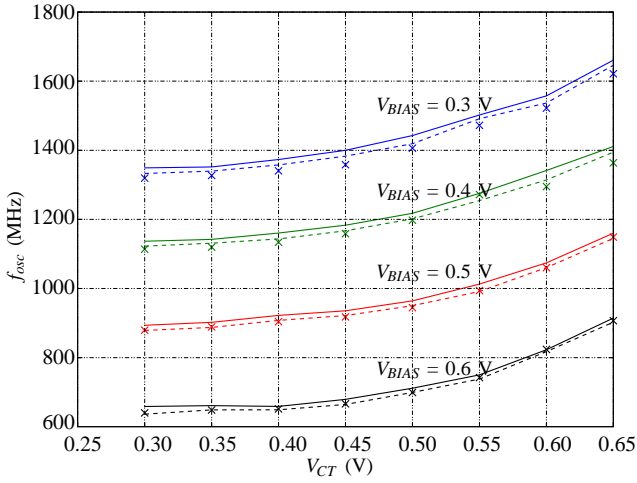


Fig. 2. DCO oscillation frequency ( $f_{osc}$ ) simulated at 27 °C during 10 years of degradation. The result before the stress is represented in the solid line, after the stress it is in dashed line and the aged model is in x marker

performance for a lifetime longer than 10 years. Finally, we evaluated the variability and the reliability for each case.

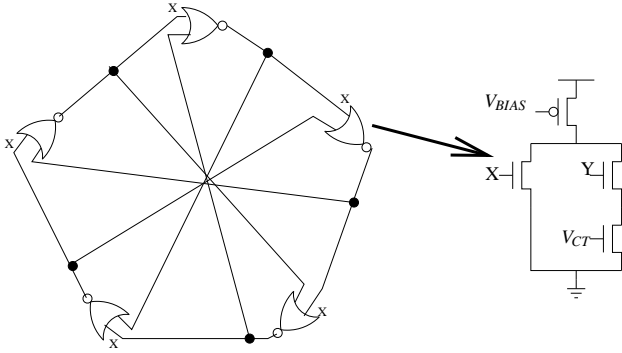


Fig. 3. The 5-3 NOR interpolative DCO schematic [7].

In this circuit, the minimum number of stages is 3 and the maximum ( $N_{max}$ ) is 5, so we have 4 effective stages ( $N_{eff}$ ). The oscillation frequency is

$$f_{osc} = \frac{1}{2N_{eff}t_d}, \quad (3)$$

where  $t_d$  is the NOR cell delay. We found  $80 \text{ ps} < t_d < 200 \text{ ps}$  to the cell delay, which can be described as

$$t_d = \frac{C_L}{gm}, \quad (4)$$

we assume that the delay is the same for all cell both the rise and fall transitions of the signal. Approximately,

$$gm = \frac{2I_{DS}}{V_{ov}}, \quad (5)$$

where  $V_{ov}$  is the overdrive voltage and  $I_{DS}$  is the drain to source current. The  $gm$  is function of the size and the bias, and the charge capacitance ( $C_L$ ) is function of the size only. Therefore,  $f_{osc}$  is a function of  $I_{DS}$ , such as

$$f_{osc} = \frac{I_{DS}}{N_{eff}C_LV_{ov}}, \quad (6)$$

and the current degradation will represent a loss in the oscillation frequency.

The maximum power consumption evaluated as

$$P_{max} = N_{max}I_{BIAS}V_{DD}, \quad (7)$$

is only limited by  $I_{BIAS}$  (assuming constant  $V_{DD}$ ). If the power consumption is optimized, the designer will choose  $V_{DD} - V_{BIAS}$  as low as possible. In this bias condition, the reliability analysis would show lower NBTI degradation. The Figure 4 illustrates the amount of NBTI degradation from years of degradation for each  $V_{BIAS}$ . Clearly, the circuit will present lower NBTI degradation for  $0.5 \text{ V} < V_{BIAS} < 0.6 \text{ V}$  and will consume less power. Aiming to cover the oscillation frequency span, the designer has to choose between accepting the degradation presented in Figure 4 or redesigning the DCO to be reliable. If the reliability and the power consumption constraints are chosen to be optimized, the designer will need an oversized DCO to cover from 600 MHz to 1.2 GHz for  $0.5 \text{ V} < V_{BIAS} < 0.6 \text{ V}$ .

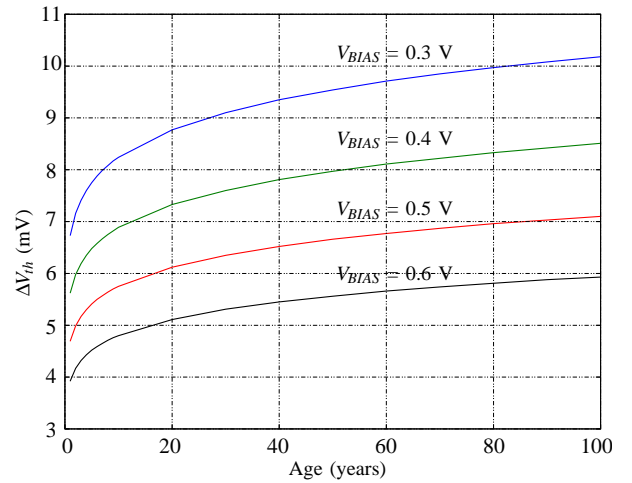


Fig. 4.  $\Delta V_{th}$  degradation for the PMOS DCO transistors stressed by NBTI.

In order to reduce the phase noise, the sizes should be increased. The Table I confirms the phase noise reduction as the NMOS width ( $W$ ) increases, but it also indicates the increase of the oscillation frequency degradation over a 10 years lifetime. If it is reasonable for the target standard, the reliable DCO may have smaller transistors and present more phase noise. Assuming that the phase noise is lower enough for the  $W = 3 \mu\text{m}$  case, the circuit could be designed for better reliability performance. Also, the PMOS width should be 3 times bigger than the NMOS width, in order to generate the DCO clock with an equal duty cycle.

## VI. DCO PERFORMANCE RESULTS

Combining both tendencies indicated by the reliability analysis, the reliable DCO was sized with  $W_{NMOS} = 3 \mu\text{m}$ ,  $W_{PMOS} = 9 \mu\text{m}$  and  $L = 0.5 \mu\text{m}$  to cover from 600 MHz to 1.2 GHz for  $0.5 \text{ V} < V_{BIAS} < 0.6 \text{ V}$ . The DCO consumed  $850 \mu\text{W}$  of power without stress and  $832 \mu\text{W}$  after 10 years of stress degradation.

Then, we considered the circuit variability test bench, by performing 1000 points of Monte Carlo simulation for the

TABLE I

PHASE NOISE AT 1 MHz OFF-SET AND ITS CUT-OFF FREQUENCY ( $f_c$ )  
VERSUS THE OSCILLATION FREQUENCY DEGRADATION ( $\Delta f_{osc}$ ) AT 10 YEARS  
LIFETIME FOR EACH DESIGN SIZING.

| W ( $\mu\text{m}$ ) | $\Delta f_{osc}$<br>@ 10 years | L(1.0 MHz)<br>@ 1 GHz (dBc/Hz) | $f_c$ (kHz) |
|---------------------|--------------------------------|--------------------------------|-------------|
| 5                   | 1.6%                           | -94.3                          | 10.3        |
| 4                   | 1.5%                           | -93.4                          | 11.4        |
| 3                   | 1.4%                           | -92.3                          | 13.2        |

reliable DCO programmed at  $f_{osc} = 1$  GHz, stressed at  $27^\circ\text{C}$ . And for the reliability-variability test bench, we simulated the reliable DCO at the same conditions with the ageing model (presented in Figure 1) extracted from the nominal run for 10 years of stress. We analyzed the mean ( $\mu$ ) and the standard deviation ( $\sigma$ ). We found the probability density function related to circuit variability simulation pointed out  $\mu = 1.017$  GHz and  $\sigma = 97.5$  MHz. The reliability-variability simulation pointed out  $\mu = 1.000$  GHz and  $\sigma = 96.3$  MHz. The Figure 5 illustrates the probability density function related to circuit reliability-variability simulation, clarifying that the reliability has no significant impact compared to the variability, and therefore it could be neglected in our example.

Next, we simulated the reliable DCO phase noise performance for  $f_{osc} = 1$  GHz, shown in Figure 6. We found -92.5 dBc/Hz of phase noise for a 1 MHz off-set and  $f_c = 13.1$  kHz (cut-off frequency). The DCO figure of merit [1] was evaluated as  $2.0 \cdot 10^{18} \text{ J}^{-1}$  before stress and  $2.1 \cdot 10^{18} \text{ J}^{-1}$  after 10 years of stress, assuming no degradation of the phase noise.

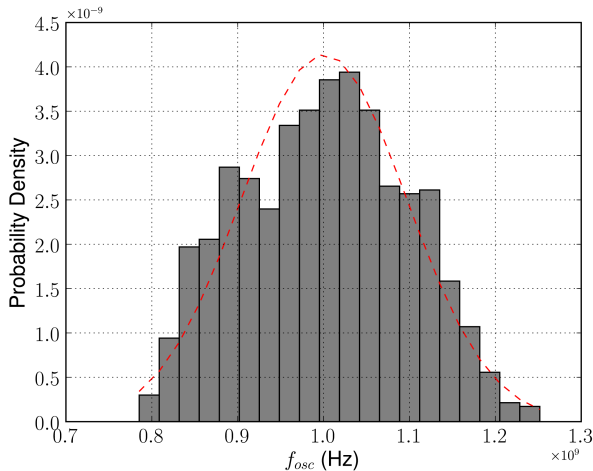


Fig. 5. The circuit reliability-variability performance deviation, simulated from the reliable DCO with the ageing model for 10 years of stress at  $f_{osc} = 1$  GHz by 1000 Monte Carlo runs.

## VII. CONCLUSIONS

In this work, we proposed the design for reliability method developed for AMS/RF circuits. First, we introduced the physical phenomena context and how they could be avoided. Next, we presented the design for reliability method and validated its reliability analysis model. We checked that the reliability

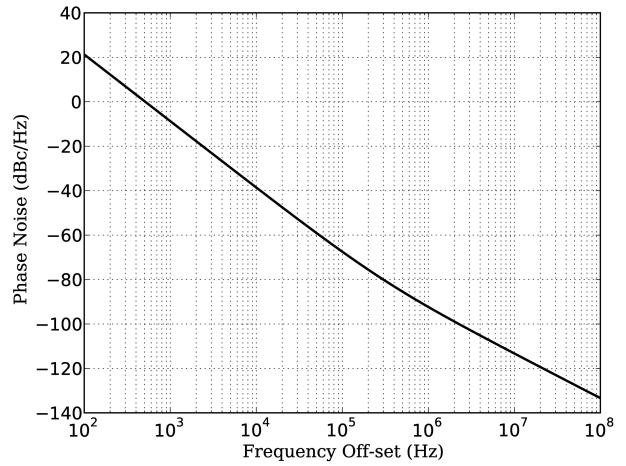


Fig. 6. The phase noise performance, simulated for  $f_{osc} = 1$  GHz.

analysis feedbacks the method and lets a more reliable circuit to be designed. In this context, the reliability became a constraint into the design. The presented methodology might play with the reliability circuit constraint, showing how to optimize it and exposing its advantages and disadvantages.

In order to investigate our method, we have designed a 5-3 NOR interpolative DCO near 1 GHz applications. The reliable DCO design example has presented 1.4% decrease of oscillation frequency and 2.1% decrease of power consumption after 10 years of degradation. According with the trends presented in Table I, we estimate that the  $f_{osc}$  ageing degradation was improved of 13 % by applying the design for reliability method.

Going further, we can say that the design for reliability methodology can be exploited in the architecture level. Also, the architecture performance can be described by each circuit behavior, and the variability or reliability issues can be propagated to the architecture. Therefore, the architecture robustness as well as each circuit robustness can be analyzed and improvements may definitely be found.

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