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WLAN/WiMAX RF Front-End Reliability Analysis

Pietro M. Ferreira, Hervé Petit and Jean-François Naviner
Institut TELECOM ; TELECOM ParisTech ; CNRS LTCI ; ParisTech
maris@ieee.org,(herve.petit,jean-francois.naviner)@telecom-paristech.fr

Abstract—Circuit ageing degradation is becoming worse in advanced node technologies, where low power and low cost RF front-end should be implemented. Thus, reliability is one of the most important challenges. In this work, we analyze a WLAN/WiMAX RF front-end architecture reliability with a behavioral description language (VerilogA) using a top-down approach. We have found the sensitive building blocks and the worst performance variations. We pointed out the programmable gain amplifier (PGA) as the most sensitive building block. The PGA failure is responsible for the degradation of the gain, the noise, and the linearity of the architecture. In low frequency signals, the digital controlled oscillator (DCO) becomes the dominant source of noise degradation.

I. INTRODUCTION

A low power and low cost WLAN/WiMAX RF front-end needs more advanced CMOS technologies for electronic circuit integration. Circuit ageing degradation is becoming worse in these technologies, while application fields like military, medical and aerospace demand more reliability. Thus, reliability is one of the most important challenges of the semiconductor industry. Reliability is defined as the ability of a circuit to work in accordance with its specifications over a given period of time and under specified conditions [1].

Circuit performance criteria are usually in terms of area, frequency, bandwidth, power consumption, noise performance, linearity and gain. The ageing stress conditions include temperature, signal swing and bias. Design for reliability in an architectural level is describing the building blocks performance variations, and finding how to increase the architecture performance and to point out the sensitive building blocks.

The reliability concept is more and more used in digital circuit design [2], but has not been systematically used in AMS or RF circuits [3]-[5]. In order to design a reliable architecture, we need knowledge of the physical degradation for all building blocks and models to analyze the reliability degradation in earlier stages. In the top-down approach, the challenge is to choose the budget for all building blocks taking the reliability degradation into account.

In this work, we analyze the reliability of a WLAN/WiMAX RF front-end architecture using the method of AMS and RF circuit design for reliability [5]. For this goal, we will explore this method in the top-down approach with a behavioral description language (VerilogA). We will point out the sensitive building blocks and find the worst performance variations.

We start our work reviewing the physical phenomena that degrade the circuit performance and seeing how we can avoid them (in Section II). In Section III, we explain how the architecture reliability can be analyzed. Subsequently, we describe the chosen WLAN/WiMAX RF front-end architecture (Section

IV) and discuss the analysis results (Section V). Finally, we present our conclusions.

II. PHYSICAL PHENOMENA

The design of a reliable architecture begins with the study of the building blocks' ageing phenomena. The building blocks are often designed in CMOS, where the physical phenomena mostly responsible for the ageing degradation are:

- *Hot Carrier Injection (HCI)* - the phenomenon that charges gain sufficient energy to overcome a potential barrier and then migrate to a different area of the device [6]. Such phenomenon occurs at the end of the drain junction of a transistor in saturation, creating many interface traps, which increase the substrate leakage current and cause a drain current decrease.
- *Negative Bias Temperature Instability (NBTI)* - the phenomenon that generates positive charges and interface traps. The NBTI is typically seen as a threshold voltage shift after stress [7]. The threshold voltage degradation can be recovered if the stress is stopped.
- *Time Dependent Dielectric Breakdown (TDDB)* - the phenomenon of sudden loss of the layer's insulating properties, where the soft breakdown is more likely causing the circuit to lower its performance [8].

Passive devices have ageing degradation caused by:

- *Electromigration (EM)* - the phenomenon of transport of mass in metals [9]. This erosion effect causes the stressed conductor fails.

The focus of this article is on the physical phenomena HCI and NBTI. The reason for this choice is that EM can be avoided with inductor-less schematics and careful layout design, and TDDB probability can be reduced by leakage control and careful layout design. The bias and the temperature should be controlled to minimize the HCI and the NBTI degradations. However, they cannot be minimized enough to be neglected because it could result in considerable loss of the block performance. Therefore, the reliability analysis should take the HCI and the NBTI into account.

The HCI degradation can be reduced if the transistor bias currents are decreased. However, this is not always feasible, since noise and output charge represent a more important constraint in most of building blocks. Regarding the NBTI, a good way to reduce its degradation is to increase the ratio between the recovery time and the stress time. However, it is not the case in the blocks controlled by a clock, as time constraints are imposed by the speed needs. In order to be reliable, the architecture must fulfill its performance needs during all lifetime despite HCI and NBTI degradations.

III. ANALYSIS METHODOLOGY

We believe that in the near future, reliability analysis tools will be part of the design process in the same way that the variability tools already are. The reliability analysis must be placed in early stages and must be connected with the design.

The reliability analysis is applied at the building blocks hierarchical level [5]. The behavior chosen to model the ageing degradations for each performance Φ , can be shown as

$$\Phi_{aged} = \Phi_{fresh} - \Delta\Phi. \quad (1)$$

The frequency, bandwidth, power consumption, noise, linearity and gain performances of the blocks are estimated by simulation. And then, the $\Delta\Phi$ variations are evaluated by the reliability analysis tools, and they are described by the equation (1). Thus, our analysis consists of evaluating the $\Delta\Phi$ impacts in the whole architecture performance, and pointing out the sensitive blocks.

The most important step is describing the typical environment conditions, such as temperature, signal swing and circuit frequency. In order to obtain a consistent model, the architecture test bench should represent these stress conditions. Thus, the building block degradation is simulated under these environment conditions. By the chosen behavior of the lower level under HCI and NBTI degradations [5], all $\Delta\Phi$ margins are extracted. The building block failure is defined as a Φ degradation big enough to overcome a $\Delta\Phi$ margin.

The earlier the designer can simulate the block performance, the better it is to evaluate $\Delta\Phi$ degradation. Moreover, such degradation represents the behavior variation that the building block should be robust to. Thus, our analysis methodology could predict how robust the architecture is and if a possible redesign can increase its reliability. In order to achieve better results, the analysis should be iterated with the design.

IV. WLAN/WiMAX RF FRONT-END ARCHITECTURE

In this work, we propose to exploit the design for reliability methodology in the architecture level. Also, the architecture performance can be described by each circuit behavior, and the reliability issues can be propagated to the architecture. Thus, the robustness of both the architecture and its circuits can be analyzed and improvements may be found.

With this purpose, we will analyse the RF front-end, presented in the Figure 1, for WLAN/WiMAX applications [10]. The RF front-end architecture specifications are summarized in the Table I. We implement our method in the top-down approach with a behavioral description language (VerilogA).

TABLE I

RF FRONT-END ARCHITECTURE SPECIFICATIONS FOR WLAN/WiMAX APPLICATIONS.

Operational Frequency	1 GHz - 6 GHz
Bandwidth	> 20 MHz
Gain	> 30 dB
NF	3.5 dB @ 1 GHz - 6 dB @ 6 GHz
IP3	< 0 dBm
S11	< -10 dB

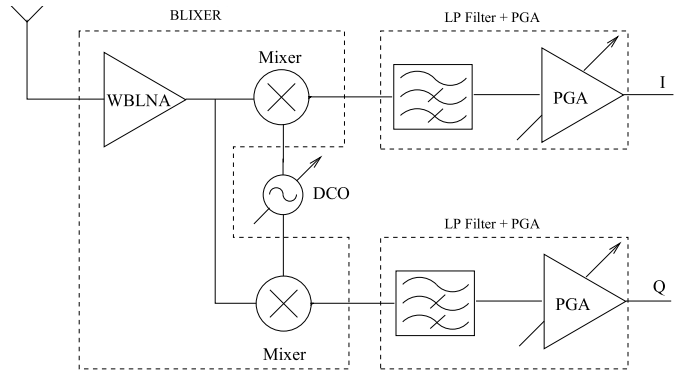


Fig. 1. RF front-end architecture for WLAN/WiMAX applications: illustration.

The WLAN/WiMAX budget will be separated between three main blocks: the BLIXER [11], aggregating a balun, a wide-band low noise amplifier (WBLNA), and a mixer; the digital controlled oscillator (DCO), and the programmable gain amplifier (PGA) together with the low-pass filter. The BLIXER will be modeled with 14 dB of gain (G) for an output bandwidth (BW) limited to 100 MHz (single pole filter model), with 3.5 dB of noise figure (NF), and with 1.1 dBm of 3rd harmonic interception point (IP3). Input matching impedance and the mismatch between I and Q channels will not be modeled at this work. The DCO will be modeled with -2 dBm of output power (P_{io}), and with -120 dBc/Hz of phase noise for 1 MHz (L(1 MHz)) at 5 GHz of operational frequencies (f_{io}). We assume that a ideal PLL will control the oscillator in a fixed frequency point. The PGA will be modeled with 20 dB programmable gain by 2 bits in 25 MHz of bandwidth (single pole filter model), with 30 dB of NF, and with -10 dBm of IP3.

The building block failure margins are a function of the stress time and environment conditions, and they depend on the schematic used in the level below (transistor level). However, we arbitrarily choose the failure margins in order to analyze the building block sensitivities. The BLIXER block failure is defined by:

- $\Delta G = -3$ dB,
- $\Delta NF = 1$ dB,
- $\Delta IP3 = 1$ dBm, and
- $\Delta BW = 50$ MHz.

The DCO block failure is defined by:

- $\Delta P_{io} = -3$ dBm,
- $\Delta L(1MHz) = 10$ dBc/Hz, and
- $\Delta f_{io} = 0$ (by a ideal PLL).

The PGA block failure is defined by:

- $\Delta G = -3$ dB,
- $\Delta NF = 10$ dB,
- $\Delta IP3 = 1$ dBm, and
- $\Delta BW = 10$ MHz.

V. ANALYSIS METHODOLOGY AND RESULTS

The WLAN/WiMAX front-end architecture, modeled in VerilogA, was simulated in SpectreRF (CADENCE simulator) for fresh circuit test and degraded test cases. We propose to

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investigate the architecture performance degradation for eight test cases, composed by the cases: no failure, each block failure, the combinations of two blocks failure, and the failure of all blocks together. The test cases are summarized in the Table II.

TABLE II
FAILURE TEST CASES APPLIED TO THE RF ARCHITECTURE (FIGURE 1).

Case	PGA failure	DCO failure	BLIXER failure
no failure	no	no	no
test 1	no	no	yes
test 2	no	yes	no
test 3	no	yes	yes
test 4	yes	no	no
test 5	yes	no	yes
test 6	yes	yes	no
test 7	yes	yes	yes

The circuit power consumption decreases with ageing degradation [12]. The architecture power consumption is

$$P = P_{BLIXER} + P_{DCO} + P_{PGA}, \quad (2)$$

and we found that the architecture P also decreases by

$$\Delta P = \Delta P_{BLIXER} + \Delta P_{DCO} + \Delta P_{PGA}. \quad (3)$$

Thus, the power consumption reduction is a measure of the ageing degradation in the architectural level, because the ageing phenomena reduces the bias current of the transistors [5].

The architecture gain in dB is

$$G = G_{BLIXER} + A_{LO} + G_{PGA}, \quad (4)$$

where G_{BLIXER} and G_{PGA} are the gain of the BLIXER and of the PGA, and

$$A_{LO} = \frac{V_{LO}}{V'_{LO}}. \quad (5)$$

In the Equation (5), V_{LO} is the DCO amplitude of the test case and V'_{LO} is the amplitude of the nominal case. The degradation of the architecture gain is equally sensitive to ΔG_{BLIXER} , ΔA_{LO} , and ΔG_{PGA} . The ageing degradation, measured by the power consumption reduction, decreases the architecture gain in the same way. The gain decrease can be estimated by the power consumption reduction.

The architecture gain degradation is shown in the Figure 2 with the no failure case in solid line, the BLIXER failure case with dashed line, the DCO failure case with dotted line, and the PGA failure case with square marks. The failures obtained from the combination of blocks are shown with the combination of failure representations (eg. the BLIXER and PGA failures are represented with dashed line and square marks). The test cases were referred in the Table II. The PGA failure has presented the bigger gain degradations among all test cases. The PGA block failure has the biggest impact on gain degradation, and moreover we lost the gain programming. The BLIXER and the DCO failure combination also can reduce the gain under the specification. The architecture bandwidth is reduced as the gain is. Thus, the gain and bandwidth reliability are mostly determined by the PGA reliability.

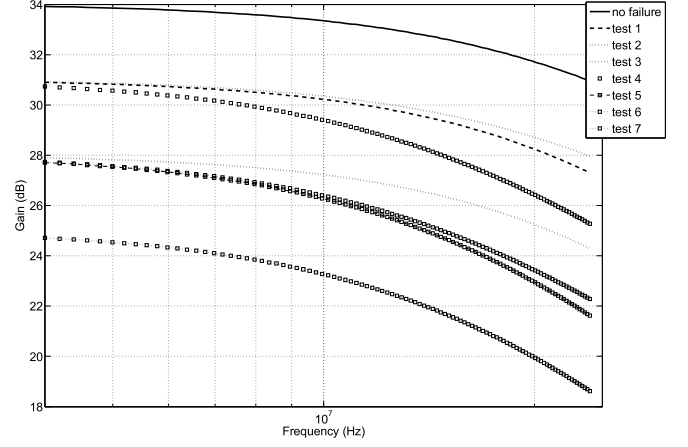


Fig. 2. The architecture gain degradation: no failure case in solid line, the BLIXER failure case in dashed line, the DCO failure case in dotted line, and the PGA failure case with square marks.

The architecture noise performance is analyzed by the power of the output noise due to the circuit noise sources and by the power of the output noise due to the input noise source. The architecture NF is evaluated by the power spectral density into the band of the signal propagating noise sources to the output. The main noise sources analyzed are the phase noise and the amplifiers NF, and in this case we take into account that the PGA is an unmatched stage. We found that the flicker noise coming from the DCO impacts the lower frequency baseband signals. And, the BLIXER's and PGA's NF are dominant for higher frequencies by the Friss formula relationship

$$\lim_{f \rightarrow BW} F = F_{BLIXER} + \frac{F_{PGA} - 1}{G_{BLIXER} A_{LO}}, \quad (6)$$

where F_{BLIXER} , F_{PGA} are the block's noise factor ($NF = 10 \log(F)$), and G_{BLIXER} , A_{LO} are in V/V.

The architecture NF degradation is presented in the Figure 3 with the no failure case in solid line, the BLIXER failure case with dashed line, the DCO failure case with dotted line, and the PGA failure case with square marks. The failures obtained from the combinations of blocks are shown with the combination of failure representations (eg. the BLIXER and PGA failures are represented with dashed line and square marks). The test cases were referred in the Table II. The PGA failure has presented the bigger noise degradations. Moreover, if there is another failure combined, the PGA noise degradation is increased as predicted in the Equation (6). The result presented in the Figure 3 also confirms the dominant sensitivity of the architecture's NF by the DCO in lower frequency signals. Thus, the architecture NF reliability is also a big constraint in single failures test cases.

The architecture linearity is analyzed by its

$$IP3 = \frac{1}{\sqrt{\frac{1}{IP3_{BLIXER}^2} + \frac{G_{BLIXER}^2 A_{LO}^2}{IP3_{PGA}^2}}}, \quad (7)$$

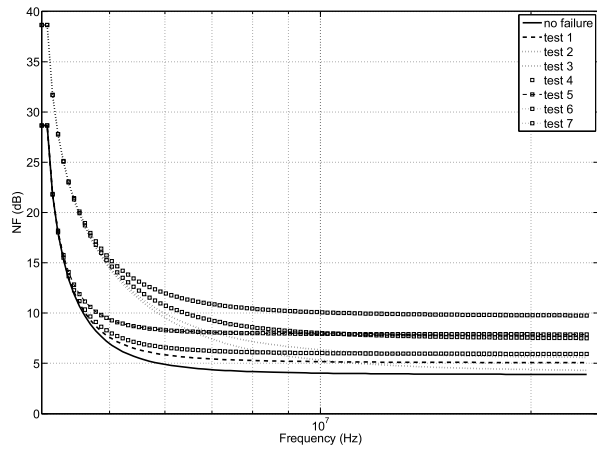


Fig. 3. The architecture NF degradation: no failure case in solid line, the BLIXER failure case in dashed line, the DCO failure case in dotted line, and the PGA failure case with square marks.

where $IP3$, $IP3_{BLIXER}$, and $IP3_{PGA}$ are expressed in milliwatts; and G_{BLIXER} , A_{LO} are in V/V. As the power consumption is reducing, the transistors will present a more linear and a smaller transconductance. The ageing degradation increases the architecture linearity by increasing its $IP3$.

The architecture $IP3$ degradation is presented in the Figure 4 for all test cases. The results present the BLIXER failure as the most sensitive block, increasing in $\Delta IP3 = 1$ dBm. Moreover, the $IP3$ increase does not characterize an architecture failure as a bigger linearity is desired. However, the PGA failure reduces the architecture $IP3$ (eg. $\Delta IP3 = -0.01$ dBm at Figure 4). This $IP3$ reduction could compromise the architecture reliability. And so, the PGA linearity represents the biggest reliability constraint.

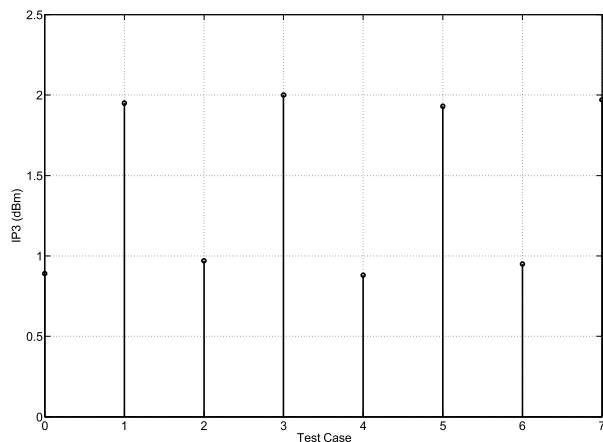


Fig. 4. The architecture $IP3$ degradation for all test cases.

VI. CONCLUSIONS

In this work, we exploited the reliability analysis at the architectural level. As a result, the architecture performance in a

higher abstraction level was described by individual circuit behavior in the level below. We defined the failure of the building block and analyzed the architecture performance degradation for different combinations of failures. Then, we proposed the power consumption as a measure of the ageing degradation in the architectural level.

The WLAN/WiMAX RF front-end architecture reliability was analyzed, and we pointed out the PGA as the most sensitive building block. The PGA failure is responsible for the degradation of the gain and the linearity of the architecture. Moreover, if it is combined with another block failure, the degradation of the noise of the architecture is increased. In lower frequency signals, we found that the DCO is dominant in the degradation of the noise of the architecture.

Going further, we expect to exploit the design for reliability methodology [5] for different building blocks at transistor level. Thus, the architecture lifetime will become a design criterion. Therefore, the robustness of both the architecture and its blocks can be analyzed and improvements may be found.

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