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CMOS 65 nm Wideband LNA Reliability Estimation

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Abstract—Radio frequency (RF) products are very demanding in terms of technology developments. Reliability will be one of the most important challenges for the semiconductor industry during the following years. This work presents a wideband low noise amplifier (WBLNA) designed in CMOS 65 nm, its model for reliability estimation, and simulated results of fresh and aged devices. The WBLNA failure, defined in this work as the amount of degradation to have 3 dB gain loss or 10% bandwidth reduction, has been found for HCI I_D , SBD and EM degradations. The most important simulated reliability degradation results have been highlighted. Therefore, the design for reliability concept can be systematically applied in the RF front-end circuits, and it has helped with WBLNA reliability improvement.

I. INTRODUCTION

Radio frequency (RF) products are very demanding in terms of technology developments. These products have been driven by many circuit constraints as die area, frequency, bandwidth, power consumption, noise performance, linearity and gain. According to the ITRS Roadmap, reliability will be one of the most important challenges for the semiconductor industry during the following years [1]. Reliability is defined as the ability of a circuit to conform to its specifications over a specified period of time and under specified conditions [2].

The design for reliability concept is already applied in digital circuits inserted at the radio core, but not systematically in the RF front-end circuits. The development of reliable RF circuits needs the knowledge of the degradation physics and models for all front-end circuits. The first block at front-end is the low noise amplifier, and its performance is very important to the entire RF circuit performance. Then, the reliability estimation of the low noise amplifier is a constraint in RF circuit reliability estimation. The reliability framework will be able to help the RF front-end circuit designer, aiming the increase of the RF devices reliability.

This work presents a wideband low noise amplifier (WBLNA) designed in CMOS 65 nm, its model for reliability estimation, and simulated results of fresh and aged devices. Sec. II describes the physical phenomena responsible for the WBLNA aging degradation. In Sec. III is explained the WBLNA design steps, aiming the desired performance. In Sec. IV, the gain, the bandwidth, the impedance matching, the noise figure and the power consumption are analytically derived to estimate the WBLNA performance loss in front of the reliability degradation. In Sec. V, the fresh and aged WBLNA performance results are obtained and the circuit reliability are predicted with the technology rules. Finally, design for reliability guidelines are provided to improve RF circuits performance in earlier stages of the product development (Sec. VI).

II. THE PHYSICAL PHENOMENA

The physical phenomena responsible for the most aging degradation in active devices are

- Negative Bias Temperature Instability (NBTI),
- Hot Carrier Injection (HCI) and
- Time Dependent Dielectric Breakdown (TDDB).

They degrade the circuit performance with crystalline structure defaults that changes the device parameters. Passive devices also have aging degradation, mostly caused by

- Electromigration (EM).

In this Section, the HCI, TDDB and EM physical phenomena are discussed. The NBTI is out of the scope of this work, because it affect only p-type transistors [2] which aren't present on WBLNA topology, shown in Fig. 1 [3].

A. Hot Carrier Injection

The HCI is the phenomenon in solid state devices or semiconductors where either an electron or a hole gains sufficient kinetic energy to overcome a potential barrier, becoming a *hot carrier*, and then migrating to a different area of the device. It occurs at the end of the drain junction of a transistor in saturation. The hot carrier is injected from the silicon substrate to the gate dielectric, creating many interface traps. The HCI is more significant in n-type transistors than in p-type ones, and this degradation cannot be recovered in most cases [2].

Hot carriers can degrade the gate dielectric causing electron and hole traps which increase the leakage substrate current and cause drain current decrease. The HCI takes effect when the V_{GD} is greater or equal to zero and the V_{GS} is very high [2]. This is the most common bias operating point in amplifiers circuits. So that, the HCI is a major reliability concern in this work.

B. Time Dependent Dielectric Breakdown

The dielectric breakdown is manifested by a sudden loss of the layer's insulating properties. In older technologies, it was less a problem, where even more pessimistic reliability predictions satisfied the 10 year lifetime for 99.99% of circuits at operating conditions [4]. Nowadays, the probability of oxide breakdown strongly increases with the increasing oxide field in downscaled technologies. For dielectric breakdown two scenarios are distinguished:

- **Extrinsic breakdown** is due to defects in the dielectric which can be introduced during different processing steps and it is out of the scope of this reliability study;
- **Intrinsic breakdown** is caused by the nature of the dielectric itself and occurs at a certain electric field, defined by the dielectric strength.

The intrinsic TDDB failure was classified into two groups, depending on the magnitude of the post-breakdown behavior:

- **Hard Breakdown** is considered a catastrophic failure of the device and, consequently, of the entire circuit;
- **Soft Breakdown (SBD)** is more likely to occur at operating environment and causes a circuit performance loss as a consequence of a few conductive path [5].

C. Electromigration

Electrons passing through a conductor transfer some of their momentum to its atoms, and, at sufficiently high electron current densities (greater than 10^5 A/cm² [6]), these atoms may shift causing electromigration that is the transport of mass in metals. The stressed conductor may fail, caused by an accumulation of vacancies by a positive divergence in the ion flux. The most important circuit damages are:

- the decrease of the electrical conductance,
- formation of open circuit conditions,
- thinning and
- localized heating.

As integrated circuits technologies continue to shrink the metal interconnections and to rise the current densities, EM will remain a reliability concern [6].

III. WBLNA DESIGN

The topology presented in Fig. 1 has been chosen because it has wideband impedance match and noise cancellation [3]. The bias point was obtained with the needed voltage gain (≈ 20 dB). Then, the transistors width was designed to provide the wideband impedance match as $gm_1 = 1/50$ S. Next, $R_{L1,2}$ were calculated to close the gain and matching constraints and they also include the inductor parasitic resistance. Later, gm_2 was designed to provide the noise cancellation with the relationship $R_{L1} = R_s gm_2 R_{L2}$ [3], where $R_s = 50 \Omega$ is the impedance matched with gm_1 . C_L represents all parasitic and load capacitance estimated as 200 fF, $L_{1,2}$ were designed to obtain a 80% LNA flat bandwidth enhance with the equation

$$m = \frac{R_{L1,2} C_L}{L_{1,2} / R_{L1,2}} \approx 2 \quad [7]. \quad (1)$$

The cascode transistors were designed larger enough for low noise and high output impedance. The pad and the bondwire were taken account, according to the technology guidelines, in a embedded ladder filter with a desired upper cutoff frequency bigger than 7 GHz to allow a wideband gain from 100 MHz to 7 GHz. Finally, the values were corrected by simulation to achieve the desired performance, and the final values are presented in Tab. I.

Table I
WBLNA DESIGN VALUES.

M1 size = 64.0 $\mu\text{m}/0.06 \mu\text{m}$	M2 size = 200 $\mu\text{m}/0.06 \mu\text{m}$
M3 size = 200 $\mu\text{m}/0.06 \mu\text{m}$	M4 size = 200 $\mu\text{m}/0.06 \mu\text{m}$
$L_1 = 7$ nH	$R_{L1} = 300 \Omega$
$L_2 = 3.5$ nH	$R_{L2} = 150 \Omega$

IV. WBLNA RELIABILITY ESTIMATION

Aiming the highest product life time, the reliability has to be evaluated in early stages of the design process. So that, the gain (G), the bandwidth (BW), the impedance matching (S11), the noise figure (NF) and the power consumption (P) were analytically derived to estimate the WBLNA performance loss in real operation environment with all physical phenomena degradations. The WBLNA performance figures are

$$G = (gm_1 R_{L1} + gm_2 R_{L2}); \quad (2)$$

$$BW = \frac{1}{2\pi R_{L1,2} C_L} \sqrt{\left(\frac{-m^2}{2} + m + 1\right) + \sqrt{\left(\frac{-m^2}{2} + m + 1\right)^2 + m^2}} \quad [7], \quad (3)$$

where m is from equation (1);

$$S11 = \frac{1 - gm_1 R_s}{1 + gm_1 R_s} \quad [7]; \quad (4)$$

$$NF = 1 + \frac{\frac{(gm_1 R_L)^2 - (gm_2 R_L)^2}{gm_1 R_s + 1} \overline{e_{n1}^2} + (gm_2 R_L)^2 \overline{e_{n2}^2} + 2\overline{e_{nL}^2}}{\frac{(gm_1 R_L)^2 - (gm_2 R_L)^2}{gm_1 R_s + 1} \overline{e_{ns}^2}}, \quad (5)$$

where NF was obtained by the WBLNA circuit noise analysis and $\overline{e_{ni}^2}$ is the noise voltage of the component i ;

$$P = V_{DD} (I_{D1} + I_{D2}), \quad (6)$$

where V_{DD} is the technology voltage supply.

Assuming equal and not correlated probability of occurrence for all physical phenomena in all transistors, the WBLNA reliability can be estimated for each scenario and the worst case can be found. The transistor degradation behavior is illustrated in Fig. 2, where $\Delta I_D = \alpha I_D$ is the α HCI I_D degradation model ($I_{Daged} = (1 - \alpha) I_{Dfresh}$) and SB_d , SB_s are the SBD conductive path [8]. The circuit HCI current degradation is modeled as percentage of decrease in the typical transistor drain current. The circuit post-SBD behavior is a conductive path modeled by a 10 k Ω resistance [8]. The inductor EM degradation model is an additional resistance in series with $R_{L1,2}$, not shown in Fig. 2.

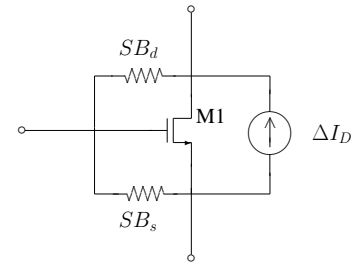


Figure 2. N-type transistor degradation electrical behavior [8]

The HCI degrades more the transistors M1 and M2 than the cascodes. With the drain current or transconductance decreases, the WBLNA has a decrease in gain, power consumption and impedance matching (only if the HCI takes place in M1). The transconduction reduction represents a noise reduction, but not necessary a lower NF. The $\overline{e_{n1}^2}$ reduction suggests a lower NF, but the HCI in M2 lower the $\overline{e_{n2}^2}$ and the topological noise cancellation; corresponding to a higher NF. The dielectric

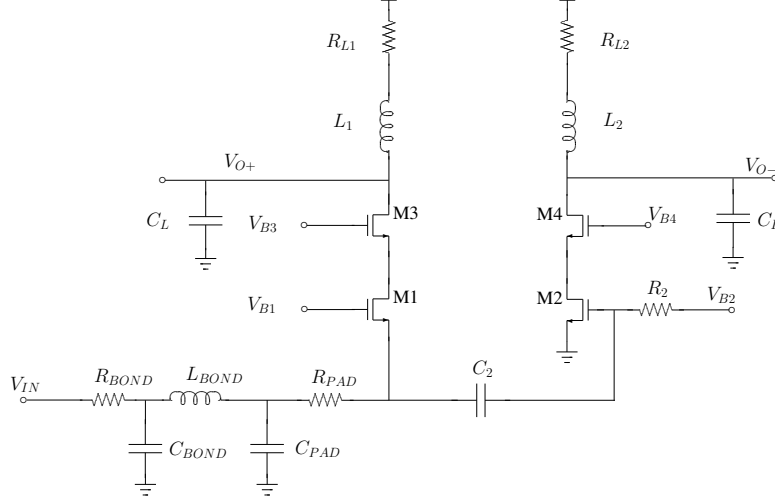


Figure 1. The WBLNA schematic illustration ($R_{BOND} = 0.5 \Omega$, $C_{BOND} = 200$ fF, $L_{BOND} = 1$ nH, $R_{PAD} = 0.2 \Omega$, $C_{PAD} = 200$ fF, $R_2 = 50$ k Ω , $C_2 = 4$ pF)

breakdown conductive path creates a negative feedback which reduces gain and power consumption. It is a resistor noise source and causes a higher NF. The EM affects the integrated inductors increasing R_L , so it causes a bandwidth loss with a minor increase in gain and NF.

V. SIMULATION RESULTS

The WBLNA was simulated with the fresh transistor model, and the important performance results are summarized at Tab. II. Then, the aged transistor model (Fig. 2) was used for circuit reliability simulations with the technology rules.

Table II
WBLNA SIMULATED PERFORMANCE RESULTS.

G = 19 dB	BW = 7.1 GHz
NF (min) = 2.4 dB	NF @ BW = 3.4 dB
P = 5.24 mW	S11 < -11 dB
P1dB @900 MHz = -15.3 dBm	IIP3 @900 MHz = 1.8 dBm
P1dB @2.4 GHz = -16.2 dBm	IIP3 @2.4 GHz = 1.9 dBm
P1dB @5 GHz = -16.6 dBm	IIP3 @5 GHz = 1.6 dBm

The WBLNA reliability estimation highlights the gain or the bandwidth loss, and the WBLNA failure is defined as the amount of degradation to have 3 dB gain loss or 10% bandwidth reduction and both represent a limitation for RF signal detection. Also, the NF increase suggests a failure if it is higher than the standard specification, and it must be taken into account in the worst case scenario.

The HCI has been simulated with different values of α . It was found that 40% HCI I_D degradation is critical for 3 dB gain loss or 10% bandwidth reduction with NF increase. Also, the 40% HCI I_{D1} degradation reduces the impedance matching to S11 < -9 dB. The typical, I_{D1} and I_{D2} 40% HCI degraded gain results are presented in Fig. 3, and the respective NF are presented in Fig. 4. The cascode transistors degradation did not present any significant performance loss until 80% HCI I_D degradation and it is negligible for WBLNA reliability estimation (the simulation results are not presented).

The SBD has been simulated in all transistors as a 10 k Ω conductive path. An SBD event in M2 shows the worst NF and the biggest gain and bandwidth losses. The M1 SBD noise degradation is well canceled by the topology, and the gain degradation is not enough to represent a failure (under the 3 dB loss). The typical, M1 and M2 SBD degraded gain results are presented in Fig. 5, and the respective NF are presented in Fig. 6. The cascode transistors post-SBD behavior did not represent a significant performance loss and it is negligible for WBLNA reliability estimation (the simulation results are not presented).

The EM has been simulated as a $R_{L1,2}$ continuous increase. It was found that only a 50 Ω increase in R_{L2} is enough for a 10% bandwidth reduction and a NF increase. However, the R_{L1} can be increased by EM until 1 k Ω before it represents a failure and the impedance matching loss becomes S11 < -2.5 dB. The inductors should be designed with a larger enough metal line to a lower current density and negligible EM, but it will increase the circuit area. The typical, R_{L1} and R_{L2} EM degraded gain results are presented in Fig. 7, and the respective NF are presented in Fig. 8.

VI. CONCLUSION

This work presented a WBLNA designed in CMOS 65 nm, its model for reliability estimation, and simulated results. The WBLNA failure, defined in this work as the amount of degradation to have 3 dB gain loss or 10% bandwidth reduction, has been found for HCI I_D , SBD and EM degradations. The most important simulated reliability degradation results have been highlighted.

Therefore, design for reliability should be systematically applied in the RF front-end circuits. Moreover, the reliability framework has helped the circuit design. The WBLNA reliability was improved by the cascode transistors and by M2 amplifier branch. However, the M2 amplifier has become the most sensible part of the circuit. The M2 HCI, M2 SBD and L_2 EM have caused severe performance reduction. And,

the wideband impedance matching has remained very sensible to I_{D1} degradation by HCI or L_1 EM, even with WBLNA reliability improvement.

REFERENCES

- [1] ITRS, "Radio frequency and analog/mixed-signal technologies for wireless communications," International Technology Roadmap for Semiconductor, Tech. Rep., 2007, www.itrs.net.
- [2] G. Gielen *et al.*, "Emerging yield and reliability challenges in nanometer CMOS technologies," in *Proc. IEEE Design, Automation and Test in Europe*, March 2008, pp. 1322–1327.
- [3] R. Bagheri *et al.*, "An 800-MHz-6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, December 2006.
- [4] B. Kaczer *et al.*, "Impact of MOSFET gate oxide breakdown on digital circuit operation reliability," *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 500–506, March 2002.
- [5] B. Kaczer *et al.*, "Gate oxide breakdown in FET devices and circuits: From nanoscale physics to system-level reliability," *Microelectron. Reliab.*, vol. 47, no. 4-5, pp. 559–566, May 2007.
- [6] J. B. Bernstein *et al.*, "Electronic circuit reliability modeling," *Microelectron. Reliab.*, vol. 46, no. 12, pp. 1957–1979, December 2006.
- [7] T. H. Lee, *The design of CMOS radio-frequency integrated circuits*, 2nd ed. Cambridge University Press.
- [8] G. T. Sasse *et al.*, "RF CMOS reliability simulations," *Microelectron. Reliab.*, vol. 48, no. 8-9, pp. 1581–1585, September 2008.

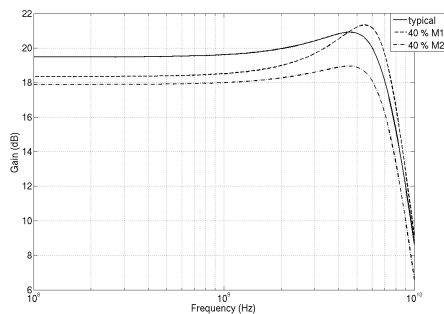


Figure 3. The typical, M1 and M2 40% HCI degraded gain simulated results.

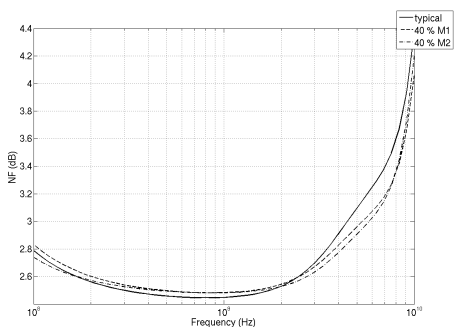


Figure 4. The typical, M1 and M2 40% HCI degraded NF simulated results.

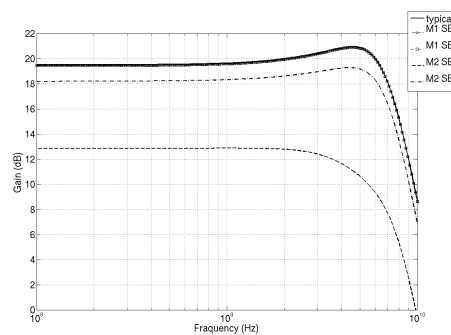


Figure 5. The typical, M1 and M2 SBD degraded gain simulated results.

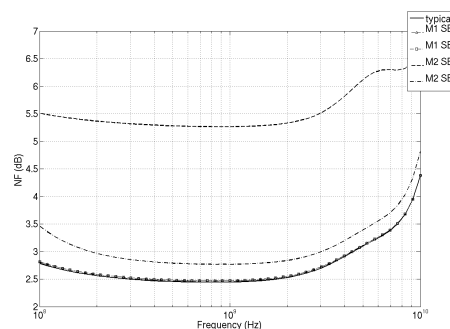


Figure 6. The typical, M1 and M2 SBD degraded NF simulated results.

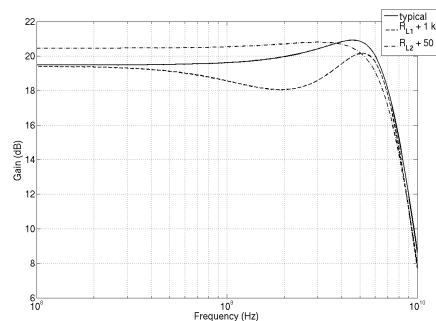


Figure 7. The typical and EM degraded gain simulated results.

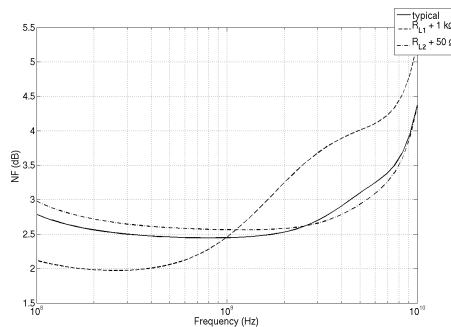


Figure 8. The typical and EM degraded NF simulated results.