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## Current Mode Read-out Circuit for Infrared Photodiode Applications in $0.35 \mu\text{m}$ CMOS

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### ABSTRACT

Infrared focal plane arrays have a wide range of military, medical, industrial and scientific applications, where high resolution and high performance read-out integrated electronics are required. This work advances a regulated cascode current mirror (RCCM) amplifier in  $0.35 \mu\text{m}$  CMOS technology for application in hybrid CMOS-InGaAs implementations. With an output impedance of  $236 \text{ k}\Omega$ , the RCCM produces an output noise power of  $8.06 \text{ nA}$  (RMS), to achieve a SNR of  $77 \text{ dB}$  and a dynamic range of  $60 \text{ dB}$  at  $-40 \text{ dB THD}$ . Comparisons with alternative approaches considering key performance parameters are presented.

### Categories and Subject Descriptors

B.7.2 [Integrated Circuits]: Design Aids—Layout; Simulation

### General Terms

Design

### Keywords

current-mode, infra-red, read-out, image sensor

## 1. INTRODUCTION

Read-out integrated circuits (ROICs) for image sensors are designed for visual wavelength detection purposes, such as the ones in [1]–[7], and have been proposed for infrared wavelength [8]–[13]. However, infrared focal plane arrays have a wide range of military, medical, industrial, and scientific applications, where high resolution and high performance read-out electronics are required. The resolution can be increased by increasing the number of pixels, but then, the pixel size needs to be reduced to decrease not only the overall chip area and therefore its cost, but also the cost of optics. However, the small pixel size limits the complexity, and hence the performance of the read-out circuit.

A high performance circuit should provide a controlled detector bias to reduce the dark current and detector noise. It should have low input impedance to obtain high injection efficiency (i.e.,

$R_D / (R_{IN} + R_j)$ ), for integrating maximum amount of current generated by the detector on the integration capacitance and for increasing its bandwidth and decreasing its input referred noise. Also, it should have a large dynamic range to increase the maximum charge storage capacity, which requires large integration capacitance and high voltage swing [12]. The integration capacitor is preferable placed outside the pixel, as shown in Fig. 1, so the capacitance can be increased without increasing the pixel size.

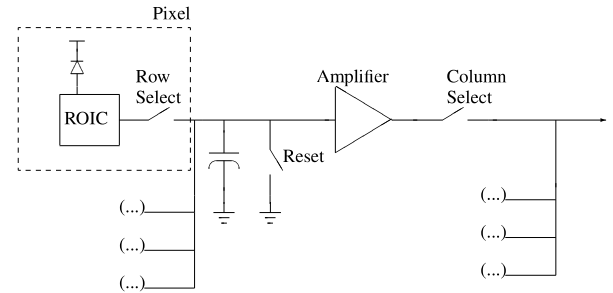


Figure 1: Architecture for current mode read-out circuits.

The majority of the reported read-out circuits are implemented in voltage-mode. They are based on the framework illustrated in Fig. 2, and digitize the integrated current at the column amplifiers. However, as technology scales down, the voltage supply is reduced, affecting the column amplifier operation. The most significant resulting effect is a lower signal swing.

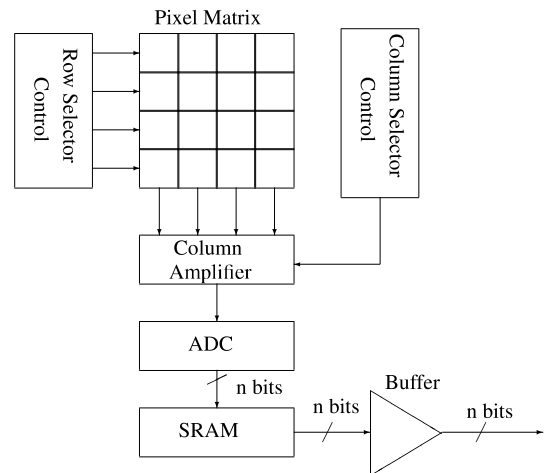
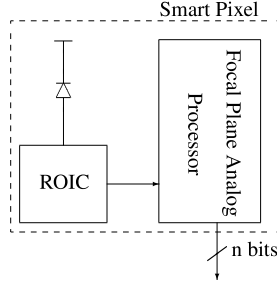


Figure 2: Architecture for voltage mode read-out circuits.

By contrast, in current-mode signal processing, the signal swing is not affected by such trends. Also, current-mode circuits demand less silicon area, have higher operation speed and use simpler building blocks to process the image signal. Moreover, a current-mode read-out approaches, as depicted in Fig. 3, is easily integrated with mixed-signal smart pixels for image processing in analog domain before digitization [14]–[18]. However, the read-out circuit must have high output impedance, aiming at an ideal current controlled source output.



**Figure 3: Smart pixel architecture for current mode read-out circuits analog image processing.**

The InP-InGaAs infrared sensors have been considered to be potential alternatives to low band gap semiconductor infrared photodetectors such as HgCdTe, which suffers from nonuniformity problems in the long-wavelength infrared band. The InP-InGaAs technology offers long-wavelength infrared arrays at significantly lower cost. A disadvantage of InP-InGaAs for infrared applications is the lack of flexibility in adjusting the peak detection wavelength by changing the barrier/well material composition limiting the peak responsivity wavelength to a narrow range around  $8\ \mu\text{m}$  [19]. On the other hand, an InGaAs photodiode can be easily modeled as a Si photodiode, and the read-out circuits implemented in CMOS technology can be redesigned in a hybrid CMOS-InGaAs implementation [20], where the photodiodes are integrated in InGaAs technology and the read-out CMOS circuits are flip-chip Indium bond connected to the sensors.

This work proposes a new design approach for current amplifier implementation for read-out circuit purposes. The target application is in hybrid CMOS-InGaAs implementations, using a  $0.35\ \mu\text{m}$  CMOS technology. The proposed circuit is compared to other competing realizations, considering key performance parameters. Section 2 provides a short review on reported read-out circuits. The proposed current amplifier scheme is presented in Section 3. Results, obtained through theoretical derivation, of noise distortion produced by the proposed circuit are shown in Section 4. Post-layout Spice simulations using BSIM3V3 device model are presented in Section 5, where comparisons are made with alternative realizations. Concluding remarks are made in Section 6.

## 2. REVIEW ON PREVIOUS READ-OUT CIRCUITS

The majority of the reported read-out circuits are implemented with the three transistors active pixel sensor (APS) topology. They are based on an amplifier scheme (transconductance amplifier for current mode applications), having one switch to reset the pixel light information and another one to select line read-out mode. These topologies, including self-integration, source-follower-per-detector, and direct-injection, are simple and occupy small area, but they are unable to satisfy most of the usual performance requirements [1], [12].

More recently proposed amplifier structures, such as buffered-direct-injection and capacitive feedback transimpedance amplifiers, provide a better performance in terms of injection efficiency and detector bias stability with the help of an in-pixel operational amplifier [12], but their performances are limited by the quality of the operational amplifier that should be implemented in a small pixel area. The buffered gate modulation input approach [11] provides in-pixel detector current amplification and background flux suppression with the integration capacitance placed outside the pixel, but it also requires an operational amplifier for detector bias stabilization purposes. As a result, its performance depends on area and operational amplifier performance. Another interesting approach, called switched current integration [13], provides large charge storage capacity with the use of an off-pixel integration capacitor. However, it requires an in-pixel amplifier that limits its detector bias and injection efficiency performance and affects the pixel area.

The current mirroring direct injection technique [10], satisfies the high injection efficiency and controlled detector bias requirements. But it also requires the integration capacitor to be in the pixel, and therefore has large pixel area, low dynamic range, and low charge storage capacity. A high performance read-out structure called current mirroring integration (CMI) was presented in [9]. The circuit provides high performance without needing an in-pixel operational amplifier or integration capacitor, and can be implemented in a small pixel area.

In summary, previous solutions present either low performance with simple structures, or achieve high performance at the cost of large pixel area. Best trade-offs combining high performance with small area was achieved by the CMI structure with a cascode output. However, such circuits do not have large enough output impedance for applications in smart pixel image signal processing (see Figure 3).

## 3. THE RCCM AMPLIFIER

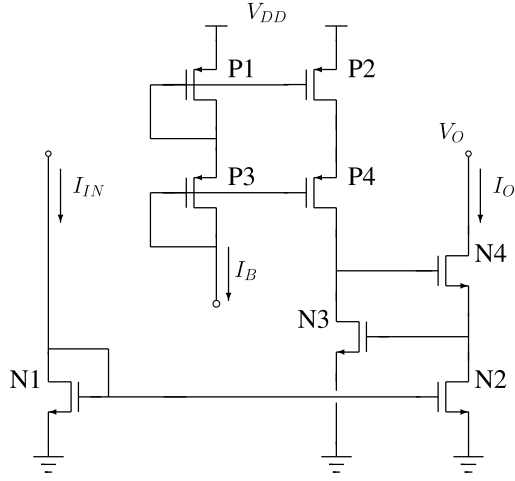
The InGaAs sensor electric model is a non-ideal current source, whose current is a function of the energy of the incident photon. This function is determined by the photodiode responsivity. The current amplifier reads the instantaneous light information directly in continuous time.

A current mirror can be regarded as a current amplifier, whose gain is controlled by the transistor dimensions. Since these are produced simultaneously during the fabrication process, the gain can be precisely implemented, except for channel-length modulation effects, which are the dominant cause of non-linear distortions in the circuit. The RCCM amplifier's gain, shown in Fig. 4, is given by the equation

$$\frac{I_O}{I_{IN}} = \frac{W_2/L_2}{W_1/L_1} \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} \quad (1)$$

where  $I_{IN}$  is anode current produced by the photodiode, and  $\lambda$  is termed the channel-length modulation parameter. This equation indicates that channel-length modulation occurs if  $V_{DS1} \neq V_{DS2}$  [21]. By choosing the bias current  $I_B$  as a fraction of  $I_{IN}$ , equal to the scale factor relating the aspect ratios of N1 and N3, then channel-length modulation effects can be considerably reduced, regardless of the load driven by the RCCM.

The circuit was designed to provide a gain  $I_O/I_{IN} = 10$ , with  $I_B = 0.5\ \mu\text{A}$  from DC up to a cutoff frequency of 2 MHz, taking into account the output capacitance of the input current source, that is, the junction capacitance of the photodiode. The design focused on maximum dynamic range (maximum output current swing) with lower area cost, and it achieved the transistors dimensions shown in Table 1.



**Figure 4: Schematic diagram of the RCCM amplifier.**

Designing N1 and N2 in the saturation region, it should be observed dynamic range trades with harmonic distortion, since  $V_{DS1}$  deviates from  $V_{DS2}$  in large dynamic range applications. Note that  $V_{DS2}$  is fixed at

$$V_{DS2} = \sqrt{\frac{2I_B L_3}{K'_n W_3}} + V_{Tn} = 0.55 \text{ V} \quad (2)$$

whereas

$$V_{DS1} = \sqrt{\frac{2I_{IN} L_1}{K'_n W_1}} + V_{Tn} \quad (3)$$

varies in the range

$$0.51 \text{ V} \leq V_{DS1} \leq 0.58 \text{ V} \quad (4)$$

because the input current  $I_{IN}$  changes with illumination conditions. As a consequence, a current deviation gain of about 2% is produced by Eq. 1. Another constraint in current gain can be observed by

$$V_O \geq \sqrt{\frac{2I_B L_3}{K'_n W_3}} + \sqrt{\frac{2I_O L_4}{K'_n W_4}} - V_{Tn}, \quad (5)$$

where lower output signal removes the transistor N4 from the saturation region. The transistor N3 will be always saturated by the bias circuit ( $I_B$ ).

**Table 1: Transistor dimensions.**

Transistor	$W$ ( $\mu\text{m}$ )	$L$ ( $\mu\text{m}$ )
$N_1, N_3$	1.4	0.7
$N_2, N_4$	14	0.7
$P_1-P_4$	1.4	0.7

Other current amplifier schemes, such as the ones shown in [4] and [5], also employ a fixed voltage to bias the transistor that provides  $I_B$ . In these cases, the difference between  $V_{DS1}$  and  $V_{DS2}$  leads to more significant channel-length modulation effects.

## 4. NOISE ANALYSIS

In this section a theoretical noise analysis is developed for the RCCM circuit. To this end each transistor of Fig. 4 is replaced with a noiseless transistor having a current source connected between the drain and the source terminals with noise power  $I_{Ni}^2$  or  $I_{Pi}^2$ , depending on the transistor type.

The analysis gives the total output current noise power

$$I_{n,O}^2 = I_{n,N}^2 + I_{n,P}^2, \quad (6)$$

where

$$I_{n,N}^2 = I_{N2}^2 + I_{N4}^2 + \frac{gm_{N2}^2}{gm_{N1}^2} I_{N1}^2 + \frac{gm_{N4}^2 r_{o3}^2 I_{N3}^2}{r_{o2} (gm_{N4} + 1/r_{o4}) + 1} \quad (7)$$

is the noise power produced by the transistors N1-N4, and

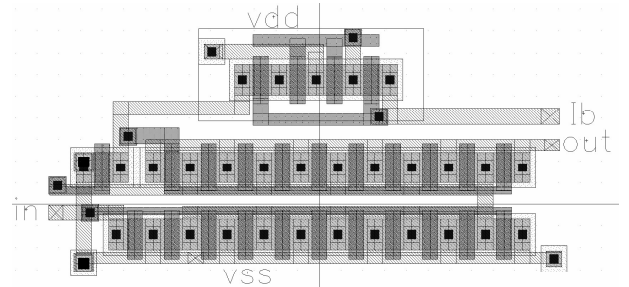
$$I_{n,P}^2 = \frac{gm_{N4}^2 r_{o3}^2}{r_{o2} (gm_{N4} + 1/r_{o4}) + 1} \left( I_{P2}^2 + I_{P4}^2 + \frac{gm_{P2}^2}{gm_{P1}^2} I_{P1}^2 + \frac{gm_{P4}^2}{gm_{P3}^2} I_{P3}^2 \right) \quad (8)$$

is the noise produced by the transistors P1-P4, of the bias circuit.

Since the RCCM gain has a dominant pole at 2 MHz, its noise frequency band is  $\pi$  MHz [22]. The theoretical analysis gives  $I_{n,N} = 4.27$  nA RMS,  $I_{n,P} = 0.69$  nA RMS, and hence the output noise is  $I_{n,O} = 4.33$  nA RMS, integrated in the noise frequency band.

## 5. POST-LAYOUT SIMULATION RESULTS

With an area of  $273 \mu\text{m}^2$ , the layout of the RCCM circuit is displayed in Fig. 5. Post-layout simulations have been carried out for the proposed RCCM circuit. Some key results are compared with those reported by other approaches, namely, the CMI in [9] and the 3T current mode APS in [1].

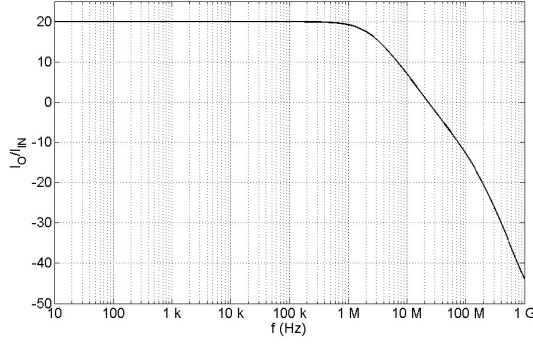


**Figure 5: Layout of the RCCM circuit.**

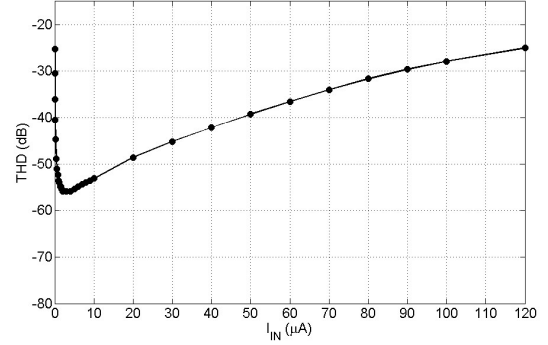
As presented in Fig. 6, the frequency response shows a cut-off frequency of 2.3 MHz with a current gain  $I_O/I_{IN} = 20$  dB. These results agree closely with the theory. Another important parameter is depicted in Fig. 7, in which the RCCM input is a DC current that is swept from 8 nA up to  $120 \mu\text{A}$ . As can be observed, the output practically deviates from the linear relationship as the current increases beyond about  $50 \mu\text{A}$ . As predicted in Section 3, the increasing non-linearity is mainly caused by channel-length modulation. The total harmonic distortion (THD), as a function of the input current, is plotted in Fig. 8. The THD is smaller than  $-40$  dB THD for input currents in the range from  $50$  nA up to  $50 \mu\text{A}$ .

The output noise was computed and integrated in the passband, yielding 4.86 nA RMS, which is close to the theoretical estimate, if one recalls that the simulated frequency band is about 15% larger than the theoretical one. Since the maximum input current is  $50 \mu\text{A}$  for a THD of  $-40$  dB, the signal-to-noise ratio is 77.2 dB. The

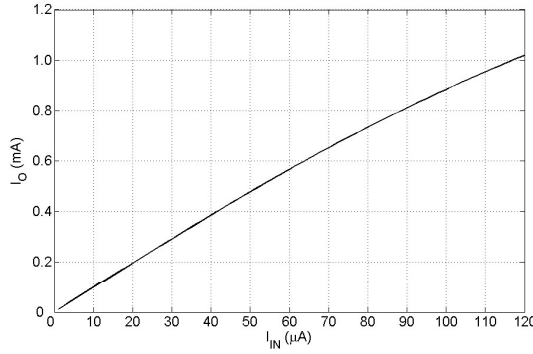




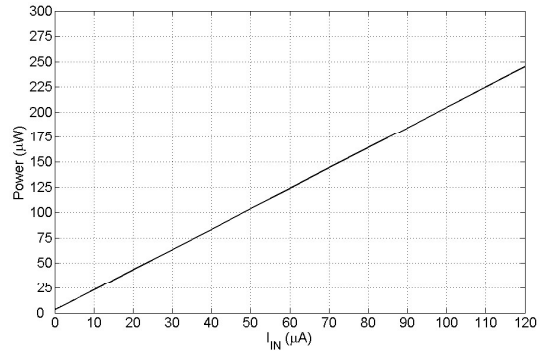
**Figure 6: Frequency response.**



**Figure 8: Harmonic distortion analysis.**



**Figure 7: DC signal range.**



**Figure 9: Power consumption.**

dynamic range, defined as the ratio of the maximum and minimum inputs such that the THD is smaller than  $-40$  dB, is 60 dB. The measured output impedance is  $236$  k $\Omega$ , and the input impedance is evaluated as  $25$  k $\Omega$  for the maximum signal swing. The injection efficiency calculated with this input impedance is 73%.

The power consumption was evaluated against the DC signal range, and is shown in Fig. 9. Variations in the output voltage produce gain deviations if the bounds defined by Eq. 5 are not satisfied. Such deviations, as a function of the output voltage, are shown in Fig. 10. It has been observed that for output voltages in the range from  $0.45$  V up to  $3.35$  V, the current gain error is smaller than 1%.

Table 2 summarizes and compares the performance of the RCCM circuit with the CMI presented in [9] and the two 3T current mode APS approaches reported in [1]. It can be seen that the RCCM outperforms the other approaches in most of the parameters. In addition, the RCCM amplifier presented larger signal-to-noise ratio and dynamic range, with lower area than that of the CMI circuit. The 3T current mode APS circuits [1] have smaller area, but their small output impedance, owing to the single output transistor, make them inviable for smart pixel processing application, such as shown in see Fig. 3.

## 6. CONCLUSIONS

This paper proposed the implementation of a current amplifier for photodiode read-out. The circuit was designed in a  $0.35\mu\text{m}$  CMOS, for application in hybrid CMOS-InGaAs technologies. Notwithstanding, the regulated cascode current mirror can be designed in

moderate or weak inversion. This design allows a trade-off between high output impedance and high output range; this trade-off can be used to choose current-mode amplifiers for specific low-voltage applications.

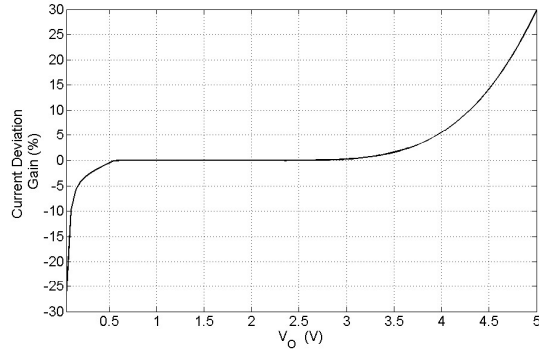
The regulated cascode current mirror, developed in this work, achieved a better balance between high performance requirements, low area cost, high signal-to-noise ratio, and high dynamic range. Post-layout simulation results agreed with the theoretical predictions. Comparisons were made with other approaches. The proposed circuit seems to be a good choice for mixed-signal smart pixels for image processing in analog domain applications.

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**Table 2: Performance summary of the RCCM approach and comparisons with other approaches.**

	[9]	[1]	[1]	This Work
Technology	0.8 $\mu$ m CMOS	0.35 $\mu$ m CMOS	0.18 $\mu$ m CMOS	0.35 $\mu$ m CMOS
Area ( $\mu$ m <sup>2</sup> )	500	100	100	273
$R_O$	$gmr_{ds}^2$	$\frac{r_{ds}}{(1 + gmr_{ds})}$	$\frac{r_{ds}}{(1 + gmr_{ds})}$	$gm^2 r_{ds}^3$
SNR (dB)	N/A	42	39	77
DR (dB)	20	64	53	60



**Figure 10: Simulated output voltage according the gain error.**

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