

Packaging of 10 kV SiC MOSFETs: Trade-Off Between Electrical and Thermal Performances

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Cyril BUTTAY^{1,2}, Hugo REYNES²

¹Laboratoire Ampère, Villeurbanne, France

²SuperGrid Institute, Villeurbanne, France

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Outline

Introduction

Thermal (in)stability

High Voltage, Low R_{Th} Ceramic Substrate

Conclusion

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Thermal (in)stability

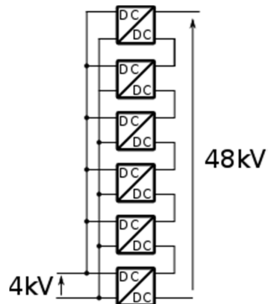
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High power converters based on SiC

Exemple: step-up converter for offshore wind turbines [1]

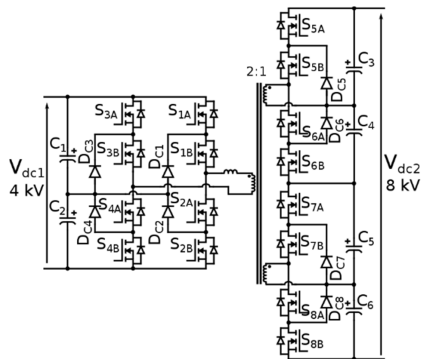
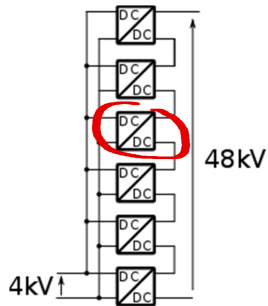
Medium voltage DC bus between wind turbine and HVDC converter



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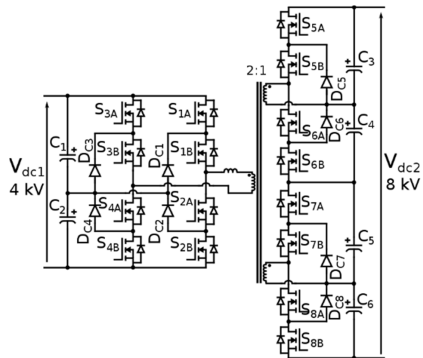
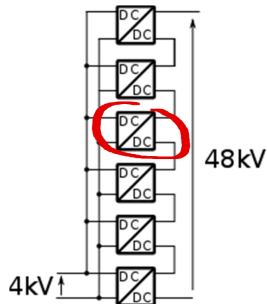
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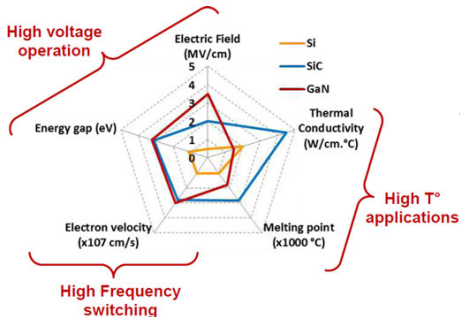
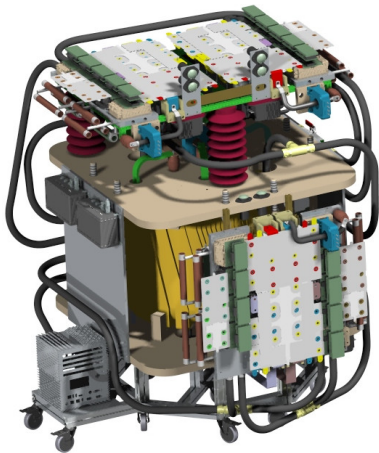
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Medium voltage DC bus between wind turbine and HVDC converter



→ Higher voltage switches allow simpler conversion circuits

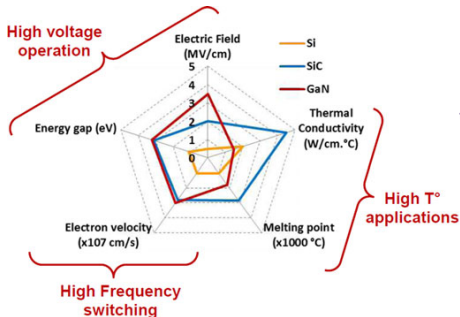
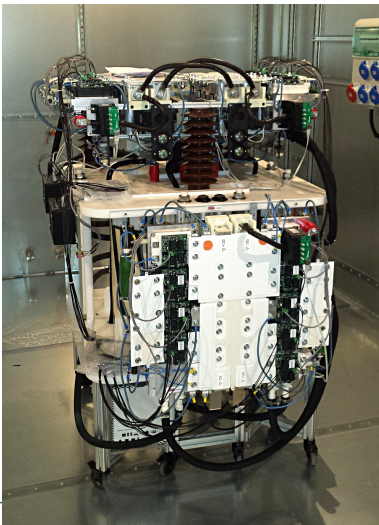
High power converters based on SiC – 2



SiC allows for:

- ▶ Higher voltage switches
 - ▶ Ideally 10 kV or more
- ▶ Higher frequency operation
 - ▶ 10's of kHz vs. < kHz for Si IGBTs
- ▶ Higher ambient/junction temp.?
 - ▶ Not necessarily so, let's find out why

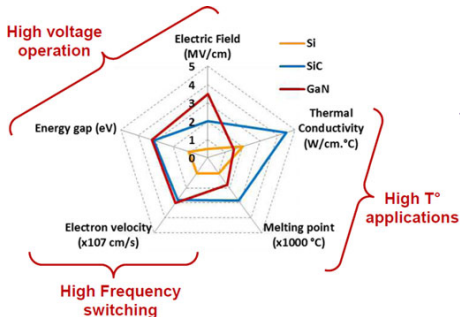
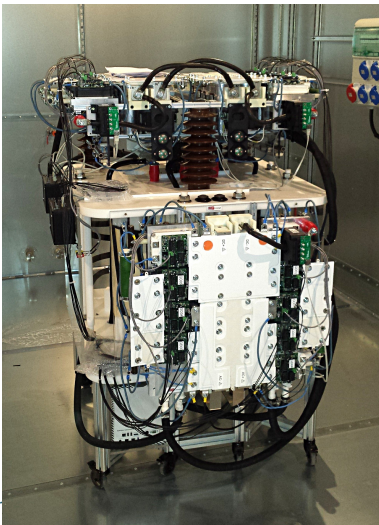
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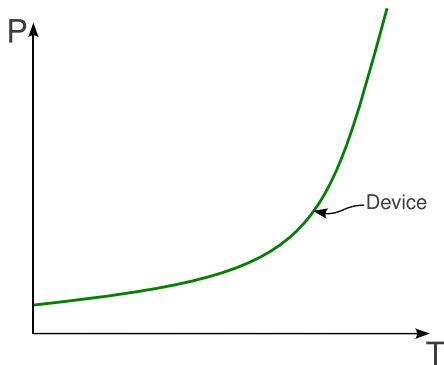
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High Voltage, Low R_{Th} Ceramic Substrate

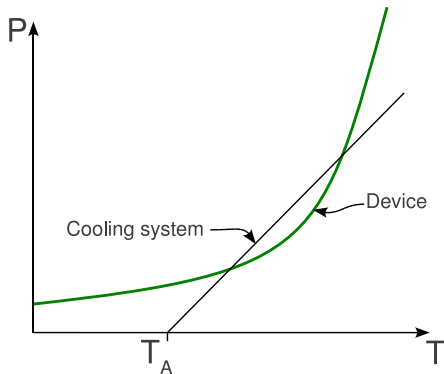
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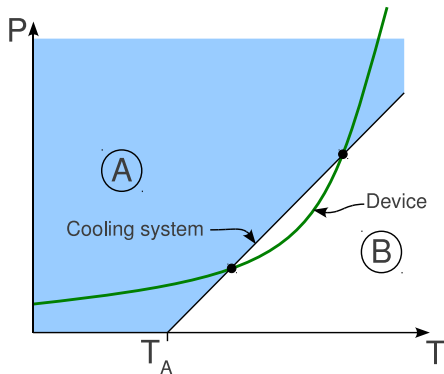
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- ▶ its associated cooling system
- ▶ in region A, the device dissipates more than the cooling system can extract
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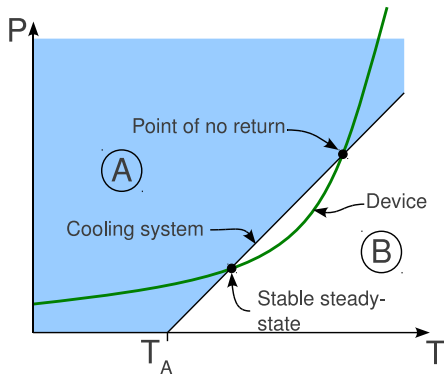
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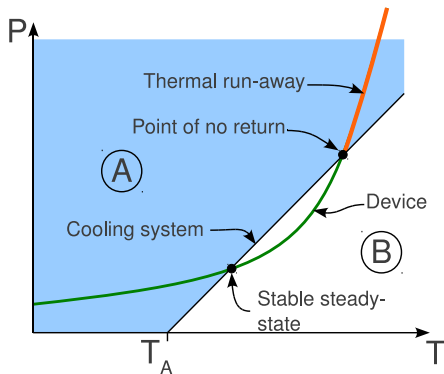
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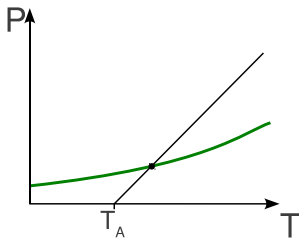
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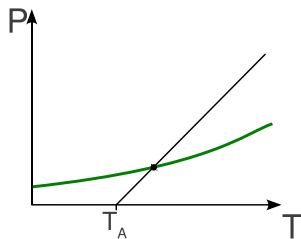
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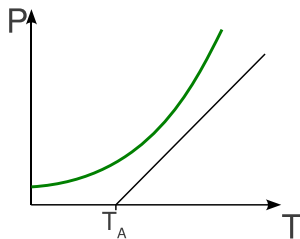
Unconditionally stable

- ▶ Other cases possible, e.g. device with a negative temperature coefficient

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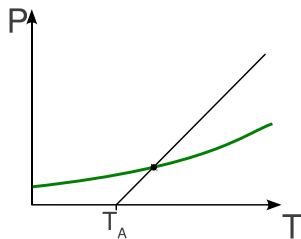
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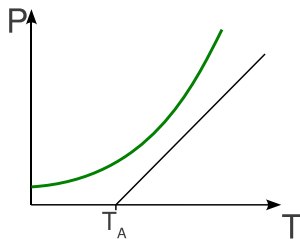
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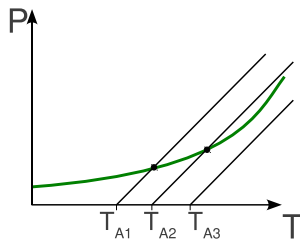
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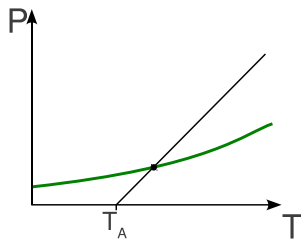
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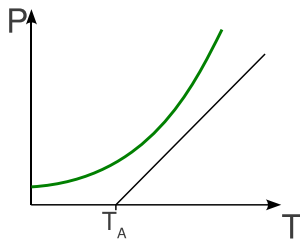
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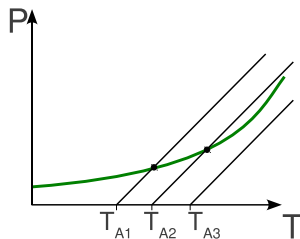
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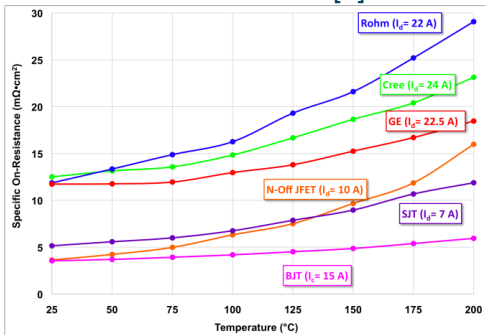


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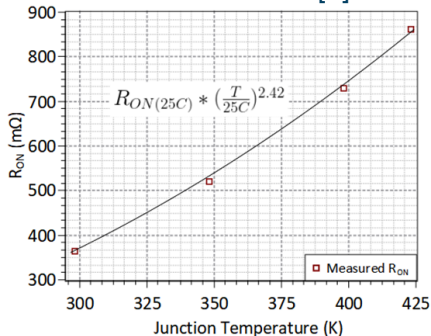
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On-state Resistance (R_{DSon}) of SiC MOSFETs

1200 V devices [3]

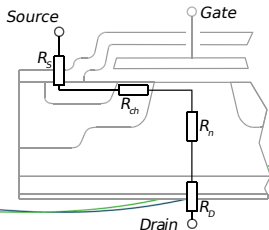


3300 V MOSFET [4]



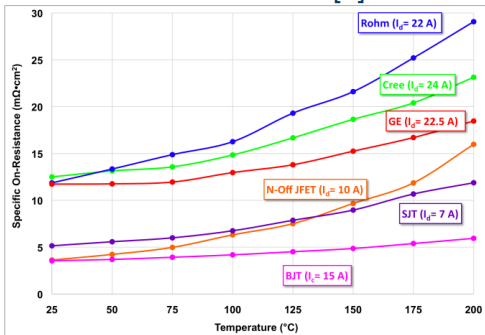
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- ▶ For high voltage devices, R_n is dominant

→ On-losses > double from 25 to 150 $^{\circ}C$

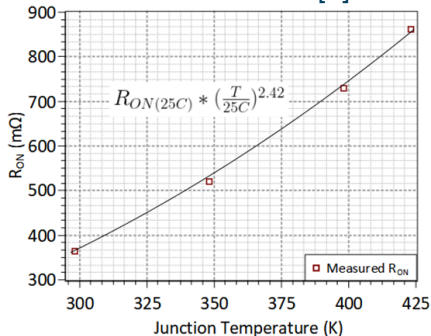


On-state Resistance ($R_{DS(on)}$) of SiC MOSFETs

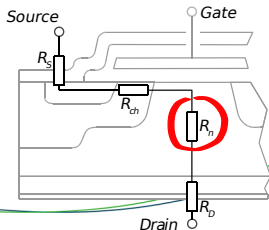
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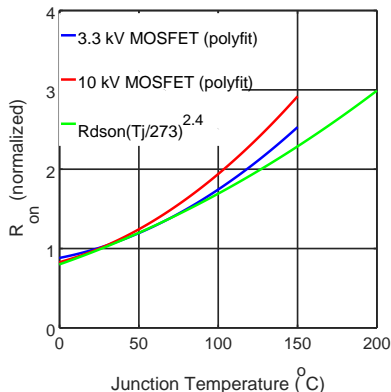
- ▶ Considering only conduction losses

- ▶ $P = R_{DS_{on}} I_D^2$

- ▶ Considering only mobility reduction

- ▶ $R_{DS_{on}}(T_J) = R_{DS_{on,273}} \times \left(\frac{T_J}{273}\right)^{2.4}$ [5]

→ Strong increase of losses with T_J



→ What are the suitable thermal resistance and ambient temperature?

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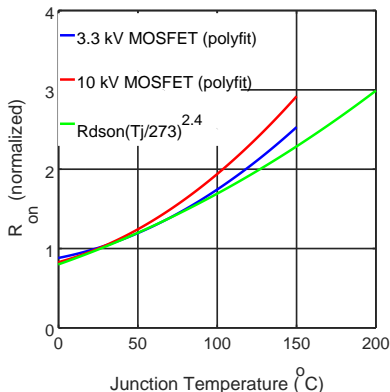
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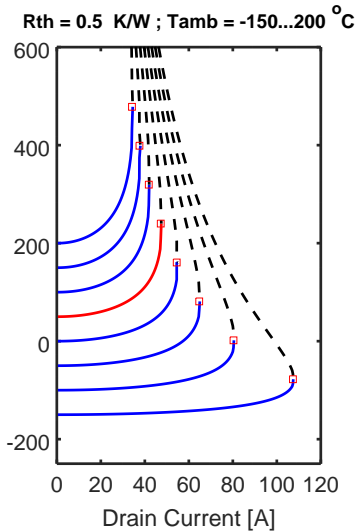
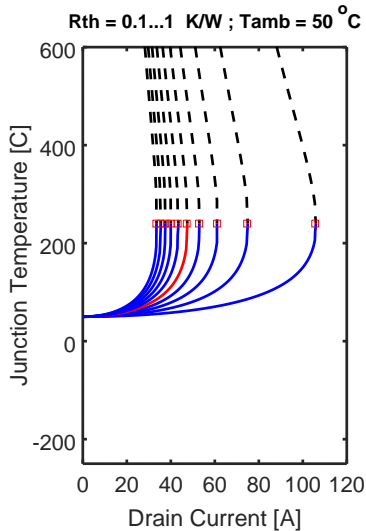
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Conclusions on thermal Run-Away

- ▶ Strong sensitivity to thermal-run-away in conduction mode
- ▶ Ambient temperature to be kept as low as possible
 - ▶ Refrigeration not desirable (risks of condensation)
- ▶ Thermal resistance should be minimized
 - ▶ Trade-off between thermal resistance and insulation
- Objective: to keep $T_J < 100^\circ\text{C}$
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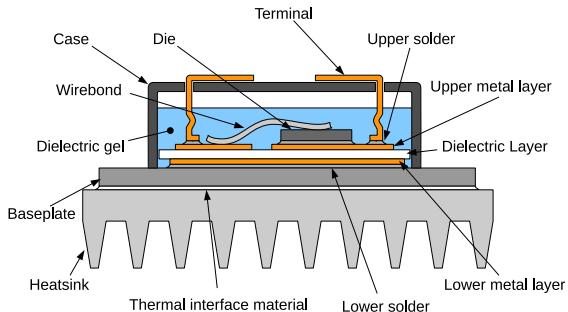
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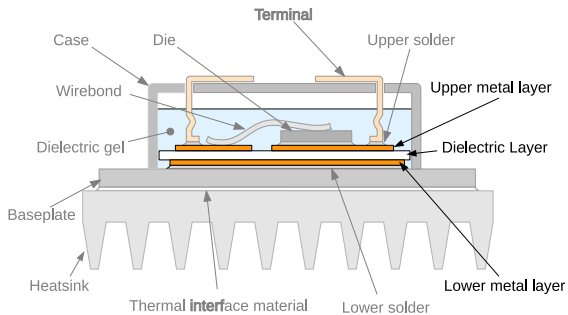
High Performance Cooling of SiC Devices



Packaging of SiC dies

- ▶ Backside cooling
- ▶ Electrical insulation of baseplate

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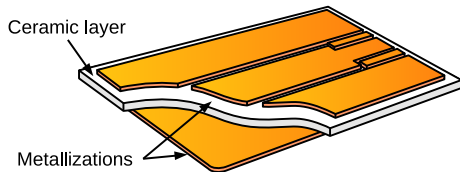


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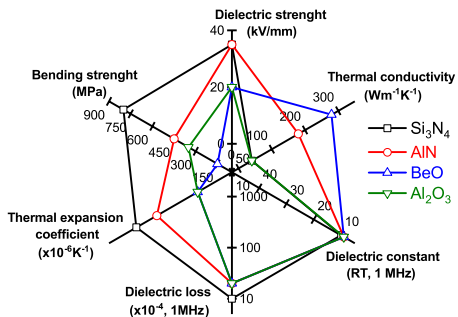
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Ceramic substrate Ensures

- ▶ Electrical insulation
- ▶ Heat conduction



Ceramic Substrates

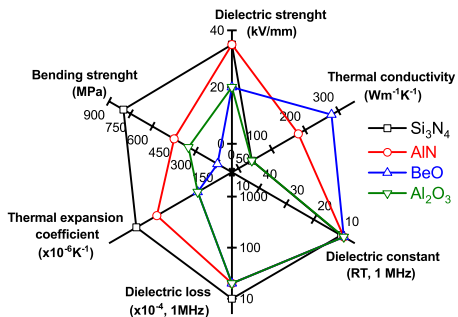


Source: Dielectric properties of ceramic substrates and current developments for medium voltage applications, L. Laudebat et al., MVDC Workshop 2017

Ceramic materials

- ▶ BeO discarded (toxic)
- ▶ AlN next best thermal conductivity
- ▶ AlN best electrical strength

Ceramic Substrates



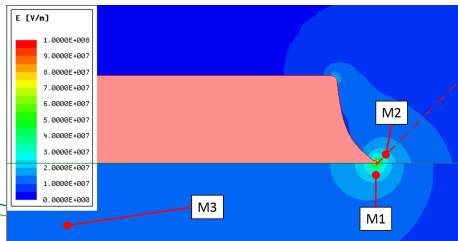
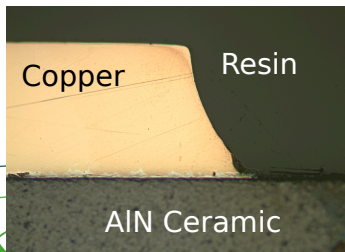
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Substrate structure

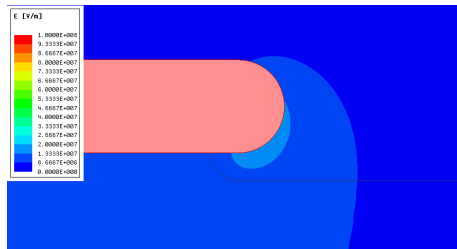
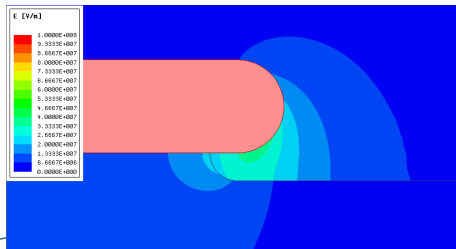
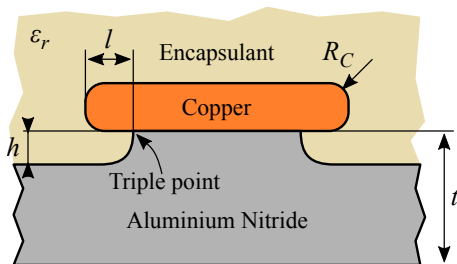
- ▶ “Triple point”
- ▶ Sharp edge of metallization
- Electric field reinforcement



New Substrate Geometry for Higher Voltages

“Protruding” structure

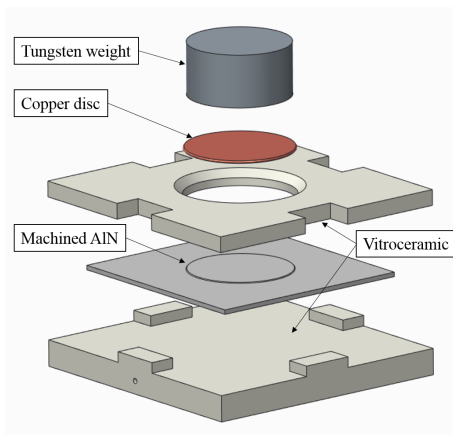
- ▶ Shielding of triple point
- ▶ Rounded electrodes
- ▶ Ideally, encapsulant and ceramic with matched ϵ_R



Substrate Manufacturing

Manufacturing process:

- ▶ Machine AlN (mechanical)
 - ▶ 1 mm-thick AlN
 - ▶ 150 μm recess
 - ▶ Could be etched
- ▶ Prepare electrode
 - ▶ 500 μm -thick copper
 - ▶ 250 μm edge radius
- ▶ Assemble the substrate
 - ▶ Tanaka TKC-651 active braze
 - ▶ Ceramic alignment jig
 - ▶ Vacuum brazing
 - ▶ 900°C peak temp.



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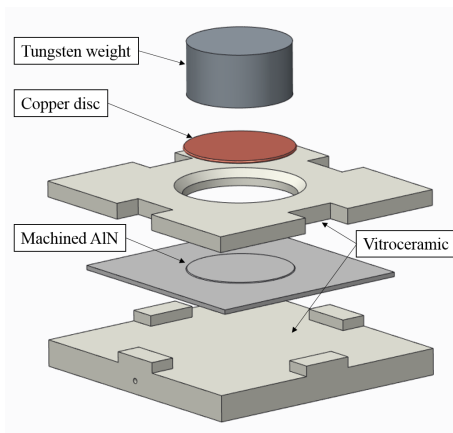
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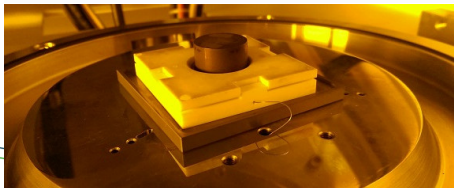
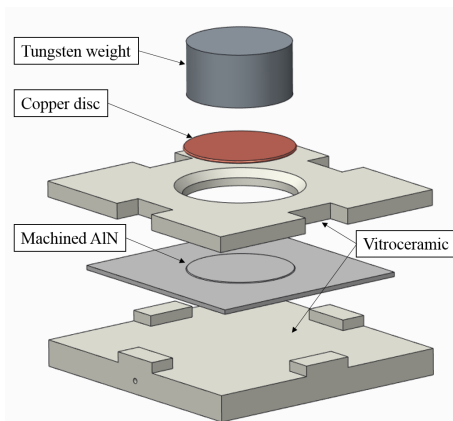
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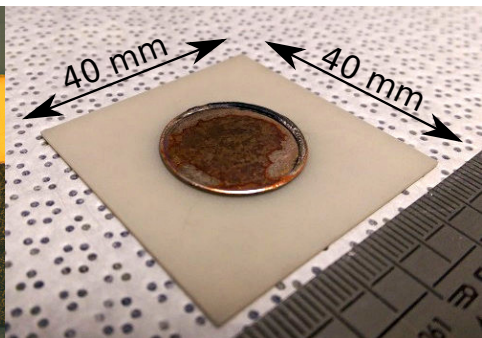
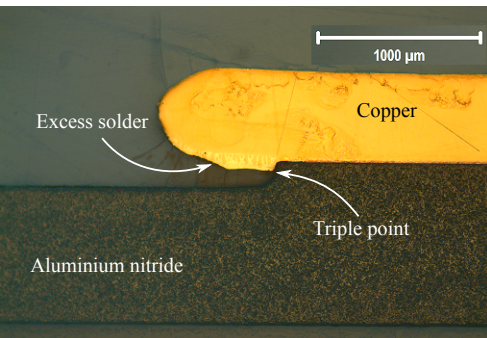
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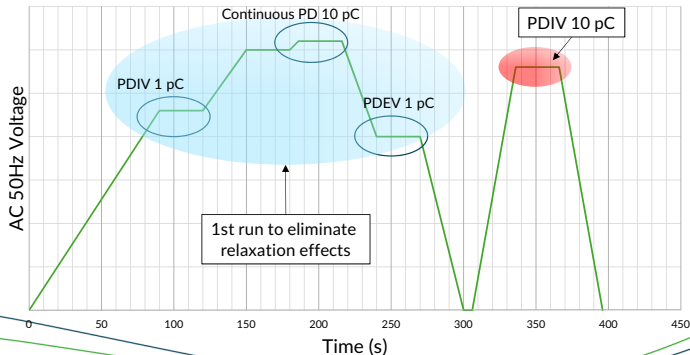
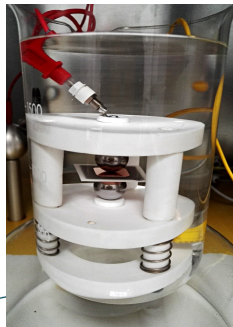
Substrate after Manufacturing



- ▶ Good copper/ceramic interface (no voiding observed)
- ▶ Excess solder flowed along copper, not ceramic
- ▶ Substrate backside coated with Ti/Ag by PVD for testing

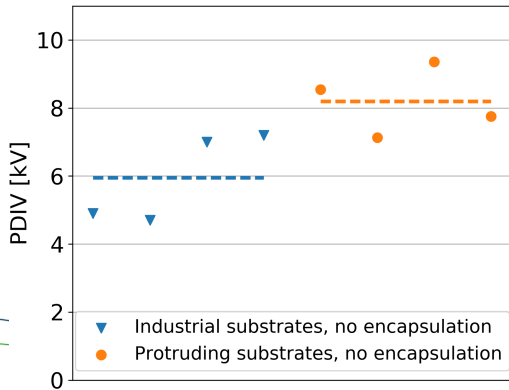
Testing

- ▶ Partial Discharge (PD) testing (LAPLACE Lab. Toulouse, France)
- ▶ Immersion in dielectric fluid (Novec 649)
- ▶ Sample conditioning to eliminate relaxation effects
- ▶ Considered PD threshold: 10 pC



Results

- ▶ Clear improvement of protruding over “standard” substrate
 - ▶ Same total ceramic thickness (1 mm), same ceramic provider
- ▶ Further improvement possible:
 - ▶ Use of encapsulant with $\epsilon_R \approx 9$ (ϵ_R Novec 649: 1.8)
 - ▶ Better manufacturing process (smoother ceramic surface)



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 - ▶ Strong increase in conduction losses with junction temperature
 - ▶ Ideally, operate at junction temperature of 100 °C or less
- ▶ Important trade-off on ceramic substrates
 - ▶ Thin enough to get low thermal resistance
 - ▶ Thick enough to sustain voltage
- Proposed changes in substrate structure
 - ▶ "Protruding structure" for reduction of field reinforcement
 - ▶ Permittivity matching of encapsulant and ceramic (todo)
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 - ▶ Thick enough to sustain voltage
- Proposed changes in substrate structure
 - ▶ “Protruding structure” for reduction of field reinforcement
 - ▶ Permittivity matching of encapsulant and ceramic (todo)
- Solution probably valid for 10-15 kV devices
 - ▶ Above that, more dramatic changes needed in the cooling system.

Conclusion

- ▶ SiC MOSFETs are sensitive to thermal runaway
 - ▶ Strong increase in conduction losses with junction temperature
 - ▶ Ideally, operate at junction temperature of 100 °C or less
- ▶ Important trade-off on ceramic substrates
 - ▶ Thin enough to get low thermal resistance
 - ▶ Thick enough to sustain voltage
- Proposed changes in substrate structure
 - ▶ “Protruding structure” for reduction of field reinforcement
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Bibliography I

-  J. Maneiro, R. Ryndzionek, T. Lagier, P. Dworakowski, and C. Buttay, “Design of a SiC based Triple Active Bridge cell for a multi-megawatt DC-DC converter Keywords,” in *European Conference on Power Electronics and Applications, EPE'17 ECCE Europe*, (Varsovie, Poland), Sept. 2017.
-  K. Sheng, “Maximum Junction Temperatures of SiC Power Devices,” *IEEE Transactions on Electron Devices*, vol. 56, pp. 337–342, Feb. 2009.
-  C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, and P. Mattavelli, “High-temperature characterization and comparison of 1.2 kv sic power semiconductor devices,” vol. 2013, pp. 000082–000087, International Microelectronics Assembly and Packaging Society, 2013.
-  R. Singh, “Realization and commercial insertion of >3300 v sic mosfet,” 2017.
-  B. J. Baliga, *Power Semiconductor Devices*. Boston: PWS Publishing Company, 1997.

Thank you for your attention

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cyril.buttay@insa-lyon.fr