

Packaging with double-side cooling capability for SiC devices, based on silver sintering

IECON 2018

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21/10/18

Introduction

Manufacturing of the 3-D structure

Results

Conclusion

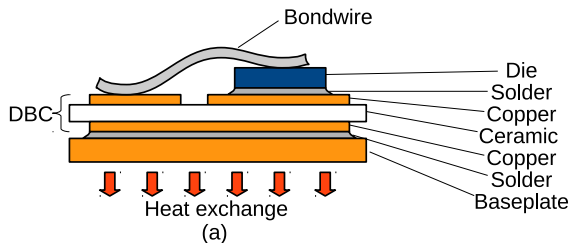
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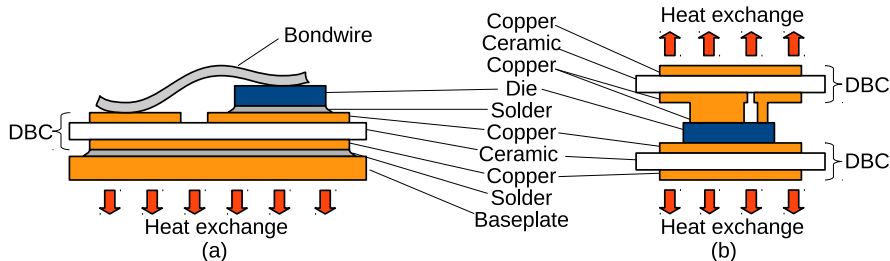
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Double Side Cooling



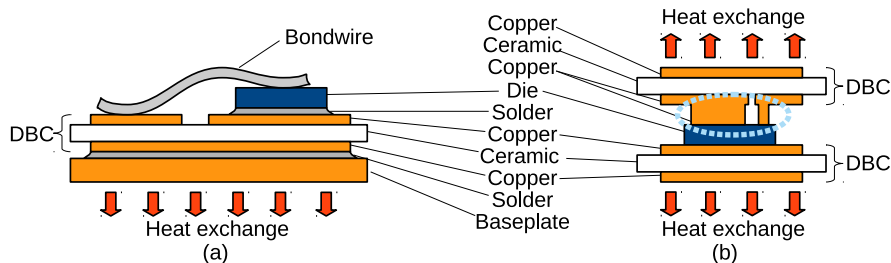
- ▶ SiC JFETs (or MOSFETs) sensitive to thermal run-away
- ➔ Need for efficient cooling, despite high temperature capability
- ▶ Standard packaging offers cooling through one side of the die only
- ▶ “Sandwich” package performs thermal management on both sides
- ▶ Requires special features for topside contact

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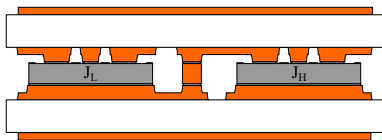
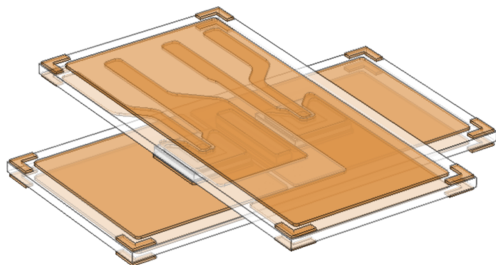
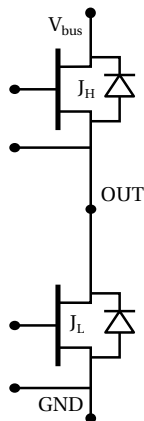
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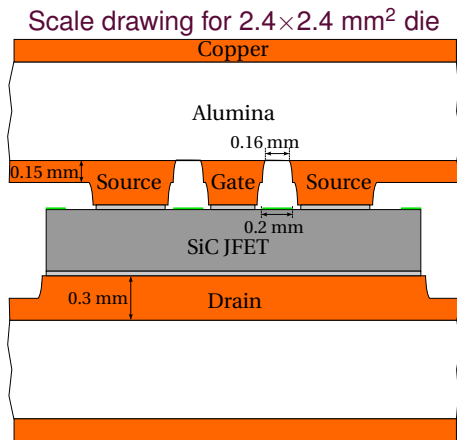
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The proposed 3-D Structure



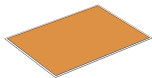
- ▶ Two ceramic substrates, in “sandwich” configuration
- ▶ Two SiC JFET dies (SiCED)
- ▶ Assembled using silver sintering
- ▶ 25.4 mm×25.4 mm (1 in×1 in)

Ceramic Substrates



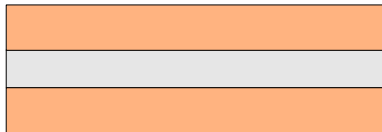
- ▶ Etching accuracy exceeds standard design rules
- ▶ Double-step copper etching for die contact
- Custom etching technique

Preparation of the Substrates

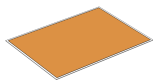


plain DBC board

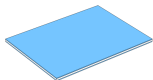
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 - ▶ Die top metallized (PVD) with Ti/Ag
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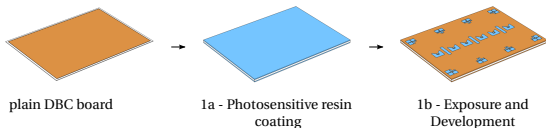


1a - Photosensitive resin coating

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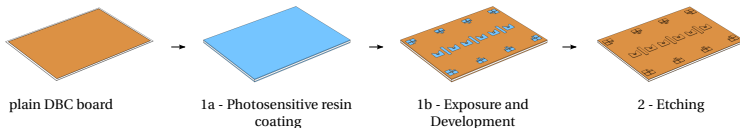
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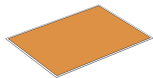
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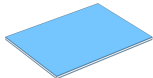
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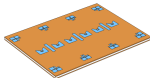
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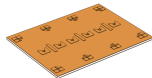
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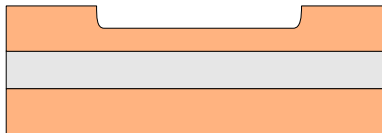


1b - Exposure and Development

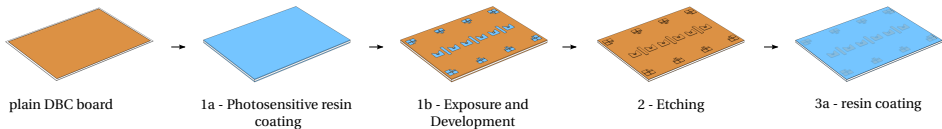


2 - Etching

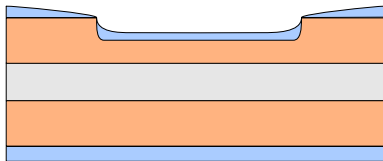
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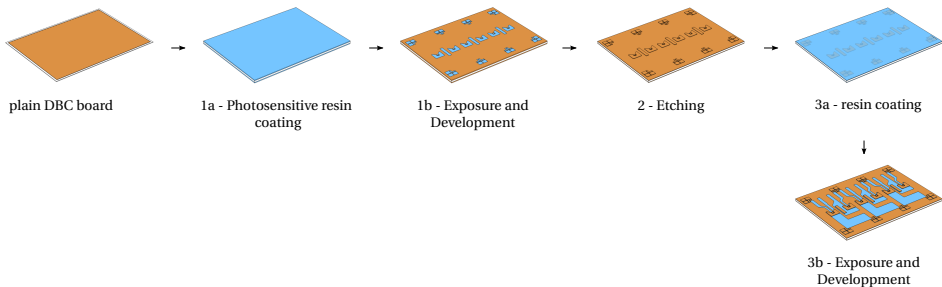
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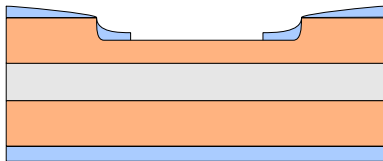
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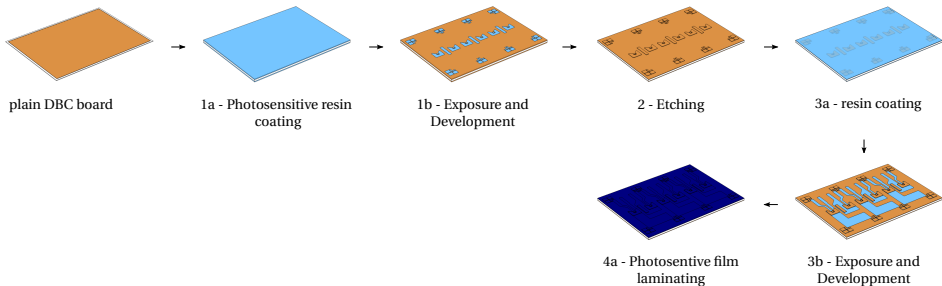
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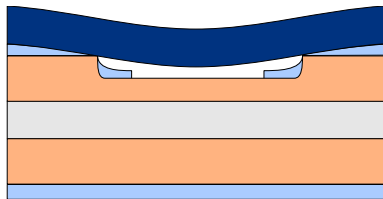
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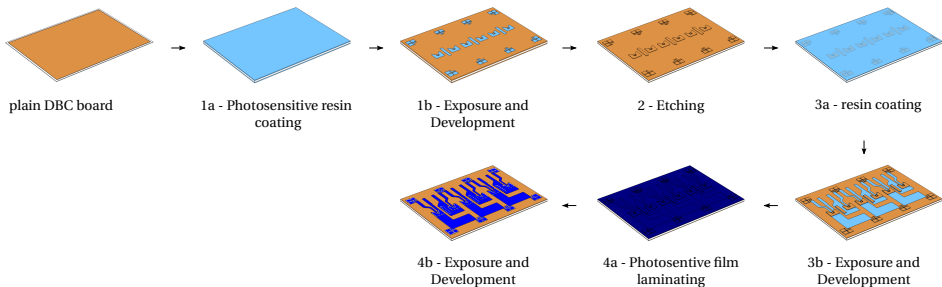
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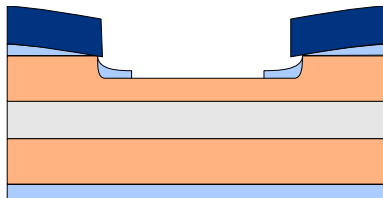
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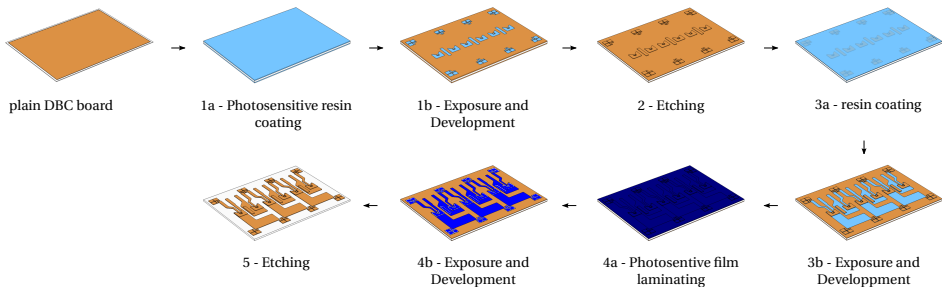
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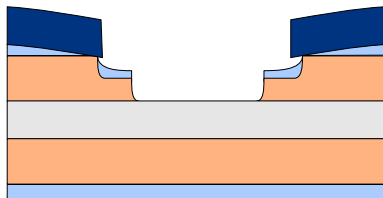
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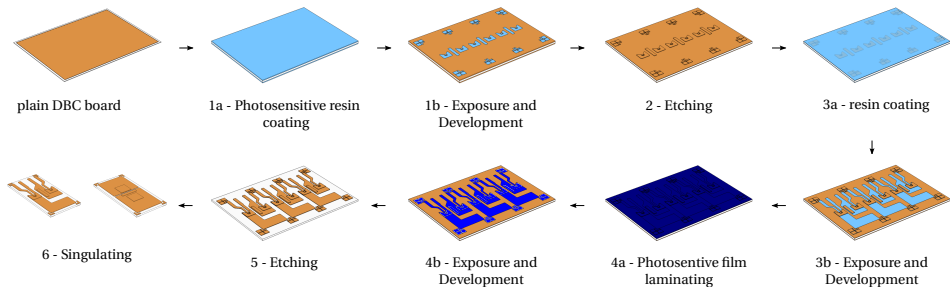
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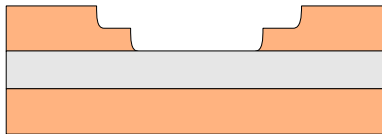
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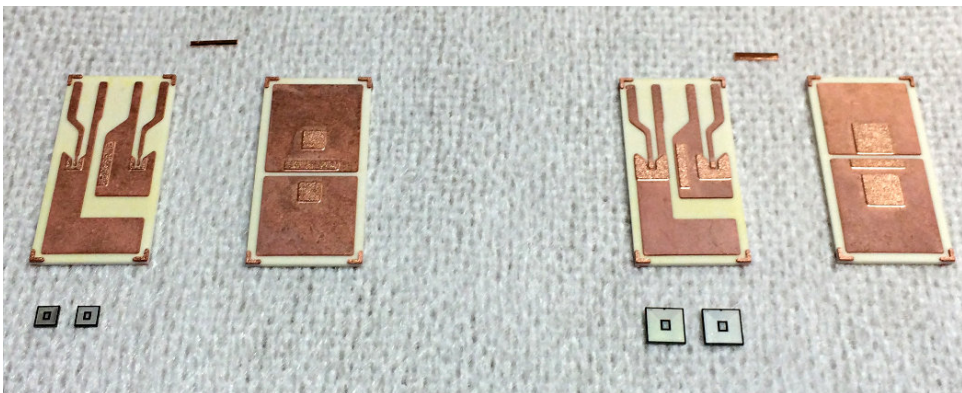
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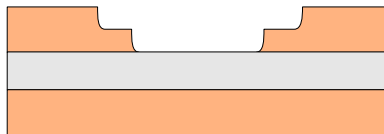
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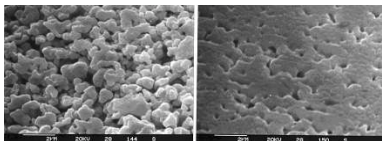
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Bonding Material: Silver Sintering



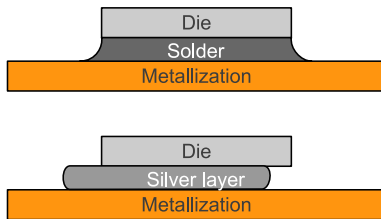
Göbl, C. et al "Low temperature sinter technology Die attachment for automotive power electronic applications" proc of APE, 2006

Silver Paste

- ▶ Based on micro-scale silver particles (Heraeus LTS-11702P2)
- ▶ Low temperature (240 °C) sintering
- ▶ Low pressure (2 MPa) process

No liquid phase involved:

- ▶ No movement of the die
- ▶ No bridging across terminals
- ▶ No height compensation thanks to wetting

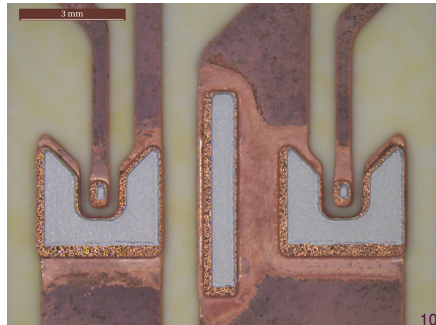


Assembly

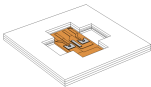


Screen printing

- ▶ Ceramic jigs for alignment of dies and substrate
- ▶ Pre-drying of paste to prevent smearing
- ▶ Two sintering steps using the same temperature profile



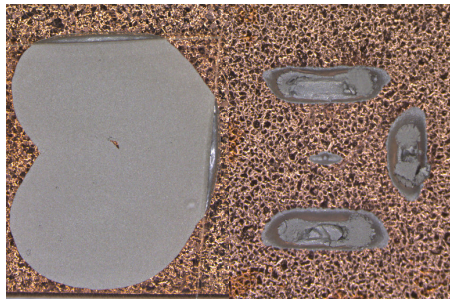
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Screen printing

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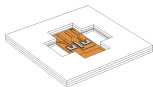
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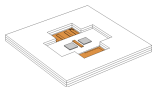
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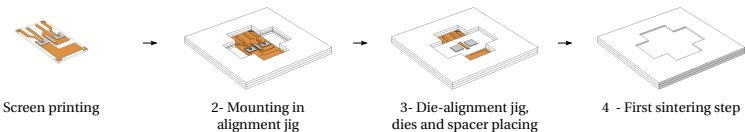
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3- Die-alignment jig, dies and spacer placing

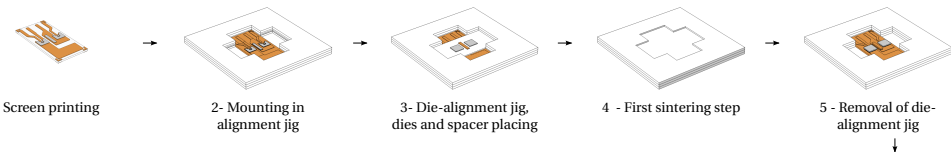
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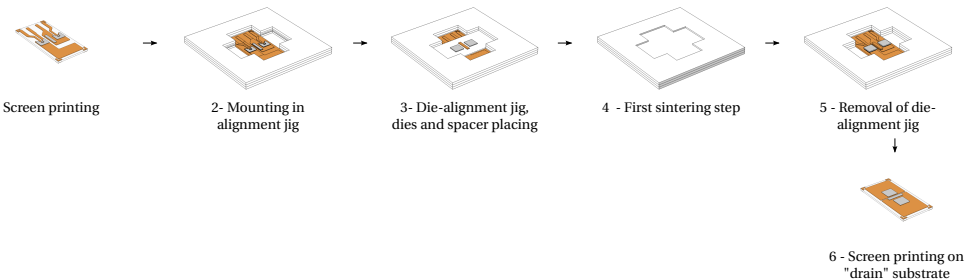
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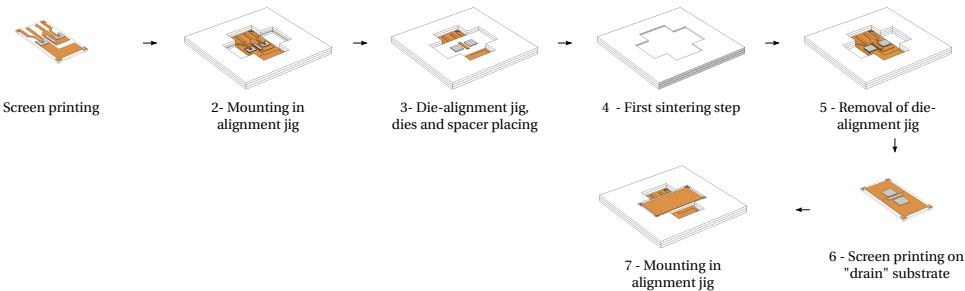
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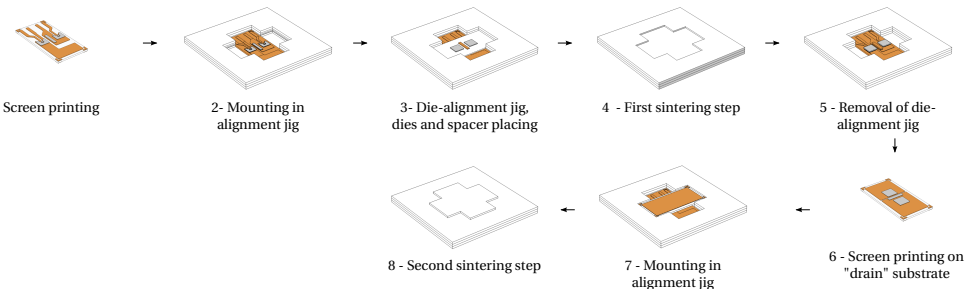
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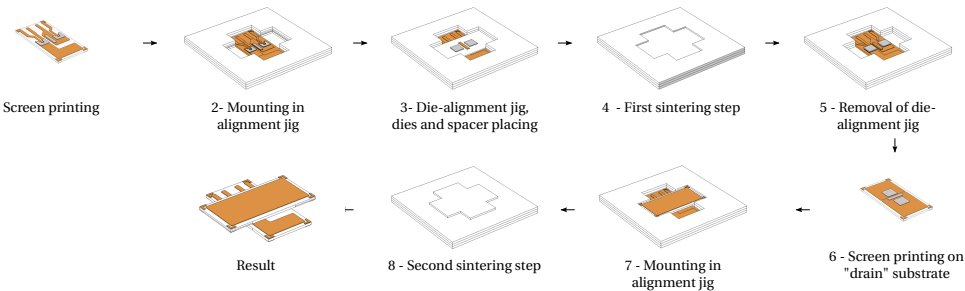
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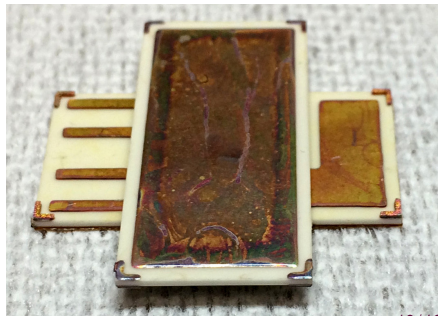


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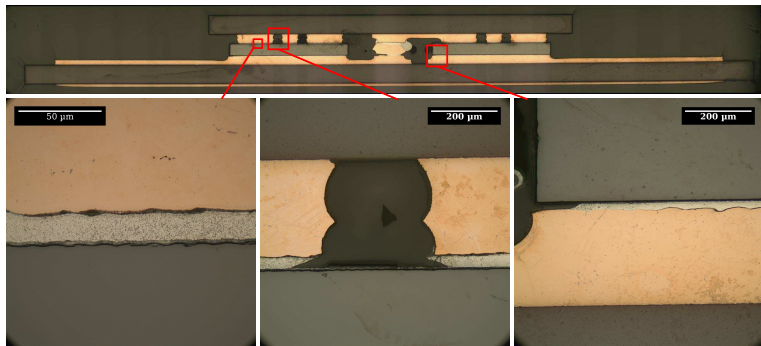
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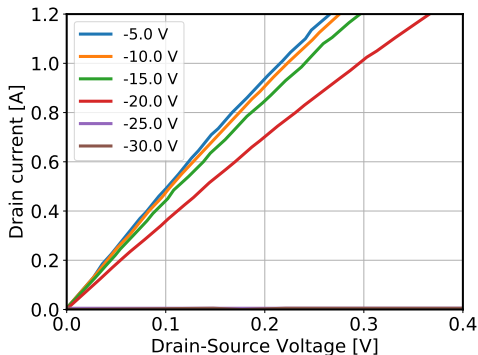
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Cross-section

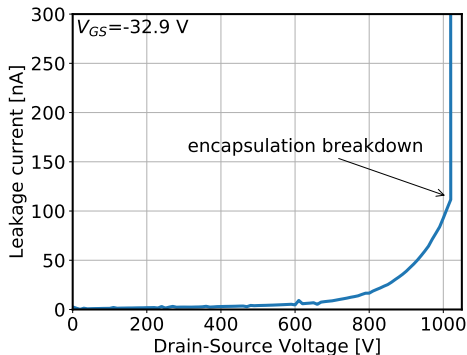


- ▶ Very good form factor, especially around gate contact
- ▶ Uniform silver layers
- ▶ Encapsulation with parylene HT (not shown here)

Electrical Test



Measurement: Tektronix 371A curve tracer, room temperature



Keithley 2410 source & measure unit, room temperature

- ▶ Contact on Gate, Source and Drain of all JFETs
- ▶ No short-circuit between contacts

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 - ▶ Should be able to operate continuously at 300 °C
- ▶ Silver sintering is suited to rigid sandwich structures.
- ▶ Proposed etching technique offers satisfying resolution
- ▶ Package for demonstration of technology, no cooling attempted yet
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Thank you for your attention.



This work was supported through the grants EPAHT (French National Foundation for Aeronautic and Space Research - FNRAE) and THOR (EURIPIDES-CATRENE).

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