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Threshold voltage instability in SiC MOSFETs as a consequence of current conduction in their body diode

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Abstract

An antiparallel PiN diode is present in the structure of the SiC Power MOSFET. For simplicity, increased module current ratings, and cost reasons, it sometimes may be preferable to use this diode rather than to add an external Schottky diode to the MOSFET. However, SiC PiN diodes are sensitive to defects in the SiC crystal, and their performance can degrade rapidly.

In this paper, we assess the effect of several stresses on the characteristics of a SiC MOSFET, focusing on the stresses which involve the body diode. We demonstrate that using the body diode does not degrade its performances. However, it may produce a noticeable shift in the threshold voltage of the MOSFET. While this behaviour is observed for MOSFETs from one manufacturer, it is not exhibited for others, which indicates that it may be a consequence of some particular design or manufacturing parameters.

1. Introduction

SiC power devices are now commercially available from many manufacturers [1]. They offer dramatic improvements in performance over the ubiquitous Si power devices [2], especially regarding high voltage or high temperature [3]. SiC technology is progressing rapidly, and although devices still suffer from some reliability issues, they continuously improve.

Many issues regarding manufacturing yield or device reliability can be traced back to defects in the SiC crystal structure, such as screw dislocations [4] or micropipes [5]: when they do not alter a device's performance so much that it becomes useless, defects can cause a gradual drift in its performance. An example is the increase in forward voltage of PiN diodes as a result of the propagation of defects such as stacking faults [6]. Similar observations were made on SiC bipolar transistors [7]. These defects also cause increased leakage current, and therefore strongly affect high voltage devices [8]. SiC wafers with reduced defect density are now available, with less than 1000 dislocations/cm² over a 150 mm wafer [1], so crystal quality is no longer considered as a major issue which could impede the commercial success of SiC.

Another set of issues affects SiC MOSFETs. It is related to the electron mobility in the channel [6] and the reliability of the oxide layer which forms the MOS structure [9]. The consequences are a higher on-state resistance (in the case of poor channel mobility) and a gradual drift in the threshold voltage of the MOSFET. In some extreme cases, such drift could cause the device to become normally-on [10]. As with the crystal defects, recent improvements in the technology have largely mitigated these issues, and SiC MOSFETs have *de facto* become

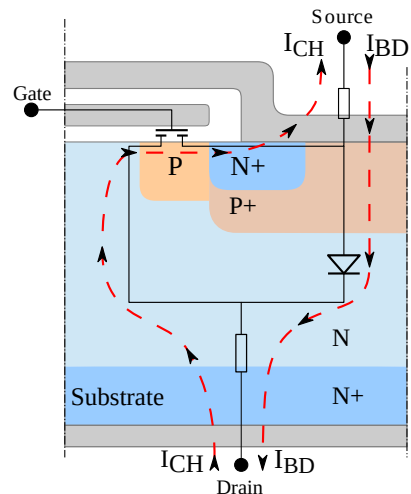


Figure 1: Cross section of a power MOSFET, showing the I_{BD} (body diode) and I_{CH} (channel) current paths.

the major SiC controlled switch. This is illustrated by the discontinuation of alternative devices such as Infineon's JFET or Fairchild's BJT.

With the improvement in technology, the SiC devices have now reached a point where they can be used in real applications, and the reliability studies have shifted from simple test setups to more complex configurations. An example is the body diode of the MOSFET. In inverter topologies, an antiparallel diode is usually connected to each transistor so current can flow during the "dead-time" periods (when both transistors of a half-bridge are in the off-state). Classically, a SiC Schottky (or Merged PiN-Schottky) diode is used, because it has a low forward voltage ($V_F \approx 1$ V) and because it does not suffer from material degradation, as presented above. However, this requires two

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components per switch (a MOSFET and a diode). As the power MOSFET structure already contains a PiN diode (Fig. 1), a possibility is to use it instead of an external diode. This saves space (one die per switch instead of two) and money, at the cost of increased losses: PiN diodes have a higher forward voltage drop ($V_F \approx 3$ V instead of 1 V for Schottky diodes) and recovery charge (although not nearly as much as comparable Si diodes). However, as the dead-time period is short, usually a few percents of the switching period, the effect remains small. It is worth noting that a SiC MOSFET with an integrated Schottky diode was introduced in [11], but in most cases, the internal (body) diode has a PiN junction as described in Fig. 1.

A recent study [12] investigated the degradation of the PiN junction of a SiC MOSFET in realistic use cases (a 3-phase inverter). Only a very small change in forward voltage drop was observed (increase as well as decrease, indicating that stacking faults were not the predominant degradation mechanism at work). Overall, it was found that the body diode could be used as a functional element, in place of external diodes.

Here, we present the results of a similar investigation, where we not only monitored the changes in the forward voltage drop of body diodes (V_F) but also in the threshold voltage of the corresponding MOSFET (V_{th}). As in [12], we observe no significant change in V_F due to current flowing in the body diode. However, we observe a strong shift in V_{th} in at least one manufacturer’s parts, which has not been reported so far.

The next section of this article presents the test protocols based on static (i.e. no switching) or dynamic (more realistic case) operations. The corresponding results are presented and discussed in section 3.

2. Test Protocol

Except when explicitly mentioned, all tests presented here were performed on C2M0080120D SiC MOSFETs (Wolfspeed), which are rated at 1200 V and 80 mΩ. The devices were purchased in two batches (2014 and 2016): the first batch was used for the HTRB/CMB tests (see below), while the second was used for all the other tests (Q1, Q3, Q4 and HTGB). For the sake of simplicity, these devices are referred to as “Wolfspeed” MOSFETs in the text. All characterizations were performed using a Keysight B1505A curve tracer, at room temperature, 1 h after the end of the corresponding test (to allow enough time for the devices to cool down, but soon enough to minimize relaxation effects).

2.1. Static Tests

Five static test circuits are used: the first two are the “High Temperature Reverse Bias” (HTRB) and “High Temperature Gate Bias (HTGB) (Fig. 2, top), described in a JEDEC standard [13], which are classically used to evaluate the effects of a continuous bias on power devices. For the HTRB, a negative voltage source (here -8 V, corresponding to a value close to the absolute minimum voltage, -10 V, allowed in its datasheet [14]) is connected to the gate and source of the Device Under Test (DUT), and a positive voltage is applied between drain and

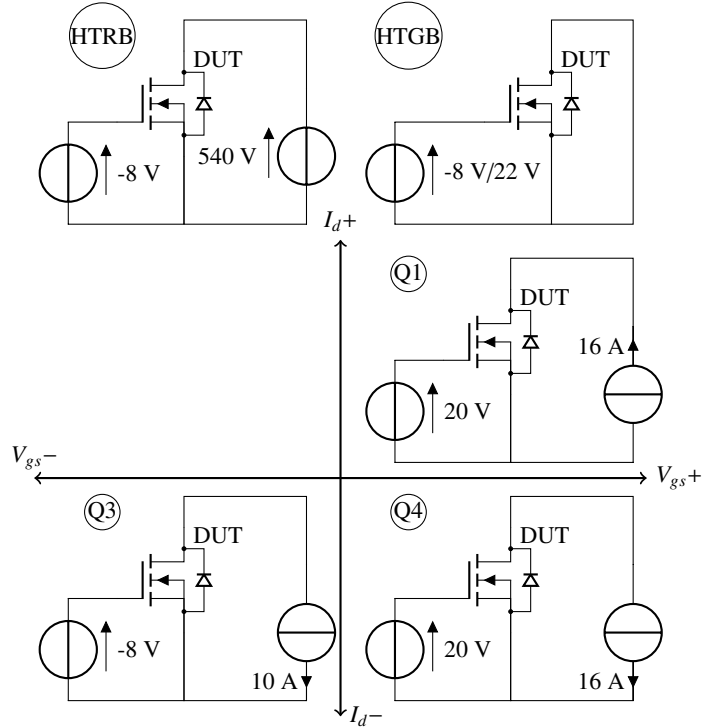


Figure 2: The five static test circuits: voltage bias on the drain (HTRB), negative or positive gate bias on the gate, with drain and source shorted (HTGB), and three tests with current bias (Q1 to Q4).

Table 1: Summary of the static tests conditions

Test	samples (N)	V_{gs} (V)	I_{ds} (A)	V_{ds} (V)	T_j ($^{\circ}$ C)	Power (W)
HTRB	10	-8	0	540	150	0
HTGB	1	-8	0	0	150	0
HTGB	3	22	0	0	150	0
1 st quadrant	3	20	16	0	150	37.3
3 rd quadrant	3	-8	-10	0	150	37.3
3 rd quadrant	3	-5	-10	0	150	37.3
4 th quadrant	3	20	-16	0	150	37.3

source (here 540 V, which corresponds to the bus voltage of the aeronautic HVDC standard [15]). For the HTGB, the drain and source terminals are shorted, and two gate levels were investigated here: -8 V or 22 V (a value very close to the absolute maximum allowed). In these tests, no current flows through the DUT.

The three remaining test circuits are also depicted in Fig. 2 (configurations Q1, Q3 and Q4). They represent the three configurations which result in current flowing through the drain of the MOSFET: either the transistor is in the on-state ($V_{gs}=20$ V, the recommended value in the datasheet) so the current flows through its channel (I_{CH} path in Fig. 1) in both directions (Q1 or Q4), or the transistor is in the off-state ($V_{gs}=-8$ V), so the current flows through its body diode (I_{BD} in Fig. 1). This latter configuration corresponds to Q3 in Fig. 2.

All tests are run at the maximum junction temperature allowed by the manufacturer (150 $^{\circ}$ C), to accelerate any degrada-

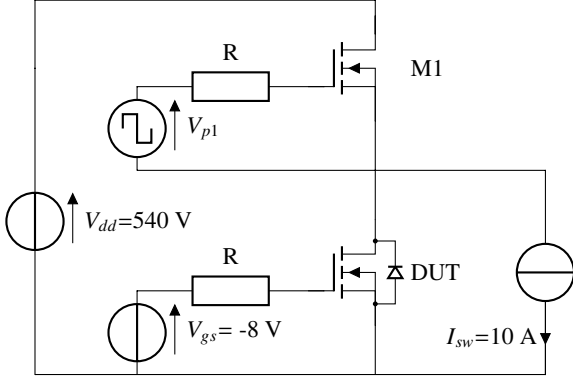


Figure 3: Circuit diagram of the CMB test.

tion mechanism which may occur. For the HTRB test, where no power is dissipated, this simply requires the DUT to be attached to a hot plate at a set temperature of 150 °C. On the contrary, for the other tests from Fig. 2 (Q1, Q3 and Q4), the DUTs dissipate a large amount of power, because of their large drain current, resulting in a noticeable self-heating. To ensure that they still operate at $T_J=150^\circ\text{C}$, they are mounted on temperature-regulated plates. Their thermal resistance “junction-to-plate” ($R_{Th,JP}$) is then characterized using the drain current of the DUT in the saturation region ($V_{gs}=6\text{ V}$, $V_{ds}=8\text{ V}$), both to generate self-heating of the device, and as a Temperature-Sensitive Electrical Parameter (TSEP, [16]) to monitor the corresponding temperature rise. $R_{Th,JP}$ is found to be 2.19 K/W. During the static tests, the drain current is set to 10 A when it flows through the body diode (quadrant Q3) and 16 A when it flows through the channel of the MOSFET (quadrants Q1 and Q4). Both conditions correspond to a power dissipation $P=37\text{ W}$ when the DUT operates at $T_J=150^\circ\text{C}$. As a consequence, the temperature-regulated plates are set to a temperature T_P of:

$$T_P = T_J - P \times R_{Th,JP} = 68.3^\circ\text{C} \quad (1)$$

A summary of the test conditions is given in Tab. 1. Tests in the Q3 quadrant were run for two values of V_{gs} (-5 V and -8 V) as this parameter was found to have a strong effect on the results.

2.2. Dynamic Tests

The circuit diagram used for the dynamic tests is presented in Fig. 3. As can be seen in the theoretical waveforms presented in Fig. 4, the DUT experiences both high voltage when M1 is on, and high current (through its body diode, as the DUT remains off) when M1 is off. This operating mode is referred to as “Chopper-Mode Bias” (CMB).

An arbitrary switching frequency of 20 kHz was chosen for the results presented here, with a 50 % duty cycle ratio between M1 and the DUT. As for the static tests, the devices are attached to a temperature-regulated plate, set at the temperature required to achieve $T_J=150^\circ\text{C}$. The temperature of the plate is calculated using eq. (1), where P is the power dissipated in the DUT when M1 is off.

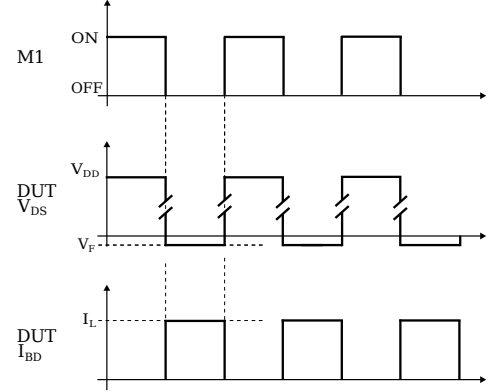


Figure 4: Principle of the CMB test bench: When M1 is in the off-stage, the current flows through the body diode of the DUT. When it is on, the full voltage (540 V) is applied between drain and source of the DUT.

3. Results and Discussion

3.1. Static tests

Fig. 5 presents the measurements of V_F for quadrants 1, 3 and 4. No significant evolution is observed over 100 h: the changes in V_F during the tests are comparable to the experimental scattering, except for Q1, which show a slightly clearer trend, with a 2 % drop in V_F after 15 h. For the HTRB and HTGB tests (not presented here because of space limitations), V_F exhibits no significant change. As for V_F , the evolution of $R_{ds(on)}$ was also measured, but it is not presented here as this parameter shows no significant change, for any of the test conditions (HTRB, HTGB, Q1, Q3 or Q4).

The evolution of V_{th} is plotted in Figs. 7 and 6. It remains essentially constant for the HTRB, HTGB, Q1 and Q4 tests. For Q3, however, V_{th} shows a dramatic drop over time (-40% in 60 h) when the MOSFETs are driven with $V_{gs} = -8\text{ V}$. The tests were repeated on 3 other devices, with $V_{gs} = -5\text{ V}$, a value which still ensures proper blocking of the transistor (initial V_{th} values were found to be 1.12 – 1.45 V). The drop in V_{th} then appears to slow down considerably (orange line in Fig. 7).

Q3 corresponds to the condition in which the biasing current flows through the body diode of the MOSFET (Fig. 2); in Q1 and Q4 the current flows through the channel, while HTRB and HTGB correspond to a voltage-only bias. However, contrary to what was expected, no degradation of the body diode is observed (increase in V_F caused by the propagation of stacking faults). Instead, the devices exhibit a large drop in V_{th} , for the Q3 test condition. Such decrease is undesirable, as it makes the device harder to block, and makes it more vulnerable to electromagnetic interference (which might cause spurious turn-ons).

3.2. Dynamic Tests

Using the CMB setup (Fig. 3), devices from three manufacturers (Wolf speed, ST Microelectronics and Rohm Semiconductors) were tested. The results are given in Fig. 8 for V_{th} (V_F and $R_{ds(on)}$ were also monitored, but as with the static tests, they show no significant evolution). For Wolf speed devices, a large V_{th} drop is observed (Fig. 8). On the contrary, almost no change is observed for ST’s or Rohm’s MOSFETs.

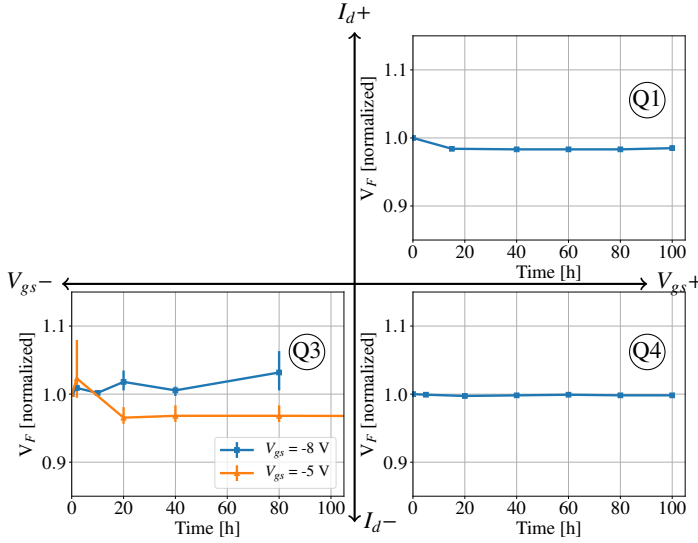


Figure 5: Evolution of the forward voltage of the MOSFETs (normalized for $t=0$, measured at $I_d=10$ A, $V_{gs}=-8$ V, $T_J=25$ °C) during the current-bias tests described in Fig. 2 (3 samples per test for Q1, Q3 and Q4, 10 samples for HTRB). All tests were run at $T_J=150$ °C.

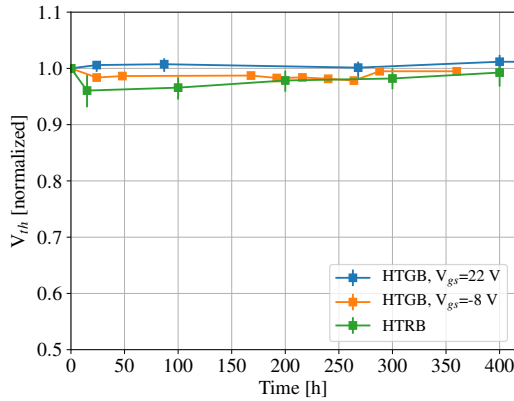


Figure 6: Evolution of the threshold voltage for HTRB (10 samples) and HTGB conditions (1 sample for $V_{gs}=-8$ V, 3 samples for $V_{gs}=22$ V). All tests were run at $T_J=150$ °C.

A comparison between the V_{th} drop observed using the CMB test setup and the static Q3 test setup is presented in Fig. 9. Note that the x-axis corresponds to the time during which current actually flows through the body diode (i.e. 100 % of the test time for Q3, and 50 % of the test time for CMB). Tests were performed using two values of V_{gs} : -5 and -8 V. In both cases, a good agreement is found: most of the V_{th} drop can be associated with the use of the body diode of the DUT.

In an attempt to identify the cause behind the differences in behaviour among components from different manufacturers, additional investigations were conducted. Fig. 10 presents the results of HTGB tests performed on devices identical to those used for Fig. 8. Contrary to the data presented in section 3.1, these tests were run at $T_J=200$ °C, to strongly accelerate ageing. It should be noted that while this temperature is within the allowed range for ST's MOSFETs [17], it exceeds Rohm's (175 °C, [18]) or Wolfspeed's (150 °C, [14]). The high tem-

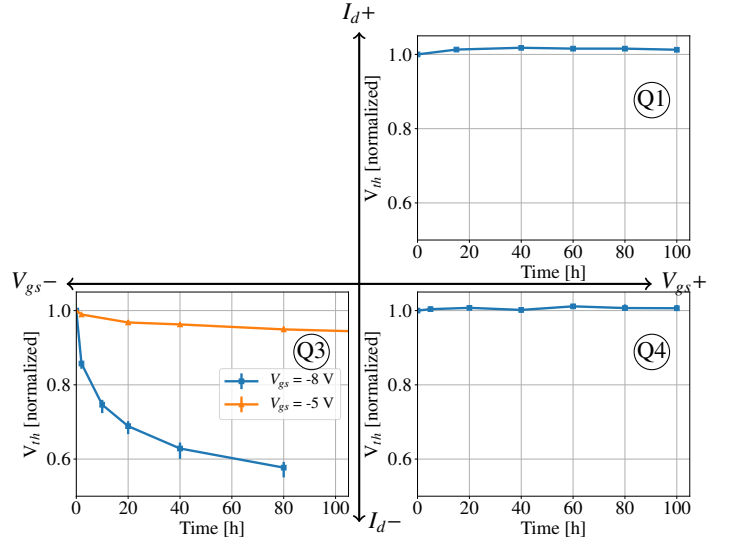


Figure 7: Evolution of the threshold voltage of the MOSFETs (normalized for $t=0$, measured at $I_d=100$ μ A, $V_{dd}=1$ V, $T_J=25$ °C) during the static tests described in Fig. 2 (3 samples per test). All tests were run at $T_J=150$ °C.

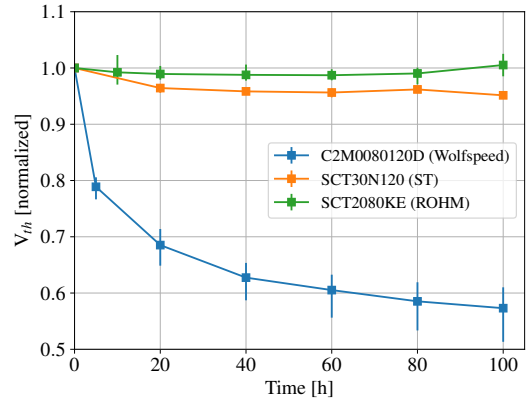


Figure 8: Evolution of the V_{th} of MOSFETs from three different manufacturers, as a function of time in conditions of CMB (3 samples per test), data normalized for $t=0$, measured at $I_d=100$ μ A, $V_{dd}=1$ V, $T_J=25$ °C and $V_{gs}=-8$ V. All tests were run at $T_J=150$ °C.

perature was nonetheless required to observe any difference in behaviour: as can be seen in Fig. 10, while all devices exhibit a small shift in V_{th} (≈ 6 %) within 50 h of test, MOSFETs from ST and Rohm tend to stabilize over time at around a ≈ 10 % increase in V_{th} . On the contrary, Wolfspeed MOSFETs exhibit a continuous increase in V_{th} , with 30 % more over 1000 h. Only positive-bias HTGB tests were performed at 200 °C, because of limited sample availability.

Additionally, cross sections were performed on devices from the three manufacturers. They were prepared mechanically (cut with a diamond saw, and polished using diamond particles down to 1 μ m, followed by 50 nm oxide suspension), and observed using a scanning electron microscope (SEM, Vega 3, Tescan). It is found that all three devices exhibit a planar gate structure, with some differences in the size of their features. The resolution of the images is limited, and very fine details such as oxide thickness cannot be observed clearly. There is,

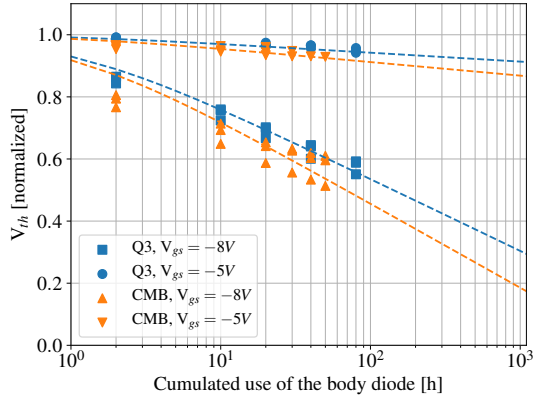


Figure 9: Evolution of the V_{th} as a function of time for the Static (3rd quadrant) and CMB tests (3 samples per test), data normalized for $t=0$, measured at $I_d=100\ \mu\text{A}$, $V_{dd}=1\ \text{V}$, $T_J=25\ ^\circ\text{C}$. All tests were run at $T_J=150\ ^\circ\text{C}$.

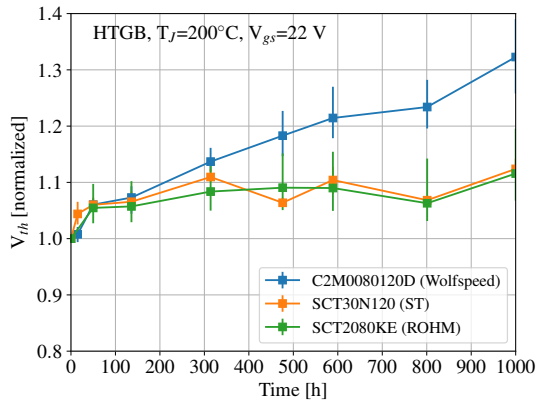


Figure 10: Evolution of the V_{th} for MOSFETs from three different manufacturers, in HTGB conditions ($V_{gs}=22\ \text{V}$), for an ambient temperature of $200\ ^\circ\text{C}$.

however, no obvious geometric parameter which could be correlated with the observed shift in V_{th} .

4. Discussion and Conclusion

Recent SiC MOSFETs were tested, initially to evaluate the extend of know degradation mechanisms in static tests and realistic (switching) conditions: the drift in V_{th} caused by the voltage bias of the gate, and the increase in V_F caused by the propagation of stacking faults in the crystal.

While none of these degradation mechanisms was found to have significant effects in our test conditions (this shows the progress of the SiC MOSFET technology in recent years), we observed a new degradation mechanism: the use of the body diode resulted in a strong drop in V_{th} . In summary, the following conclusions can be drawn from the measurements presented above:

- for the Wolfspeed MOSFETs, static (Q3) and dynamic (CMB) tests have the same consequence, a large V_{th} drop occurring when current flows through the body diode, with comparable time constants in the drop;

- this drop depends on V_{gs} , with a larger change in V_{th} with $V_{gs} = -8\ \text{V}$ ($> 40\ \%$ after 80 h) than with $V_{gs} = -5\ \text{V}$ ($20\ \%$);
- in the absence of current biasing of the body diode (i.e HTRB/HTGB conditions, with only voltage bias, or Q1/Q4 conditions, with current biasing of the channel), no noticeable V_{th} drift is observed at $T_J=150\ ^\circ\text{C}$;
- increasing T_J up to $200\ ^\circ\text{C}$ yields a noticeable V_{th} increase in HTGB conditions, but it remains much slower than that observed for Q3 or CMB tests (hundreds of hours vs. tens of hours)
- devices from different manufacturers (here ST Microelectronics and Rohm Semiconductor) appear to be much less sensitive to this V_{th} drift, which indicates that the issue can be mitigated through improvements in the device design or manufacturing processes;
- the V_{th} drift in Q3 or CMB conditions is correlated with a larger drift in HTGB conditions at $200\ ^\circ\text{C}$ (i.e. it affects Wolfspeed's MOSFETs much more than Rohm's or ST's), but the physical cause remains unknown. Cross sections of the three devices do not show fundamental differences in the geometry of these transistors.

The root cause of this mechanism is not fully understood yet: as depicted in Fig. 1, body diode current and channel current flow through different paths. Charge injection in the channel (which would cause a drift in V_{th}) is therefore unlikely when using the body diode. For the same reason, it is not expected that the channel area would reach a higher temperature when using the body diode, as self heating occurs in a slightly different location. The power dissipation (and therefore the junction temperature) is identical for Q1, Q3 and Q4 tests, so a possible error in the estimation of the junction temperature would affect Q1, Q3 and Q4 test results identically, and yet the V_{th} drift is very different (see Fig. 7). This degradation is relatively severe, as it may make some devices impossible to turn off, or make them very sensitive to voltage transients on the gate within a few tens of hours of operation.

Qualifications test standards, such as HTRB or HTGB, were developed mainly for Si devices. With the development of SiC MOSFETs, some additional tests should be introduced. Here, we describe a very simple static test circuit (the Q3 test setup) which gives results which are consistent with those obtained in switching conditions. As shown in the paper, this test setup is capable of exposing weaknesses which were not visible after HTGB or HTRB tests, and yet may eventually cause some transistors to fail.

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