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Adiabatic Capacitive Logic: a paradigm for low-power logic

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Abstract—Although CMOS technology scaling combined with efficient frequency and voltage scaling strategies offer femto Joule per logic operation, energy consumption remains orders of magnitude above the limit given by information theory. To alleviate this inherent energy dissipation, this paper introduces a new paradigm: the *adiabatic capacitive logic*. Based on adiabatic operation, the principle also relies on a smooth capacitance modulation to achieve a quasi zero-power logic dissipation. This method limits leakage by using metal-metal junctions instead of semiconductor one. It also avoids dynamic power consumption by adiabatic transitions. The contact-less operation promises a better reliability compared to logic based on nano-mechanical relays.

Keywords—*adiabatic logic; mems; low-power; variable capacitor*

I. INTRODUCTION

The classical combinational logic approach is based on the charge and discharge of the equivalent gate capacitor C_o of the n^{th} gate by a constant voltage supply V_{cc} through the resistive channel R_{on} of the $n-1^{\text{th}}$ gate as shown in Fig. 1.a. This particular energy transfer for coding a logic state at the operating frequency f_{sw} leads to an inherent power dissipation equal to $C_o V_{cc}^2 f_{sw}$ due to the charge-discharge cycle. Furthermore, the inherent leakage of semiconductor junctions used in CMOS transistors induces a static power loss $I_{leak} V_{cc}$ which is linked to the threshold voltage V_{th} and the supply voltage ratio. To balance the dynamic and static power losses, the designer has to find the best trade-off between the technology $\{V_{th}, C_L, R_{on}\}$ and design $\{V_{cc}, f_{sw}\}$ parameters. Unfortunately, the energy per operation of the classical CMOS logic is 6 to 10 decades higher than Landauer's theoretical limit of $kT \ln 2$ [1]. CMOS scaling such as modifying the on-off ratio does not drastically change this previous statement. It is

therefore clear that there is room for a new logic coding concept to dramatically reduce the power consumption of the present CMOS digital core. To limit the dynamic loss, $C_o V_{cc}^2 f_{sw}$, the loss-less transformation called adiabatic logic was proven using a CMOS transistor as shown in Fig. 1 [2].

The principle of adiabatic logic is to charge and discharge capacitors at constant current generally by applying a ramping supply voltage instead of a constant voltage. By using this principle, the active power dissipation becomes can be expressed as [1]:

$$P = \frac{RC_o}{T} C_o V_{PC}^2 f_{sw} \quad (1)$$

where R is the on-state resistance of the switch and T is the duration of the power supply ramping. A large reduction is possible if T larger than the product RC_o . Unfortunately using CMOS technology, a non-adiabatic dissipation $C_o V_{th}^2$ appears due to the threshold voltage V_{th} of the transistor. Due to a non-adiabatic threshold voltage effect, this technique reduces by a factor of 10 if V_{th} is assumed to be a third of the supply voltage. But the static loss is not suppressed as it is still based on semiconductor technology and follows the Shockley law. To reduce the static loss, electromechanical relays [3] seem to be a promising approach as their leakage current is only due to surface leakage effects instead of following the Shockley law [4]. In other words, the channel is a metal-to-metal contact instead of a semiconductor barrier [5]. Unfortunately, their poor mechanical reliability, low switching frequencies, and relatively high operating voltages have been highlighted in literature [6,7].

This paper propose a new paradigm to design a combinational ultra-low-power logic from these two existing solutions combined with a new contact-less approach.

II. ADIABATIC CAPACITIVE BASED LOGIC

Fig. 1 shows the basic comparison of a resistive based inverter gate in non-adiabatic and adiabatic operation. Our approach is called adiabatic capacitive logic (ACL). The output load C_o represents the capacitance of the next gates and the interconnect. The timing sequence is similar to adiabatic logic where the power supply is a trapezoidal voltage V_{PC} called the power clock divided in four phases. In our approach, the elementary device is a variable capacitor (VC) called C_{DS} which is controlled by an independent gate terminal V_G . For a Negative-type VC device (NVC) the capacitor value decreases when the gate voltage V_G increases as shown in Fig. 2.

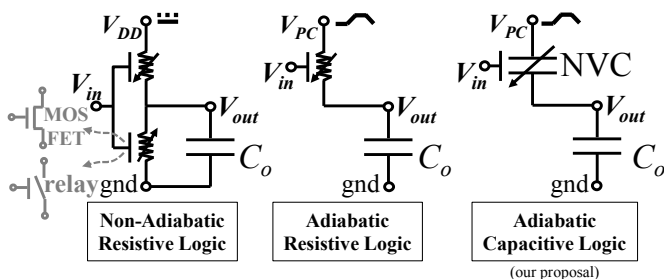


Fig. 1 Basic principle Of the Adiabatic Capacitive Logic for an inverter gate

The variation is the opposite for a positive-type CV (PCV). The $C_{DS}(V_G)$ transfer function is given by the technology of the device implementation. By operating before the electrical contact as a V_C , the physical contact in the device between the two electrodes S and D can be avoided thus improving the device mechanical reliability and avoiding the need for a low contact resistance. Another advantage is the absence of a non-adiabatic dissipation [4].

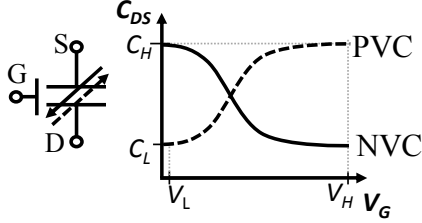


Fig. 2 Example of variable capacitor (VC) device characteristics

For an inverter or a buffer gate, shown in Fig.3, the electrical equations are:

$$V_{PC}(t) = Ri(t) + V_{DS}(V_{in}) + V_{out}(t) \quad (2a)$$

$$i(t) = C_{DS}(V_{in}) \frac{dV_{DS}}{dt} + V_{DS}(t) \frac{dC_{DS}(V_{in})}{dt} \quad (2b)$$

$$i(t) = (C_e(V_{out}) + C_i) \frac{dV_{out}(t)}{dt} + V_{out}(t) \frac{dC_e(V_{out})}{dt} \quad (2c)$$

Where V_{DS} , C_e , C_i and i are the voltage across the variable capacitor, the input capacitance value of the next stages (non-constant), the interconnect capacitance and the current flowing from the supply voltage respectively.

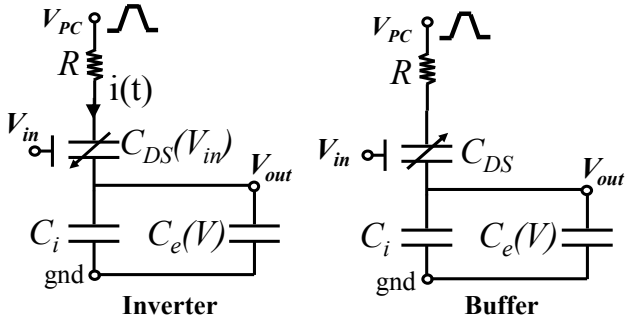


Fig.3 Simplified electrical model of the gate

If the voltage drop across resistor R is neglected and if C_e is supposed constant, it is easy to solve system given in equation (2). Therefore the output logic level is fixed at each given time can be expressed as:

$$V_{out} = \frac{C_{DS}(V_{in})}{C_{DS}(V_{in}) + C_e + C_i} V_{PC} \quad (3)$$

The input voltage variation V_{in} leads to a capacitance variation C_{DS} , then the gate, composed of a capacitor bridge divider, is modulated and transfers (or not) the power clock amplitude to the output node. To distinguish the low and high logic states, the capacitor variation has to be higher than the

load capacitor. In the classical approach, the channel resistance of the transistor is modulated between R_{ON} and R_{OFF} states which then create a resistive bridge between V_{cc} and the output.

In digital adiabatic systems, gates have to be cascaded and the adiabatic condition has to be satisfied [8,9]: during ramp-up and ramp-down of the power-clock voltage, input voltages have to be stable. Fig. 4 shows the waveform of the main signals which is similar to an adiabatic logic sequence. Four equally spaced power clocks are needed to cascade indefinitely the APL gates. The power clock of the next gate is delayed by a quarter of a period e.g. the evaluation phase of n^{th} gate is the hold phase for the $n-1^{th}$ gate.

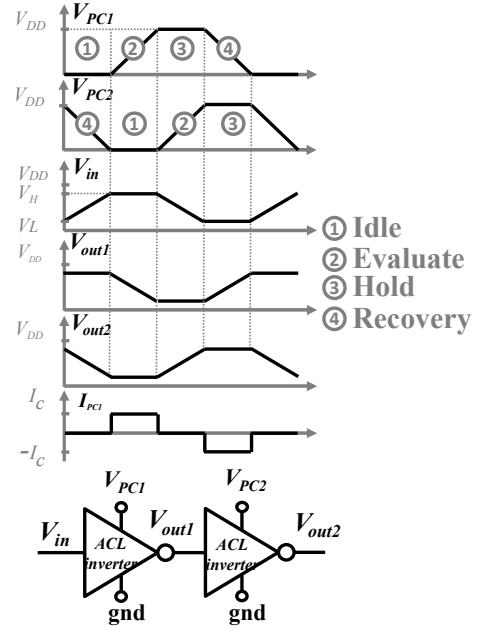


Fig.4 Pipelined Adiabatic Capacitive Logic Architecture

To satisfy the adiabatic condition, the basic gate architecture depicted Fig.3 has to be modified by introducing a supplementary variable capacitor in order to maintain the output voltage in the hold phase when the input is decreasing. Fig. 5 shows the proposed topology for the inverter gate with the complementary input logic state. This technique allows the logic evaluation of the $n+1^{th}$ gate in the third phase without losing the logic state in n^{th} gate. Reset switches with a lower timing constraint have to be introduced to regularly set the static voltage as no DC electrical path exists.

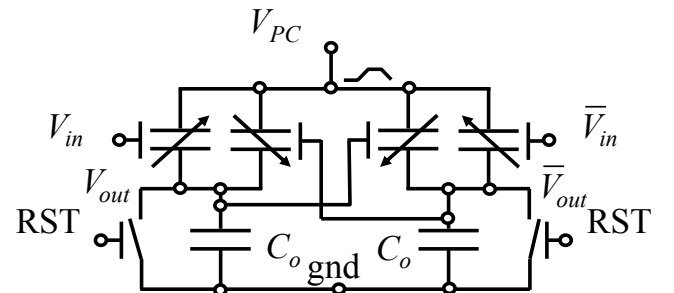


Fig.5 Full Adiabatic Capacitive Buffer-Inverter

By using only NCV and PCV devices, all combinational logic can be generated in ACL. For example, Fig. 6 shows the OR and NOR logical parts of the gates. Notice the gate does not need any complementary device as in the resistive logic (Fig. 1). The complementary logic state is achieved by the charge/discharge of the output capacitor by the same device.

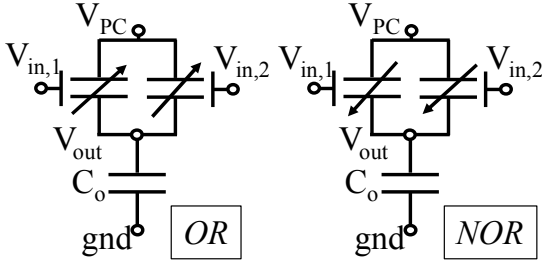


Fig. 6 Basic combinational logic functions in ACL

If the capacitance transfer functions $C_{P,N}(V_G)$ are correctly chosen, V_L and V_H values code distinguished low and high logic states during the third phase. As the power clock regenerates the signal amplitude at each stage, the logical states amplitudes are maintained over the whole logic depth. The PC current $i(t)$ is a quasi-square waveform as it provides the energy to charge the output capacitance in phase 2 then give back this energy in phase 4. This behavior implies a charge recovery supply.

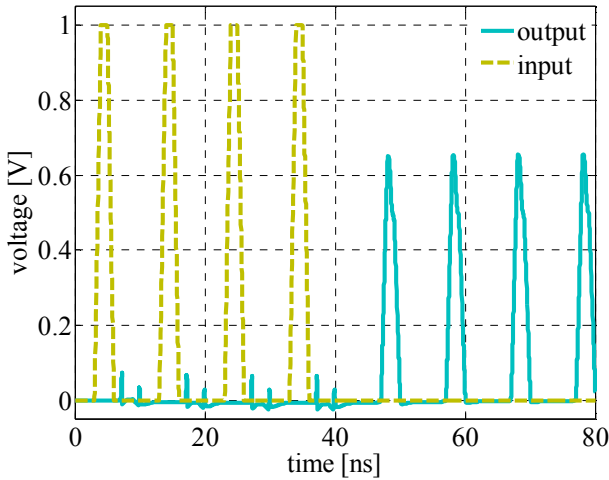


Fig. 6 Simulations of output signal in a series of 4 inverters

To prove the ability to code logic states and maintain this level during the holding period, Fig.6 shows a particular example with an arbitrary voltage to capacitor transfer function. The signals called input and output are the input signal and output signal of a four adiabatic capacitive inverters. The binary input word is “1 1 1 1 0 0 0 0”. The transfer functions of PVC and NVC capacitors are inspired from Fig.2 and are given by the following relation:

$$\begin{aligned} C_{DS} &= A + B \tanh a(V_G - V_{TP}) \\ C_{DS} &= C - D \tanh b(V_G - V_{TN}) \end{aligned} \quad (4)$$

$A, B, C, D, a, b, V_{TP}, V_{TN}$ are adjusted parameters. The simulation uses the following values:

$$\begin{aligned} C_0 &= C_{DS\max} = 1fF ; C_{DS\min} = 0.01fF ; V_{PC\max} = 1V ; \\ a &= 10 ; b = 50 ; V_{TP} = 0.3V ; V_{TN} = 0.2V \end{aligned}$$

III. USE OF ELECTROMECHANICAL DEVICES

The key challenge is being able to define the scalable hardware necessary to implement the elementary CV devices. To modulate capacitor values, the plate surface, dielectric thickness between the two electrodes and permittivity could be used. Fig. 7 shows a viable candidate for CV implementation, where the gap between the MEMS electrodes is modulated by electrostatic force applied through the gate voltage. Hence the C_{DS} is modulated by the gate voltage which is electrically isolated from the drain and source terminals. The variable gate capacitance C_G of the n^{th} gate is then the load C_o of the $n-1^{\text{th}}$ gate. Other physical phenomena could also be used such as piezo or ferroelectric materials. The main objective is to achieve a sub-volt actuation and to reduce the power clock amplitude in order to decrease the adiabatic loss due to the resistive path R and the loss due to the mechanical damping effect.

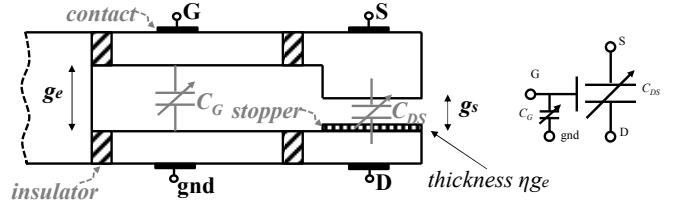


Fig. 7 NVC device implementation using electrostatic MEMS

It is very important to notice that in this device implementation, the complementary device are not needed to hold the logic state during the holding state. The hold function is created in the variable capacitor C_{DS} itself thanks to the residual electrical field. In order to calculate output signals and dissipated energy in series of four buffers, it is necessary to include the electromechanical model of the variable capacitor instead of writing the transfer function of the capacitor. The mechanical equation is written as:

$$m \frac{d^2x}{dt^2} + \frac{\sqrt{km}}{Q} \frac{dx}{dt} + kx = \frac{\epsilon_0 S_G V_G^2}{2(g_e - x)^2} + \frac{\alpha \epsilon_0 S_G V_{DS}^2}{2(g_s - x)^2} \quad (5)$$

The variables $x, m, k, Q, \epsilon_0, S_G, \alpha S_G, \eta_{ge}$ are the displacement of the beam, the mass of the beam, the spring constant, the quality factor of the beam, the vacuum permittivity, the areas of input and output capacitors, and the thickness of the stopper respectively.

It is now interesting to define normalized variables:

$$\begin{aligned} \tilde{x} &= x/g_e \quad \tilde{t} = t/t_0 \quad \tilde{V} = V/V_0 \quad \lambda = 1/Q \quad \tilde{r} = g_s/g_e \\ V_0 &= \sqrt{kg_e^3/\epsilon_0 S_G} \quad t_0 = \sqrt{m/k} \\ C_{DS} &= \frac{\alpha \epsilon_0 S_G}{g_e(\tilde{r} - \tilde{x})} ; C_G = \frac{\epsilon_0 S_G}{g_e(1 - \tilde{x})} ; \tilde{C}_{DS} = \frac{C_{DS}}{C_0} ; \tilde{C}_G = \frac{C_G}{C_0} \\ C_0 &= \frac{\epsilon_0 S_G}{g_e} ; i_0 = \frac{C_0 V_0}{t_0} ; \tilde{R} = R/\left(\frac{V_0}{i_0}\right) ; \tilde{i}(t) = i(t)/i_0 \end{aligned}$$

The result of the electromechanical simulation is shown in Fig.8 for an input signal “1 1 0 0” with the following parameters:

$$\varepsilon_0 S_G / g_e = 0.25 fF ; C_i = 0.25 fF ; \alpha = 0.01 ; r = 0.25$$

$$\eta = 0.01 ; \lambda = 2 ; \tilde{V}_{pc} \max = 1 ; \tilde{R} = 0.1$$

The limit in beam displacement introduced by the stopper is modelled by injecting an additional restoring force. C_e is supposed to be equal to $C_G + C_i$.

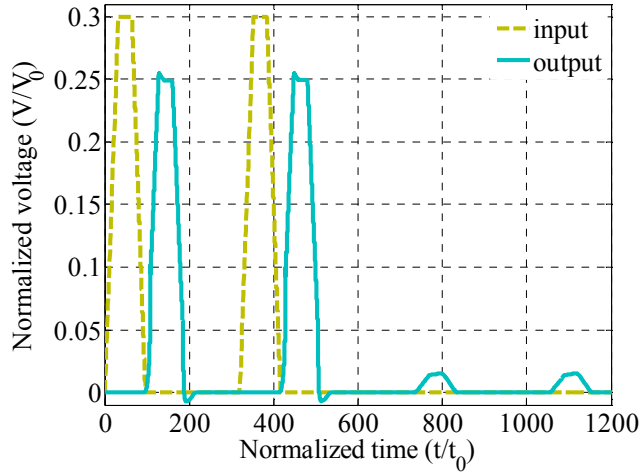


Fig.8 Input of the first gate and output of the third gate in a serie of 4 buffers

In this particular example, the ratio between the dissipated energy in the ACL gates and the energy dissipated in an equivalent CMOS gates is 0.02. This result proves the proposed approach can reduced the power dissipation of the CMOS logic by 50x.

IV. COMPARISON WITH OTHER LOGIC STYLES

The key differences with ACL are summarized in Table 1. As the adiabatic logic is based on relay, its static loss is close to zero as it relies on metal-oxide-metal junction. The main benefit of the proposed ACL approach is to avoid the non-adiabatic residue as the capacitor is only modulated instead of switched between on- and off-states in relay counterpart. This contact-less operation also reduces the mechanical contact degradation problem faced in relays. In other part, it reduces the operation frequency as the expected time to modulate the capacitor is significantly longer than the on-to-off switch in CMOS device. Moreover, the smooth transition needed in any adiabatic logic families reduces the frequency. Finally, non-compatible CMOS process is required.

	Non-Adiabatic Resistive Logic	Adiabatic Resistive Logic		Adiabatic Capacitive Logic
Device	MOSFET	MOSFET	MEMS	VC
Power supply	constant	trap-zoidal	trap-zoidal	trap-zoidal
Dynamic loss (non-adiabatic)	$C_0 V_{cc}^2$	$C_0 V_{th}^2$	$C_0 V_{po}^2$	~ 0
Dynamic loss (adiabatic part)	NA	$R_{onm} C_0 / T \times C_0 V_{dd}^2$	$R_{onm} C_0 / T \times C_0 V_{dd}^2$	$R_c C_0 / T \times C_0 V_{dd}^2$
Static loss	$I_{leak} V_{cc}$	$I_{leak} V_{cc}$	~ 0	~ 0
Normalized operating frequency	10	1	0.1 ⁽¹⁾	0.1 ⁽¹⁾
Device Reliability	High	High	Low ⁽²⁾	High ⁽³⁾

Table 1: Logic comparison at a glance

V_{po} release voltage of relay, R_{om} and R_{onm} are on-state resistances for transistors and MEMS, respectively, R_c is the interconnect resistance in a capacitive gate, (1) mechanical time constant is larger than the electrical one, (2) mainly due to the contact, (3) expected as it is a contact-less operation.

V. CONCLUSION

Based on variable capacitor technology it is possible to implement adiabatic capacitive logic (ACL) which is an innovative approach leading to ultra-low inherent static or dynamic energy dissipation hence reducing the power consumption of the existing CMOS digital core by a several decades. ACL is based on two main principles: adiabatic energy transfer and metal-to-metal junctions without physical contact, thus improving the reliability compared to logic based on MEMS relays. This proposal therefore offers new means for near-zero power consumption logic.

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