Contactless Capacitive Adiabatic Logic

Yann Perrin, Ayrat Galisultanov, Hatem Samaali, Philippe Basset, Hervé Fanet, Gaël Pillonnet

Contactless Capacitive Adiabatic Logic

Yann Perrin[a], Ayrat Galisultanov[a], Hatem Samaali[b], Philippe Basset[b], Hervé Fanet[a], and Gaël Pillonnet[a]

[a]Univ. Grenoble Alpes, CEA LETI, F-38000 Grenoble
[b]Univ. Paris-Est/ESYCOM/ESIEE Paris, Noisy-le-Grand 93162, France

ABSTRACT

CMOS technology allows a femto Joule energy dissipation per logic operation, if operated at optimal frequency and voltage. However, this value remains orders of magnitude above the theoretical limit predicted by Landauer. In this work, we present a new paradigm for low power computation, based on variable capacitors. Such components can be implemented with existing MEMS technologies. We show how a smooth capacitance modulation allows an energy-efficient transfer of information through the circuit. By removing electrical contacts, our method limits the current leakages and the associated energy loss. Therefore, capacitive logic must be able to achieve extremely low power dissipation when driven adiabatically. Contactless capacitive logic also promises a better reliability than systems based on MEMS nanorelays.

Keywords: Low-power electronics, MEMS, Adiabatic architectures, Capacitive logic gates, Energy efficiency

1. INTRODUCTION

Adiabatic logic is a promising approach explored in order to reduce the energy of computation.[1–3] The principle of adiabatic logic is to limit the dynamical losses by using smooth transitions between the logic states.[4] This generally implies to work at lower operating frequencies. However, adiabatic operation of CMOS circuits exacerbates the leakage loss intrinsic to field-effect transistors (FET).[5] In addition, the non-linearity of FETs leads to an unavoidable energy loss.[2] In order to avoid leakage loss, circuits based on MEMS nanorelays have been investigated.[6,7] Although nanorelays are a promising approach for implementing adiabatic logic, the electrical contact at the nanometer scale raises serious reliability issues.[8]

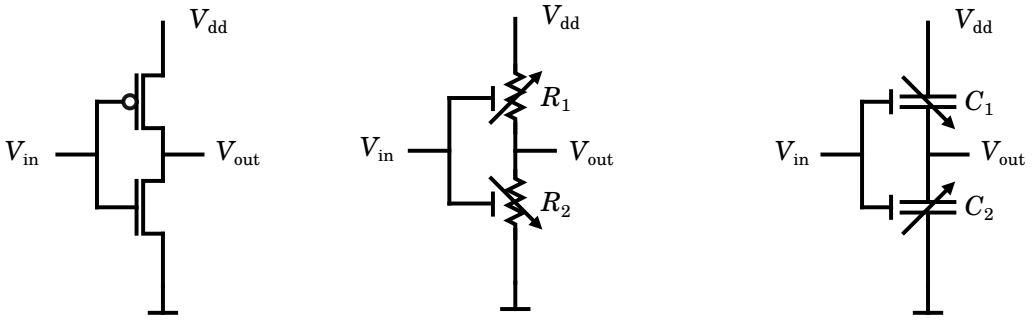

Figure 1. A conventional CMOS inverter (left) can also be seen as a bridge of variable resistors (middle). By analogy, a bridge of variable capacitors should also perform the logic function (right).

In earlier works, we presented a disruptive approach, where combinational functions are performed with variable capacitors:[9,10] combinational CMOS gates, such as the inverter depicted in Figure 1, can also be seen as a circuit with voltage-controlled variable resistors. The output voltage is then determined by the resistances values. The logic function also might be performed by variable capacitors (see Fig. 1). Capacitive logic should

Further author information: E-mail: gael.pillonnet@cea.fr

avoid the dissipation caused by leakage currents. When driven adiabatically (Capacitive Adiabatic Logic, CAL) the energy dissipated by the gate becomes almost negligible. A variable capacitor can simply be obtained by coating the plates of a nanorelay with a dielectric layer. However, the hysteretic behaviour of this system causes an unavoidable dissipation.[10] In this study, we present a new approach which does not involve mechanical contact, and that could be a good candidate for implementing adiabatic dynamic logic (ADL) architectures.[11]

2. VOLTAGE CONTROLLED CAPACITANCE

The elementary device for capacitive adiabatic logic (CAL) consists of a two-terminals variable capacitor that can be controlled by an external voltage. This can be achieved in a solid state device (eg. varicap diode), or electromechanically by using for instance comb-drive actuators.

2.1 two-terminals comb-drive actuator

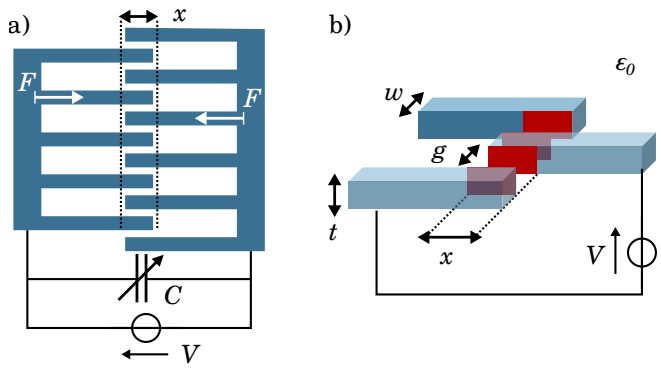

Figure 2. a) Image depicting a typical comb-drive actuator, composed of two conducting parts with interdigitated fingers. An electrostatic attractive force arises when a voltage difference is applied to the combs. b) Detailed schematics of the fingers, showing the notations employed in this paper. Only the red area is taken into account for the calculation of the capacitance.

Comb-drive actuator[12] is probably the most popular device employed for MEMS. It allows to create significant electrostatic forces, while involving extremely low electric currents. It consists of two insulated parts in electrostatic influence (See Figure 2a). The electrostatic coupling is enhanced by the presence of interdigitated fingers, overlapped by a length denoted x. When the fringing electric field is ignored, the capacitance of this comb-drive writes:

$$C(x) = \begin{cases} \dfrac{2n\epsilon_0 t x}{g} & \text{if } x \geq 0 \\ 0 & \text{otherwise.} \end{cases} \tag{1}$$

where ϵ_0, t, n and g are respectively the vacuum permittivity, the thickness of the device, the number of fingers and the gap between them. $C(x)$ increases with the displacement x. As a consequence, when a voltage V is applied between the two combs, an electrostatic attractive force F arises. Its magnitude can be calculated by differentiating the electrostatic energy with respect to x:

$$F(x,V) = \begin{cases} \dfrac{\partial}{\partial x}E = \dfrac{1}{2}\dfrac{\partial C}{\partial x}V^2 = \dfrac{nt}{g}\epsilon_0 V^2 & \text{if } x \geq 0 \\ 0 & \text{otherwise.} \end{cases} \tag{2}$$

If one (or both) combs are able to move along the x direction, $F(x,V)$ leads to a mechanical displacement which increases $C(x)$. Therefore, comb-drive actuator is a variable capacitor.

2.2 Four-terminals variable capacitor

The two-terminals variable capacitor described above cannot provide the external control of the capacitance, which is required to perform logic functions (see Fig. 1). To this purpose, we must add another pair of electrodes connected mechanically to the first one. On the device depicted in Figure 3a, the left electrodes correspond to the input, and the right electrodes to the output. By analogy with FET transistors, input and output capacitances (resp. voltages) are denoted C_G (resp. V_G, gate) and C_{DS} (resp. V_{DS}, drain-source). The output comb-drive is symmetric ; the interest of this design is that the system becomes insensitive to the effect of V_{DS} (when V_G=0). This property is verified even when considering fringing fields.

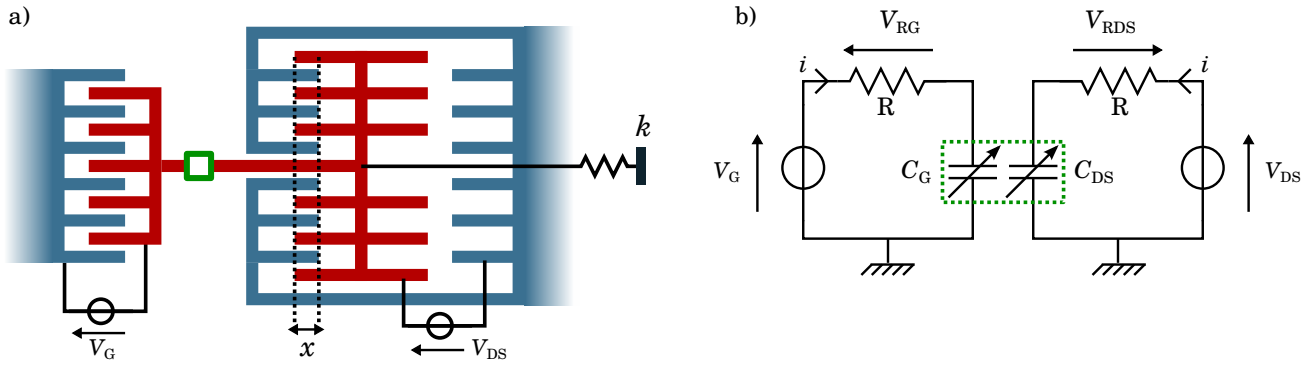

Figure 3. a) Sketch of the four-terminal variable capacitor studied in this paper. The blue elements are anchored to the substrate and are electrically insulated. The red part is free to move along the horizontal axis. A spring with a stiffness k creates a restoring force $F_k = -kx$. It tends to bring back the rotor to the position $x = 0$. The left comb-drive corresponds to the input electrodes. The right comb-drive (output) is mechanically connected to the first one, but both are electrically insulated. The green square depicts the insulating mechanical link. b) Equivalent electric diagram, showing the two electric loops coupled mechanically.

In our design, input and output comb-drives have initial overlaps denoted x_0 and x'_0 when $x = 0$. The capacitances $C_G(x)$ and C_{DS} then write:

$$\begin{aligned} C_G &= \frac{2n\epsilon_0 t}{g}(x + x_0)H(x + x_0) \\ C_{DS} &= \frac{2n'\epsilon_0 t}{g}\left[(x + x'_0)H(x + x'_0) + (x'_0 - x)H(x'_0 - x)\right] \end{aligned} \tag{3}$$

Where $H(x)$ corresponds to the Heaviside step function, which equals 0 if $x < 0$ or 1 if $x \geq 0$. n' depicts the number of fingers in the output comb-drive. In order to enhance the variation of C_{DS} capacitance, the numbers of fingers is usually greater in the output ($n' > n$).

Considering damping and inertia, the mechanical dynamic equation of the system writes:

$$\frac{\mathrm{d}^2x}{\mathrm{d}t^2} + \frac{\omega_0}{Q}\frac{\mathrm{d}x}{\mathrm{d}t} + \omega_0^2 x + \frac{F(x, V_G, V_{DS})}{m} = 0 \tag{4}$$

where m is the mass of the rotor, $\omega_0 = \sqrt{\frac{k}{m}}$ its angular frequency, and Q the quality factor of the oscillator (this includes the mechanical damping). $F(x, V_G, V_{DS})$ corresponds to the total electrostatic force resulting from input and output comb-drives.

Equations (2),(3) and (4) allow the calculation of the output capacitance C_{DS} for a set of applied voltages (V_G, V_{DS}). For the calculations presented in this paper, the parameters are set to the following values:

- Thickness: t=40 µm
- Gap: g=2 µm

- Numbers of fingers: n=100, n'=200
- Initial overlaps (for x=0): x_0=5 µm, x'_0=−2 µm
- Spring stiffness: k=2 N.m^{-1}
- Resonant frequency $\frac{\omega_0}{2\pi}$=10 kHz
- Quality factor $Q = 10$
- Vacuum permittivity: ϵ_0= 8.85 × 10^{-12} F.m^{-1}

This high thickness is required in order to obtain significant capacitances values, making the system insensitive to parasitic capacitances. The gap is set by the precision of the fabrication process. The number of fingers n and n' is must be sufficiently high in order to permit actuation voltages in the range of 10 volts. These features are compatible with realistic device which are commonly used, eg. as gyroscopes.[13] Figure 4 clearly show that V_G provides a fine tuning of C_{DS} for values greater than 10 V. This offset is due to the negative initial overlap x'_0=−2 µm which has been designed on the output comb-drive. This choice will be discussed further.

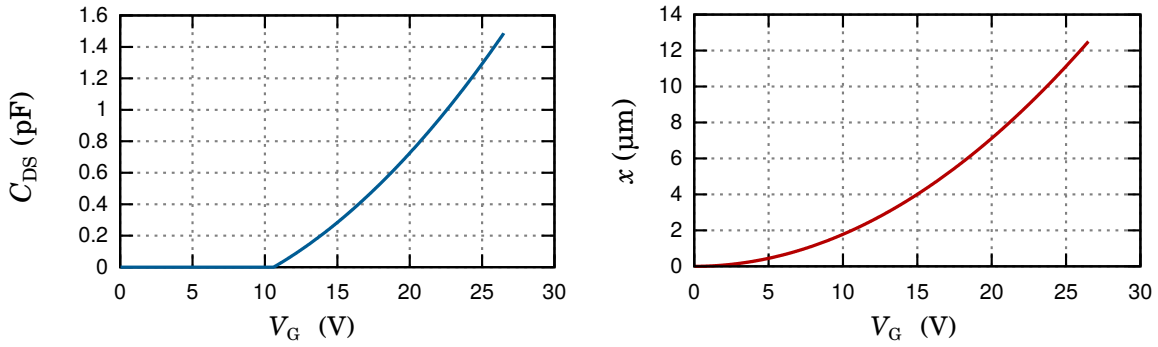

Figure 4. Graphs depicting the influence of the input voltage V_G on the output capacitance C_{DS} and the position of the rotor x.

In order to simulate accurately the system and the dissipation, we also must consider the electrical aspects. The electrical diagram consists of simple RC circuits, in which the electric current i expresses:

$$i(t) = \frac{1}{R}(V_G(t) - \frac{q(t)}{C(t)}) \tag{5}$$

where C refers to the capacitance C_G or C_{DS}, and q to the charge stored inside. q is calculated by integrating the current:

$$q(t) = \int_0^t i(t)\mathrm{d}t \tag{6}$$

Equations (5) and (6) fully describe the electrical evolution of the system. The link between electrical and mechanical equations originates from the variation of the capacitances and the electrostatic forces. In the following paragraph, the electromechanical model is solved numerically for a more complex system.

3. CASCADED BUFFERS

We now consider a circuit composed of four cascaded CAL buffers. The equivalent electric diagram is depicted in Figure 5. While keeping the numerical parameters detailed above, we study the dynamical response of the circuit to an input logic sequence 0 1 0 1. According to adiabatic dynamic logic (ADL) principles,[11] the four power clocks signals V_{PC1} to V_{PC4} have a trapezoidal shape (see Fig. 6a). In addition, a phase-shift about $\frac{\pi}{2}$ is introduced between each clock. Different approaches for generating such signals have already been investigated, such as resonant circuits or switched capacitors.[14,15]

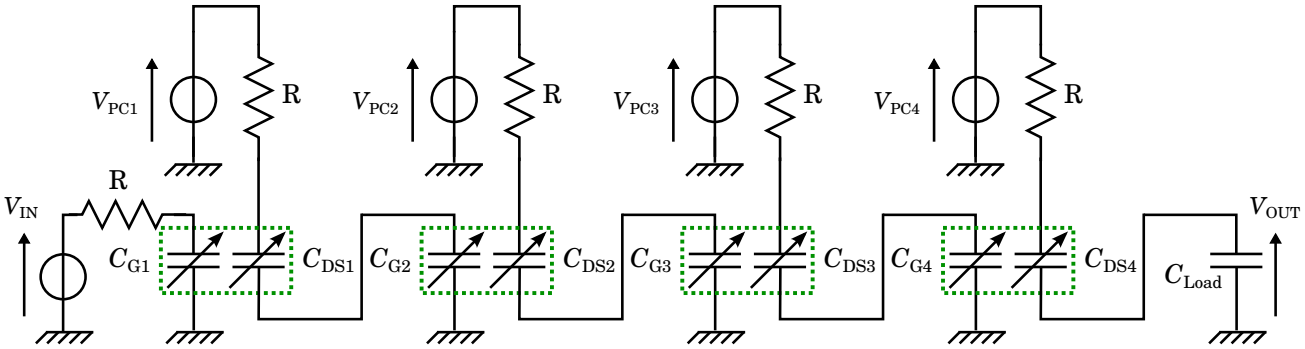

Figure 5. Electrical diagram of the four cascaded buffers considered in this section. The capacitance C_{Load} connected on C_{DS4} imitates the input of a following circuit.

Figure 6b depicts the dynamical response of the circuit for a specific input. The output signal clearly shows two different logic states, respectively at 2 V ("0" state) an 15 V ("1" state). The logic sequence in the output corresponds to the input, which is the expected behaviour for cascaded buffers. The output is delayed by one time period ; this feature is intrinsic to ADL operation. For the proper functioning of the gate, the operating frequency must be lower than the mechanical resonant frequency (10 kHz). In addition, the parasitic oscillations that occur after a "1" state must be damped before the next clock pulse. These constrains limit the operating frequency up to approximately 1 kHz.

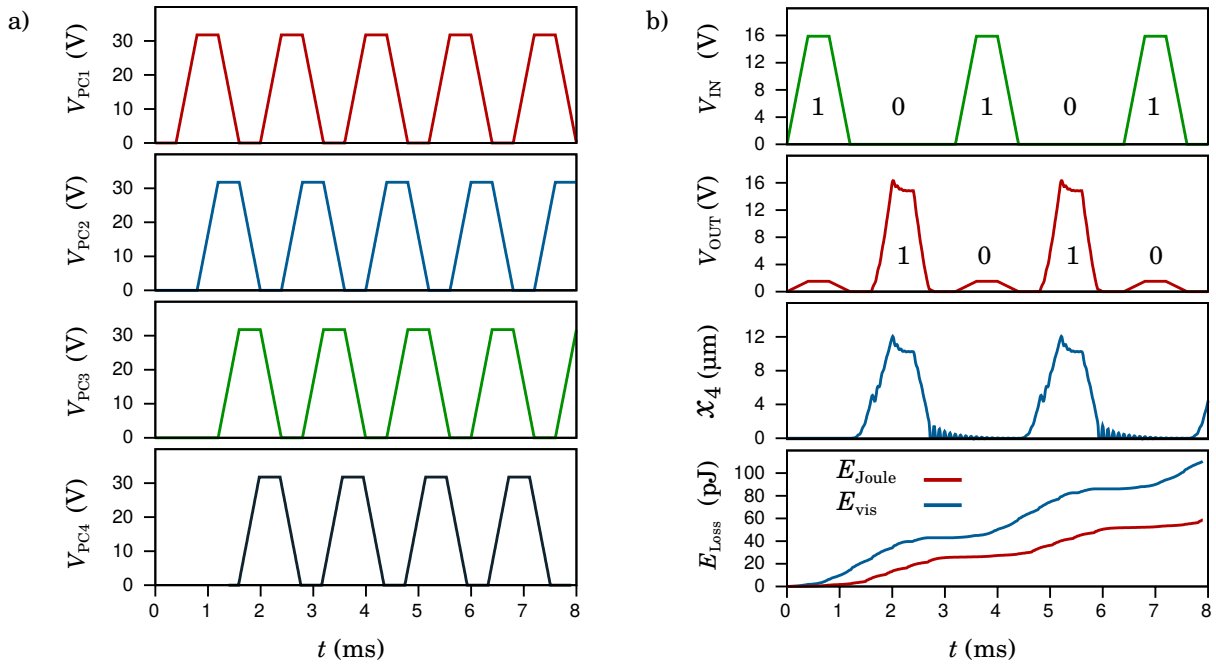

Figure 6. a) Graphs showing the four phases power clock signals employed in the simulations. The circuit is driven with an operating frequency about 632 Hz. b) Response of the circuit to an input signal carrying the logic sequence 1-0-1-0-1 (first graph). The output signal (second graph) is shifted by one time period (1.58 ms) and shows the expected logic sequence. This sequence is also visible on the position of the last comb-drive device (third graph).

We verified that the systems works properly for an operating voltage $V_{dd} > 20$ V. Under this value, "1" states are converted into "0" states. This is due to the negative overlap x_0'=-2 µm, which requires a motion of at least 2 µm in order to transmit "1" states. One could conclude that removing this overlap might allow to work at lower voltages. However, the voltage that corresponds to "0" state (2 V) triggers a motion in the following comb-drive. This motion must not trigger a "1" state in the circuit. Therefore, the negative overlap is required

in order to secure the system against fluctuations associated to "0" states.

We finally address the question of the energy dissipation in the circuit. Two sources of dissipation are considered: the Joule dissipation E_{Joule} in the resistances (R is set to 2 MΩ), and the damping loss E_{vis} in the moving parts ($Q = 10$). Both dissipation terms appears in the last graph of Figure 6b over the time. Most of the dissipation occurs when a "1" state is transmitted, as it is associated to large displacements and high capacitances variations. With the conditions of Figure 6, the energy per operation E_{op} is about 7.5 pJ. We point out that this dissipation is only a small fraction (5%) of the energy involved in the process. During the rise of the clock pulse, the power clock provides energy which is stored electrically in the capacitances and mechanically in the springs. During the decrease of the pulse, this energy is substantially recovered by the power clock. In the simulation in Figure 6, the ratio of recovered energy is about 95%. This ratio assumes a perfect (lossless) power clock.

In our system, E_{op} is far beyond the state of the art of conventional nanoscale CMOS circuits (in the order of the fJ). However, this dissipation should vanish for extremely low operating frequencies, i.e. when the system is driven adiabatically. Furthermore, the energy per operation dramatically decrease with the size of the device (E_{op} scales in g^{-3}). Therefore, passing from a microscale device to nanoscale might lead to a reduction of E_{op} by six orders of magnitude (in the order of aJ).

4. CONCLUSION

This paper introduces an original approach for implementing adiabatic dynamic logic with contactless MEMS devices. Our design avoids leakage losses, which are the biggest limitation for adiabatic circuits based on field-effect transistors. The elementary device presented here is based on comb-drive actuators which allows the realisation of a voltage-controlled variable capacitor. Based on an electromechanical model, we show how these components can be arranged in order to perform a basic combinational function (buffer pipeline). Further studies will be dedicated to other functions (inverter, AND, OR...) that can be performed with capacitive logic.

REFERENCES

[1] Koller, J. G. and Athas, W. C., "Adiabatic switching, low energy computing, and the physics of storing and erasing information," in [*Workshop on Physics and Computation*], 267–270 (Oct 1992).

[2] Athas, W. C., Svensson, L. J., Koller, J. G., Tzartzanis, N., and Chou, E. Y.-C., "Low-power digital systems based on adiabatic-switching principles," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* **2**, 398–407 (Dec 1994).

[3] Snider, G. L., Blair, E. P., Boechler, G. P., Thorpe, C. C., Bosler, N. W., Wohlwend, M. J., Whitney, J. M., Lent, C. S., and Orlov, A. O., "Minimum energy for computation, theory vs. experiment," in [*2011 11th IEEE International Conference on Nanotechnology*], 478–481 (Aug 2011).

[4] Paul, S., Schlaffer, A. M., and Nossek, J. A., "Optimal charging of capacitors," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* **47**, 1009–1016 (Jul 2000).

[5] Chandrakasan, A. P. and Brodersen, R. W., "Minimizing power consumption in digital cmos circuits," *Proceedings of the IEEE* **83**, 498–523 (Apr 1995).

[6] Houri, S., Valentian, A., and Fanet, H., [*Comparing CMOS-Based and NEMS-Based Adiabatic Logic Circuits: 5th International Conference, RC 2013, Victoria, BC, Canada, July 4-5, 2013. Proceedings*], 36–45, Springer Berlin Heidelberg, Berlin, Heidelberg (2013).

[7] Ayala, C. L., Bazigos, A., Grogg, D., Pu, Y., and Hagleitner, C., "Ultra-low-energy adiabatic dynamic logic circuits using nanoelectromechanical switches," in [*2015 IEEE International Symposium on Circuits and Systems (ISCAS)*], 2596–2599 (May 2015).

[8] Pawashe, C., Lin, K., and Kuhn, K. J., "Scaling limits of electrostatic nanorelays," *IEEE Transactions on Electron Devices* **60**(9), 2936 (2013).

[9] Pillonnet, G., Fanet, H., and Houri, S., "Adiabatic capacitive logic: a paradigm for low-power logic," in [*IEEE International Symposium of Circuits and Systems ISCAS*], (2017).

[10] Galisultanov, A., Perrin, Y., Fanet, H., and Pillonnet, G., "Capacitive-based adiabatic logic," in [*9th International Conference, RC 2017, Kolkata, India, July 6-7, 2017, Proceedings*], Phillips, I. and Rahaman, H., eds., 52–65, Springer International Publishing, Cham (2017).

[11] Dickinson, A. G. and Denker, J. S., "Adiabatic dynamic logic," *IEEE Journal of Solid-State Circuits* **30**, 311–315 (Mar 1995).

[12] Tang, W. C., Nguyen, T. C. H., and Howe, R. T., "Laterally driven polysilicon resonant microstructures," in [*Micro Electro Mechanical Systems, 1989, Proceedings, An Investigation of Micro Structures, Sensors, Actuators, Machines and Robots. IEEE*], 53–59 (Feb 1989).

[13] Yazdi, N., Ayazi, F., and Najafi, K., "Micromachined inertial sensors," *Proceedings of the IEEE* **86**, 1640–1659 (Aug 1998).

[14] Jeanniot, N., Todri-Sanial, A., Nouet, P., Pillonnet, G., and Fanet, H., "Investigation of the power-clock network impact on adiabatic logic," in [*2016 IEEE 20th Workshop on Signal and Power Integrity (SPI)*], 1–4 (May 2016).

[15] Raghav, H. S., Bartlett, V. A., and Kale, I., "Investigation of stepwise charging circuits for power-clock generation in adiabatic logic," in [*2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*], 1–4 (June 2016).