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**Title:**

*FPGA implementation of a video-based system for GNSS reception characterization along a railway line*

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**Introduction**

Train location is of main use in railway signaling applications. Currently, sensors are installed along the lines to detect the presence of a train. These sensors are called balises and balise reader aboard a train can be used to detect them. The balise initializes the odometer, and the train position is computed by the odometer as a distance run since the last relevant balise group. However, because of the high cost of these devices and their maintenance, the use of Global Navigation Satellite Systems (GNSS) is investigated in order to let the train provide itself its position instantaneously and allow removing as much as possible track-based systems. Its introduction is developed in the framework of the European ERTMS standards, via the introduction of the virtual balise concept. The virtual balises are virtual points, recorded in an embedded geographic database. These points can be the coordinates of the real (removed) physical balises. The goal of the virtual balise concept is to detect the position of the train when passing over the identified points by comparing the GNSS-based location of the train with the database. The train delivers then the same telegram that would have been sent with the use of the physical balise. As such, the process could be as transparent as possible for the global system.

The longer term advantages of such an evolution would be to increase the frequency of the trains and to reduce the energy consumption, thanks to adapted algorithms that optimizes the speed of circulation with respect to the profile of the lines.

Furthermore, in applications where a high accuracy is needed, the GNSS performance is not efficient enough due to several errors (multipath, atmospheric errors, lower power of the signal...). Here, the use of complementary sensors in addition to the navigation system becomes necessary.

**Methods**

In this context, the EU ERSAT GGC starting project intends to work on methodologies for the characterization of the lines in order to evaluate opportunities of virtual balises concept and its use efficiency. This paper presents an intelligent architecture of real-time geo-location system consisting of a video acquisition system, a GNSS navigation system and a hardware interface allowing the control of the sensors as well as the synchronization, the processing and the fusion of the data coming from the different devices.

First, the on-board processing algorithm permits to detect the presence of masking obstacles in the local environment and thus to characterize the reception environment of the GNSS signals along real lines. The second contribution is to identify the reception state of the satellites in order to be able to weight the received signals depending on their signal quality and thus increase GNSS-based performance.

Although there is a wide study of algorithms to evaluate multi-sensor fusion, not many studies are interested to use small size, flexible and low cost platforms, which is a challenge in the next generation of navigation systems. Therefore, our contribution is to develop an embedded system that combines and merges different data sets around a novel architecture based on FPGA technology.

**Results**

An Altera DE4 evaluation kit powered by Stratix-4 GX FPGA was used for building the real-time navigation system with the 32-bit embedded-processor architecture in its core running at up to 300MHz. This board is characterized by its lowest power consumption with up to 50 percent lower power than any other high-end FPGA in the market enabled by 40 nm benefits and Programmable Power Technology.

The first step of designing an FPGA-based system is the description of its functional requirements. In the case of current solution, the system modules are as follows:

- 1- Interface with the Ublox evaluation kit which includes the M8T GNSS chip using the Universal Asynchronous Receiver Transmitter (UART) serial communication interface. A UART receiver module is developed in Very High-level Design Language (VHDL) to synchronize GNSS reading data at a rate of 1 Hz relative to the PPS synchronization signal and a baud frequency of 9600 bps.
- 2- Interface with the full HD fish-eye camera system which generates a panoramic video stream of the environment using the High Definition Multimedia Interface (HDMI) transmission protocol. The camera is installed on the top roof of the train, recording the sky view at a frequency of 60 frames per second. A hardware module is developed to decode video data according to the HDMI protocol.
- 3- Extract data information from both sensors to get the GNSS time, position and satellite-related information from the GNSS receiver and image data from the camera. The GNSS chip is configured once time, on out-line, to generate UBX data. On each new PPS signal, a new packet of data is sent. Each packet integrates a number of frames. A state machine is defined in VHDL in order to read, identify UBX frames and extract useful data.
- 4- Synchronize the obtained data with respect to the pulse per second (PPS) signal for a more reliable fusion solution. The PPS signal is considered the system's heartbeat: at each PPS signal, each received image frame is time-stamped with a combination of GNSS time and a delay time (between the PPS pulse and the exact acquisition time). This delay is calculated using an FPGA clock edge counter, since a 50 MHz is used as FPGA clock frequency. This process permits to differentiate between image data acquired on the same second and having the same GNSS geo-location information.
- 5- Once the synchronized and corresponding information are available, a real-time embedded algorithm is running that can provide horizon line, segmented areas between sky or non-sky, percentage of visible sky as a visibility indicator, and the detection of satellite states of reception. The navigation processing lifecycle has to be run before the new incoming PPS signal.
- 6- Employing a customizable embedded processor on the FPGA, different data packages are sent to corresponding external memories, to be used later for validation or additional algorithms development. The FPGA-based processor can be programmed, for further processing, using high-level languages such as C/C++.

### **Conclusions and Contributions**

Using FPGA-based system offer designers the maximum flexibility to customize system architecture. Co-designing software and hardware is also an option offered for parallel computation: designers have the possibility to implement the bottleneck segments of the algorithm as a custom coprocessor or as a hardware module to speed up the algorithm. This opportunity promotes the use of embedded processors in a more attractive and feasible approach than the traditional off-the-shelf (OTS) approach.

The proposed paper will then address the following topics: after the presentation of the applicative context and the objective of the tool developed, the paper will promote using co-designed architecture for implementing real-time multi-sensor navigation system. It will present how the proposed system is designed and developed for FPGA-based processors and show the effectiveness of multi-sensors data combination on the accuracy of train geo-location and path characterization. Applicative results will be presented in order to illustrate the potential of the tool as well as its planned use in the ERSAT GGC project.