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# A $-40$ to $250$ °C Triple Modular Redundancy Temperature Sensor for Turbofan Engines

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**Abstract**—Turbofan engines using distributed control architecture require sensors and electronic instrumentation located in the engine compartment to simplify system design, improve reliability, and ease signal multiplexing. Designing a wide range temperature sensor which works reliably regardless of process variation can be extremely challenging. Using a bandgap-like topology with PiN diodes as the sensing element, this work proposes a  $-40$  to  $250$  °C temperature sensor in the IMS  $0.35$   $\mu\text{m}$  SOI technology. To circumvent the process variation challenge, a triple modular redundancy is proposed for the sensing element combined with a weighted voter and digital circuitry calibration. The proposed sensing element supplies the analog-to-digital conversion (ADC) with a  $V_{REF}$  having a typical-mean temperature coefficient of  $62$   $\text{ppm}/^\circ\text{C}$ ,  $24$   $\text{ppm}/^\circ\text{C}$  for the best corner, and  $213$   $\text{ppm}/^\circ\text{C}$  for the worst corner. An average  $V_{CTAT}$  sensitivity is estimated at  $0.282$   $\text{mV}/^\circ\text{C}$  among all corners. After a 2-point temperature calibration, the ADC quantization step presented a negligible variation over temperature, approximately  $1.0$   $\text{mV}$  among all corners, assuring a  $0.28$  °C of temperature inaccuracy.

**Index Terms**—temperature sensor, reliability, triple modular redundancy, turbofan

## I. INTRODUCTION

Turbojet engines using distributed control architecture require sensors and electronic instrumentation located in the engine compartment to simplify system design, improve reliability, and ease signal multiplexing. Reaching as close as possible to the engine’s hot zone, such harsh environment can easily exceed  $150$  °C going up to  $300$  °C under some conditions. In this context, the design of temperature sensors becomes challenging. This problem has motivated Patterson *et al* to propose a relaxation oscillator topology able to convert temperature to frequency variations using a resistance temperature detector [1]. In addition, Patterson *et al* have developed such a temperature sensor using silicon-on-insulator technology [2] exploring its decreased leakage current combined with lower power consumption.

Integrated temperature sensors proposed in the literature [3] are based on a classic system topology illustrated in Fig. 1. These sensors have a common principle: convert a complementary to absolute temperature voltage ( $V_{CTAT}$ ) using a reference voltage ( $V_{REF}$ ). Such architecture is composed of: a sensing element, a start-up circuit responsible for the

operational amplifier biasing, and the operational amplifier with a low closed loop gain.

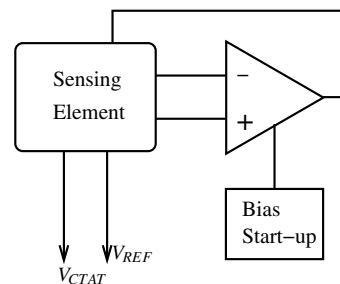


Fig. 1. A temperature sensor device based on  $V_{REF}$  and  $V_{CTAT}$  instrumentation.

K. Souri *et al* have proposed a  $-55$  to  $125$  °C temperature sensor using a PNP bipolar transistor as the sensing element [4]. A  $0.15$  °C resolution is achieved using a  $\Sigma\Delta$  ADC after digital calibration and circuit trimming. S. Jeong *et al* have proposed a  $0$  to  $100$  °C temperature sensor using MOSFETs as the sensing element [5]. A  $0.3$  °C resolution is obtained using a current-to-frequency converter combined with a frequency-to-digital converter after a 2-point calibration. Recently, H. Ardakani *et al* have proposed a  $30$  to  $50$  °C temperature sensor for biomedical applications with p- and n-type polysilicon resistors as sensing elements [6]. A  $0.8$  °C resolution is found using a 10-element distributed sensor network and a voltage-controlled-oscillator. X. Wang *et al* have proposed a  $0$  to  $100$  °C temperature sensor using MOSFETs as the sensing element [7]. A  $0.2$  °C resolution is obtained using a current-to-time converter combined with a time-to-digital converter after a 2-point calibration.

For turbofan temperature sensing, however, the principle of  $V_{CTAT}$  conversion using a  $V_{REF}$  as the ADC input reference is hindered by  $V_{CTAT}$  and  $V_{REF}$  reliability in harsh environments. By designing a sensing element, one may find that either  $V_{CTAT}$  or  $V_{REF}$  fails when temperature variations and process variability take place. A faulty element would have a highly non-linear  $V_{CTAT}$  or a non-flat  $V_{REF}$  varying over temperature. In this context, this paper proposes a temperature sensor using a triple modular redundancy (TMR) to address this issue

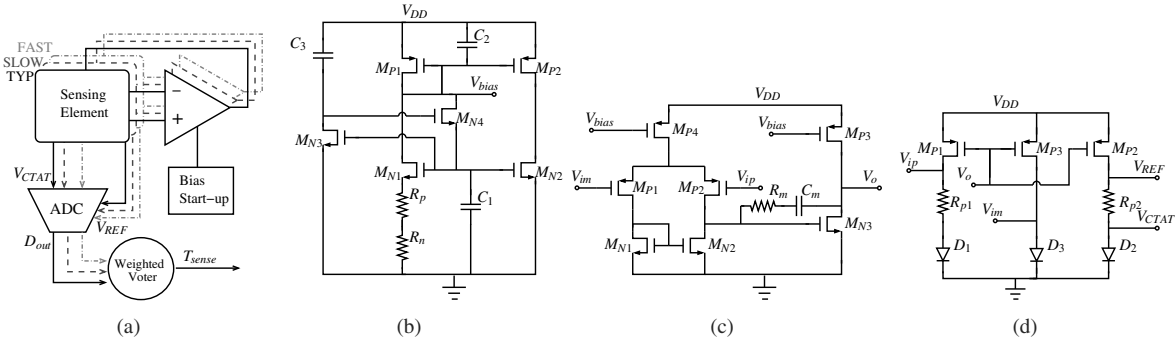


Fig. 2. Proposed TMR temperature sensor device using TYP, SLOW, and FAST sensing cores: (a) architecture illustration, (b) bias start-up schematics, (c) operational amplifier schematics, and (d) temperature sensing element schematics.

from - 40 to 250 °C temperature range for turbofan engine application. Using the 0.35  $\mu\text{m}$  thin film SOI technologies from Fraunhofer IMS, integrated circuits achieve a low leakage current suitable for high temperatures [8]. The proposed TMR temperature sensor is composed of the TYP, the FAST and the SLOW sensing elements using the PiN diode proposed in [9]. Moreover, a 3-step sensor calibration is proposed assuming two temperature points (i.e. 27 and 150 °C) where a fault-free  $V_{REF}$  is selected, a weighted voting is carried out in digitized  $V_{CTAT}$ , and a sensed temperature is estimated. Finally, post-layout simulation results are presented to assert TMR temperature sensor reliability using a corner-based analysis for 1021-points temperature variation from - 40 to 250 °C.

## II. PROPOSED TMR TEMPERATURE SENSOR

Recently, Fraunhofer IMS has developed a high temperature 0.35  $\mu\text{m}$  thin film SOI technology [8]. SOI technologies are known for their ability to operate at high temperature due to their intrinsic low leakage current. The HT 0.35  $\mu\text{m}$  SOI CMOS has 3.3/5.0 V supply voltages; p- and n-type transistors with a 9.4 nm gate-oxide in a 150 nm Si-film protected by a 400 nm buried-oxide (BOX); 4 tungsten-metal layers; and low-leakage PiN diodes.

Fig. 2(a) illustrates the proposed TMR temperature sensor composed of three sensing elements with feedback controlled by their own operational amplifier with a low closed-loop gain, and a master start-up biasing circuitry. Each sensing element has a  $V_{CTAT}$  and a  $V_{REF}$  outputs. Temperature acquisition is obtained by  $V_{CTAT}$  from low-leakage PiN diodes; a flat  $V_{REF}$  is required for  $V_{CTAT}$  ADC. Both voltages are then obtained from sensing elements having bandgap-like topology. Finally, a weighted voter is used to determine the estimated temperature among all three sensing elements.

### A. Bias Start-up

J. Pathrose *et al* have designed the bias and start-up circuit illustrated in Fig. 2(b) [3]. In Pathrose's work, they have suggested a Zero Temperature Coefficient (ZTC) biasing to minimize the temperature dependency of the operational amplifier. They have claimed that the ZTC technique cannot stabilize the amplifier gain. Rather, this work has chosen to design such

start-up biasing circuit considering the transconductance ZTC bias condition suggested by P. Toledo *et al* in [10]. One may choose to design  $M_{P1,2}$  transistors in the ZTC vicinity and use the thermal drift of polysilicon resistors  $R_{p,n}$  to compensate for the amplifier gain variations. This idea has first been used in a Gm-C filter design in [11]. The optimal sizing is presented in Tab. I.

### B. Operational Amplifier

A Miller-compensated operational amplifier, illustrated in Fig. 2(c), is designed to achieve a stable operation having a low closed-loop gain (from 1 to 4). Thus, the open-loop gain should be at least 60 dB over all corners and temperatures. One may find the analytical expression of the open-loop gain as

$$G = g_{mP1,2} \cdot g_{mN3} \cdot (r_{DSp2} || r_{DSn2}) \cdot (r_{DSp3} || r_{DSn3}). \quad (1)$$

To guarantee a  $gm$  ZTC [11], current mirrors  $M_{P3,4}$  are designed in ZTC vicinity. However, such technique limits the open-loop gain which is increased in this proposal by increasing the length of  $M_{P3}$ . Thus, output impedance is increased by a longer  $M_{P3}$  ( $L = 1.08 \mu\text{m}$ ) which improves the open-loop gain without disturbing temperature compensation.

Temperature acquisition should be done in a millisecond range. Thus, unity-gain frequency is specified greater than 1 MHz with a small drift over temperature variations. Miller-compensation is obtained by taking into consideration post-layout parasitics in  $R_m$  and  $C_m$  values for a phase margin better than 60 ° at unity-gain frequency. Literature presents that operational amplifier offset is a major drawback of such sensor architecture causing error and temperature drift [12]. Unfortunately, statistical data of HT 0.35  $\mu\text{m}$  SOI CMOS is not available, which hinders the required Monte Carlo simulations for offset estimation. For simplicity, it is assumed that offset errors are corrected using a digital calibration in the implemented ADC. The optimal sizing is presented in Tab. I.

### C. Sensing Element

A diode-based sensing element, illustrated in Fig 2(d), is known as a good thermal sensor for a wide temperature range. Adopting a bandgap-like topology [3], the sensing element

# AUTHOR VERSION

TABLE I

CIRCUIT SIZING: TRANSISTOR WIDTHS IN  $\mu\text{M}$  FOR ALL  $L = 0.35 \mu\text{M}$ , CAPACITANCE IN FF, AND RESISTANCE IN  $k\Omega$ .

Bias start-up			Op. Amp ( $M_{P3} L = 1.08 \mu\text{m}$ )				
$M_{P1}$	1.2	$M_{P2}$	1.2	$M_{P1,2}$	1.2	$M_{P3,4}$	1.2
$M_{N1,2}$	1.2	$M_{N3,4}$	1.2	$M_{N1,2}$	1.2	$M_{N3}$	1.2
$R_p$	1.94	$R_n$	0.35	$R_m$	12	$C_m$	389

provides the  $V_{CTAT}$  while supplying the ADC reference input with the  $V_{REF}$ . Temperature instrumentation is then carried out using the principle of diode voltage difference between  $D_1$  and  $D_3$ . This principle was previously presented in [13]. Souza *et al.* have highlighted an increasing thermal sensitivity when the diode current density is high. Here, a  $I_{D_3} \approx 1 \mu\text{A}/\mu\text{m}$  is chosen. To increase the sensing element's linearity, the diode voltage difference is then converted back to a diode current flowing through  $D_2$  using a feedback loop imposed with the operational amplifier (Fig. 2(c)). To achieve a reasonable footprint, it was decided to set the diode current ratio (i.e.  $I_{D_3}/I_{D_1}$ ) from one to ten. Thus, a compromise in the trade-off between sensing element sensitivity and diode area is established.

Aiming for low-leakage currents under high temperature operation, the proposed temperature sensor uses a PiN diode proposed in [9]. Such PiN diode achieves a leakage current ( $I_{GEN}$ ) of 10 fA over temperature and voltage bias; it has a multiplication factor ( $M$ ) close to the unity. To explore such characteristics, a unitary PiN diode having  $2.4 \times 3.0 \mu\text{m}^2$  area is used; diode area is increased using  $D_i$  devices in parallel. From these PiN characteristics, one may obtain

$$V_{CTAT} = M V_T \ln\left(\frac{I_{D_{P2}}}{I_{GEN}}\right), \quad (2)$$

where  $V_T = kT/q$  is the thermal voltage. Analytical calculations for the bandgap-like topology are carried out using [12], which yields:

$$V_{REF} = V_{CTAT} - \frac{R_{P2}}{R_{P1}} V_T \ln\left(\frac{D_3}{D_1}\right). \quad (3)$$

To minimize  $V_{REF}$  temperature coefficient (TC), that is

$$\text{TC}_{V_{REF}} = \frac{\partial V_{REF}}{\partial T} \rightarrow 0; \quad (4)$$

one may derive the required bias current as

$$I_{D_{P2}} = I_{GEN} \left(\frac{D_3}{D_1}\right)^{\frac{R_{P2}}{M R_{P1}}}. \quad (5)$$

Assuming that  $R_{P2}$  and  $R_{P1}$  have the same temperature variation,  $R_{P2}/R_{P1}$  TC is negligible. Since the bias start-up circuitry is designed using current mirrors in the ZTC vicinity,  $I_{D_{P2}}$  temperature variations are only determined by PiN diode physics. However,  $I_{D_{P2}}$  changes with process variability. For this reason,  $V_{REF}$  fails when (5) is not met due to combined temperature variation and process variability.

To avoid a non-flat  $V_{REF}$ , this proposal chose to determine the best  $D_3/D_1$  and  $R_{P2}/R_{P1}$  ratios available to minimize

$\text{TC}_{V_{REF}}$ . HT 0.35  $\mu\text{m}$  SOI CMOS technology has three main corners to be considered: typical-mean (TM), worst-case power (WP), worst-case speed (WS). A typical (TYP) sensing element is designed to achieve (5) condition under TM corner. In WP corner, transistor mobility is increased and worsens for high temperatures. A FAST sensing element is designed to assure (5) condition under WP corner. Conversely, a SLOW sensing element is designed to assure (5) condition under WS corner, when transistor mobility is drastically reduced – mainly for low temperatures. The final design sizing is presented in Tab. II.

TABLE II

TEMPERATURE SENSOR CIRCUIT SIZING: TRANSISTOR WIDTHS IN  $\mu\text{M}$  FOR ALL  $L = 0.35 \mu\text{M}$ , NUMBER OF DIODE UNITIES HAVING AN AREA OF  $2.4 \times 3.0 \mu\text{m}^2$ , AND RESISTANCE IN  $k\Omega$

		TYP			FAST			SLOW		
$M_{P1}$	1.2	4.8	2.4	$M_{P2}$	8.4	4.8	7.2	$M_{P3}$	1.2	1.2 1.2
$D_1$	1	4	2	$D_2$	7	4	6	$D_3$	1	1 1
$R_{P1}$	1	8	7	$R_{P2}$	7	48	105			

## D. Digital Circuitry

A 3-step sensor calibration is proposed assuming two temperature points  $T(i)$  and  $T(j)$  (i.e. 27 and 150  $^\circ\text{C}$ ). The first step consists in choosing of the best  $V_{REF}$ . Among all three sensing elements, the smallest  $V_{REF}$  variation between  $T(i)$  and  $T(j)$  is determined. Then, the chosen sensing element supplies the ADC reference input. It is expected that TYP provides the best  $V_{REF}$  in TM corner, FAST in WP corner, and SLOW in WS corner; when (5) is met.

Instrumented  $V_{CTAT}$  is analog-to-digital converted using a quantization step defined as  $q = V_{REF}/2^N$ , where  $N$  is the number of bits. According to the thermal sensitivity of PiN diodes reported in [13], a 10-bit calibrated ADC is system-level implemented using MatLab to achieve a resolution of about 0.28  $^\circ\text{C}$ . To reduce hardware costs, each sensing element is digitized using the same ADC in a sequential time skew. In the second calibration step,  $D_{out}$  values are processed, correcting analog imperfections due to process variability (e.g. operational amplifier offset). To this end, a weighted voter combines TYP, FAST, and SLOW  $D_{out}$  data in a unique temperature estimation. This strategy enables the digital circuitry to detect sensing elements failure in a specific corner when (5) is not met. The weighted  $D_{out}$  is obtained in this work using an equally weighted voter (i.e. for each sensing element, weights are equals to one).

In the final step, the weighted  $D_{out}$  is converted then into a readable temperature considering the two temperature points  $T(i)$  and  $T(j)$  to reveal the estimated temperature ( $T_{sense}$ ) as

$$T_{sense} = T(i) + (D_{out} - D_{out}(i)) \cdot \frac{T(j) - T(i)}{D_{out}(j) - D_{out}(i)}. \quad (6)$$

Afterward, the residual error is a nonlinear one. Such nonlinear error is here evaluated using a RMSE figure-of-merit defined as

$$\text{RMSE} = \sqrt{\frac{1}{M} \sum_{k=1}^M (T_{sense}(k) - T(k))^2}, \quad (7)$$

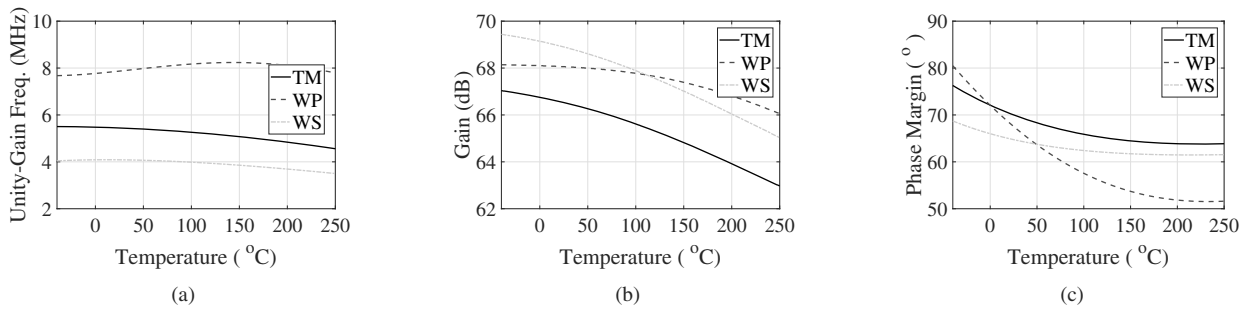


Fig. 4. Operational Amplifier post-layout simulations:(a) unity-gain frequency, (b) low-frequency gain, and (c) phase margin.

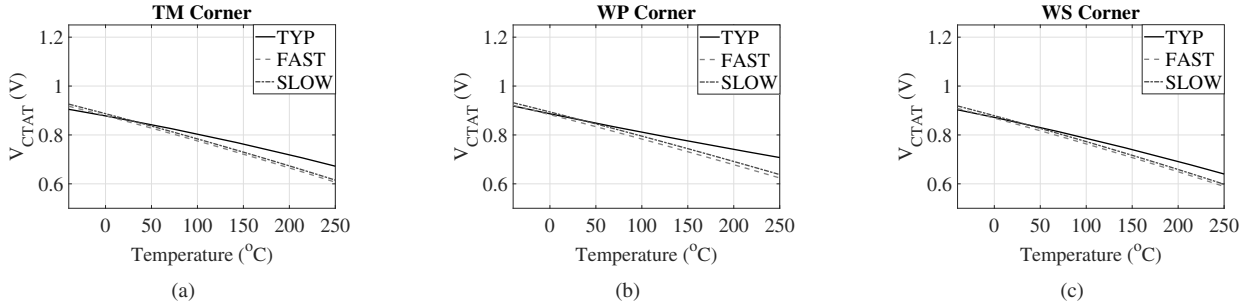


Fig. 5. Post-layout simulated  $V_{CTAT}$  for each TYP, FAST, and SLOW sensing elements in (a) TM, (b) WP, and (c) WS corners.

where  $M$  is the number of temperature points (i.e.  $M = 1021$  as presented in Sec. III).

### III. POST-LAYOUT SIMULATION RESULTS

The temperature sensor using TMR architecture is designed using HT 0.35  $\mu\text{m}$  SOI CMOS technology. Fig. 3 presents TMR temperature sensor's layout having an area of  $92 \times 136 \mu\text{m}^2$ . The digital circuitry is not presented. Post-layout simulations are carried out for 1021-points of temperature variation from  $-40$  to  $250$   $^{\circ}\text{C}$  for TM, WS, and WP corners. The proposed temperature sensor achieves a worst-case power consumption at  $250$   $^{\circ}\text{C}$  of  $506 \mu\text{W}$  for TM,  $308 \mu\text{W}$  for WS, and  $806 \mu\text{W}$  for WP corner. Results are then post-processed in MatLab using the ADC and weighted voter system-level implementation.

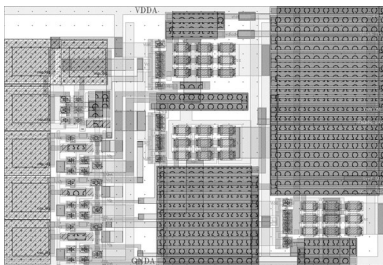


Fig. 3. TMR's Temperature Sensor having a layout area of  $92 \times 136 \mu\text{m}^2$ .

The operational amplifier is first characterized in terms of unity-gain frequency, low frequency gain, and phase margins. Post-layout results are shown in Fig. 4 using *stb* simulation in

Virtuoso Spectre for all corners and temperature range. Unity-gain frequency, illustrated in Fig. 4(a), has a flat response over temperature for each simulated corner. However, process variability does change the average unity-gain frequency. Despite this variation, frequency performance is guaranteed greater than 1 MHz. Variations found include  $3.2 \text{ kHz}/^{\circ}\text{C}$  for TM,  $1.9 \text{ kHz}/^{\circ}\text{C}$  for WP, and  $2.0 \text{ kHz}/^{\circ}\text{C}$  for WS corners. Figure 4(b) illustrates the low-frequency gain over temperature for each simulated corner. Despite the presented variations, low-frequency gain is always greater than the required 60 dB, thus assuring the correct operation of the feedback loop. Variations found include  $14 \text{ mdB}/^{\circ}\text{C}$  for TM,  $7 \text{ mdB}/^{\circ}\text{C}$  for WP, and  $15 \text{ mdB}/^{\circ}\text{C}$  for WS corners. Operational amplifier stability is studied from the phase margin metric. Figure 4(c) highlights WP corner having a phase margin lower than  $60^{\circ}$  in high temperature. Nevertheless, phase margin remains greater than the required  $45^{\circ}$  for amplifier stability. Variations found include  $2^{\circ}/^{\circ}\text{C}$  for TM,  $6^{\circ}/^{\circ}\text{C}$  for WP,  $1^{\circ}/^{\circ}\text{C}$  for WS corners.

All three sensing elements are post-layout simulated using a *tran* simulation in Virtuoso Spectre for all corners and temperatures. Fig. 5 presents the  $V_{CTAT}$  for each TYP, FAST, and SLOW sensing element, being TM corner shown in Fig. 5(a), WP corner in Fig. 5(b), and WS corner in Fig. 5(c). For the TM corner, sensitivity is estimated at  $0.232 \text{ mV}/^{\circ}\text{C}$  for TYP,  $0.309 \text{ mV}/^{\circ}\text{C}$  for FAST, and  $0.307 \text{ mV}/^{\circ}\text{C}$  for SLOW. For the WP corner, sensitivity is estimated at  $0.209 \text{ mV}/^{\circ}\text{C}$  for TYP,  $0.296 \text{ mV}/^{\circ}\text{C}$  for FAST, and  $0.290 \text{ mV}/^{\circ}\text{C}$  for SLOW. For the WS corner, sensitivity is estimated at  $0.262 \text{ mV}/^{\circ}\text{C}$  for TYP,  $0.316 \text{ mV}/^{\circ}\text{C}$  for FAST, and  $0.317 \text{ mV}/^{\circ}\text{C}$  for SLOW.

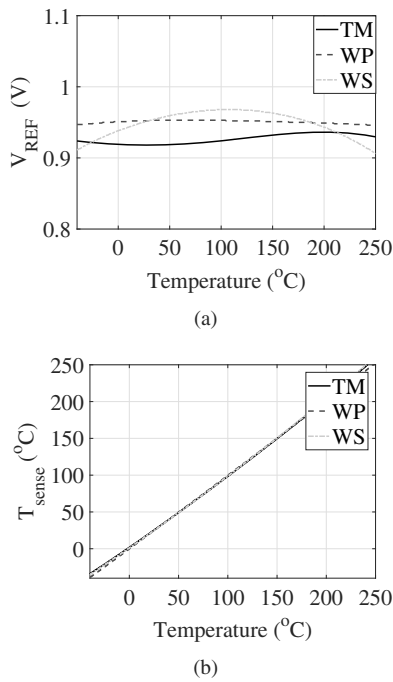


Fig. 6. Post-layout simulations after a 2-point temperature calibration at 27 and 150  $^{\circ}$ C for corner: (a) selected  $V_{REF}$  for the ADC reference, (b) calibrated  $T_{sense}$  after weighted voting.

Obtained sensing element sensitivity is as expected in [13] ensuring an average sensor resolution of about 0.28  $^{\circ}$ C after calibration.

After an analog 2-point temperature calibration in 27 and 150  $^{\circ}$ C, the best reference voltage among the three available ones is selected to supply the ADC reference. Fig. 6(a) presents the resultant  $V_{REF}$  from post-layout simulated sensing elements using a *tran* simulation in Virtuoso Spectre for all corners and temperatures. Reference accuracy is calculated at 62 ppm/ $^{\circ}$ C for TM corner, at 24 ppm/ $^{\circ}$ C for WP corner, and at 213 ppm/ $^{\circ}$ C for WS corner. A lower accuracy is found in WS corner due to  $R_{p1,2}$  temperature variation under process variability in the vicinity of 100  $^{\circ}$ C. Under such conditions, (5) is not met. Even though  $V_{REF}$  has no-flat characteristics, ADC quantization step presented a negligible variation over temperature. The estimated LSB is 0.9 mV for TM, 1.1 mV for WP, and 1.3 mV for WS corners.

Once the best  $V_{REF}$  is selected, the ADC output codes are analyzed. Three digital outputs ( $D_{out}$ ) from TYP, FAST, and SLOW are weight-voted to get a unique characteristic of  $T_{sense}$  for each corner. The offset and the gain errors are corrected; the calibrated  $T_{sense}$  is illustrated in Fig. 6(b) for each corner. The nonlinear RMSE is estimated as 3.2  $^{\circ}$ C for TM, 0.8  $^{\circ}$ C for WP, and 3.6  $^{\circ}$ C for WS corners.

Table III reveals that Souri's work has an exceptional low error and good resolution in spent of complex circuit trimming and digital calibration. An interesting compromise is found in Wang's and Jeong's work between power consumption and resolution, however the temperature range is limited. This

work presents a good compromise in error and resolution performance in spent of power consumption, while achieving a wide temperature range up to 250 $^{\circ}$ C. This is first demonstrated in the literature.

## IV. CONCLUSIONS

A temperature sensor is proposed for turbofan applications. Reliability issues in the sensing principle of  $V_{CTAT}$  conversion using a  $V_{REF}$  as the ADC input reference, are circumvented by a design of three fault-prone elements, that is a TMR. By the digital circuitry and the weighted voter, a highly non-linear  $V_{CTAT}$  and a non-flat  $V_{REF}$  varying over temperature have been calibrated. The proposal highlighted a sensing element having a  $V_{REF}$  temperature coefficient of 62 ppm/ $^{\circ}$ C for TM, of 24 ppm/ $^{\circ}$ C for WP, and of 213 ppm/ $^{\circ}$ C for WS corners. After a 2-point temperature calibration, the ADC quantization step presented a negligible variation over temperature, and an average LSB equals to 1.0 mV. An average  $V_{CTAT}$  sensitivity is estimated at 0.282 mV/ $^{\circ}$ C which ensure a temperature resolution of about 0.28  $^{\circ}$ C.

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