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Transmission des canaux de contrôles pour le HSDPA

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Transmission des canaux de contrôle pour le HSDPA

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Abbreviations

For the purposes of the present document, the following abbreviations apply:

16QAM	16 Quadrature Amplitude Modulation
AICH	Acquisition Indicator Channel
CPICH	Common Pilot Channel
CQI	Channel Quality Indicator
DPCCH	Dedicated Physical Control Channel
DPCH	Dedicated Physical Channel
HARQ	Hybrid-ARQ
HARQ-ACK	Hybrid-ARQ Acknowledgement
HS-DPCCH	Dedicated Physical Control Channel (uplink) for HS-DSCH
HS-DSCH	High Speed Downlink Shared Channel
HS-PDSCH	High Speed Physical Downlink Shared Channel
HS-SCCH	Shared Control Channel for HS-DSCH
P-CCPCH	Primary Common Control Physical Channel
PDSCH	Physical Downlink Shared Channel
PICH	Page Indicator Channel
PRACH	Physical Random Access Channel
S-CCPCH	Secondary Common Control Physical Channel
SCH	Synchronisation Channel
SF	Spreading Factor
SFN	System Frame Number
UE	User Equipment
UTRAN	UMTS Terrestrial Radio Access Network

1 HS-Physical Channels

1.1 Uplink Dedicated Control Channel associated with HS-DSCH transmission (uplink HS-DPCCH).

Figure 1 illustrates the frame structure of the HS-DPCCH. The HS-DPCCH carries uplink feedback signalling related to downlink HS-DSCH transmission. The HS-DSCH-related feedback signalling consists of Hybrid-ARQ Acknowledgement (HARQ-ACK) and Channel-Quality Indication (CQI) [TS 25.214]. Each sub frame of length 2 ms (3*2560 chips) consists of 3 slots, each of length 2560 chips. The HARQ-ACK is carried in the first slot of the HS-DPCCH sub-frame. The CQI is carried in the second and third slot of a HS-DPCCH sub-frame. There is at most one HS-DPCCH on each radio link. The HS-DPCCH can only exist together with an uplink DPCCCH. The timing of the HS-DPCCH relative to the uplink DPCCCH is shown in section 1.4.

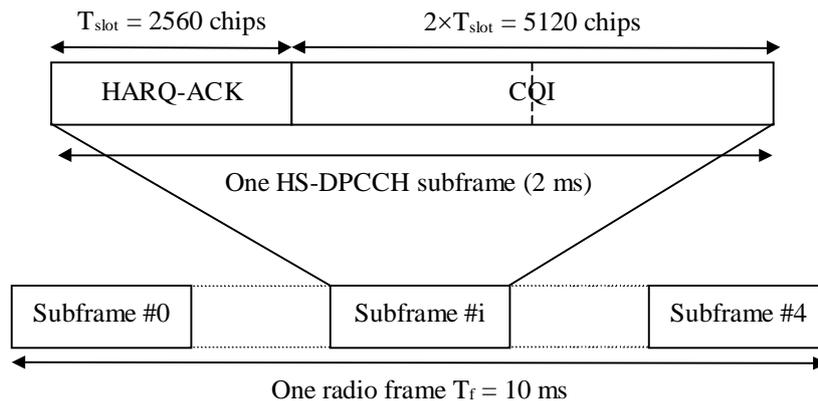


Figure 1: Frame structure for uplink HS-DPCCH

The spreading factor of the HS-DPCCH is 256 i.e. there are 10 bits per uplink HS-DPCCH slot. The slot format for uplink HS-DPCCH is defined in Table 1.

Table 1: HS-DPCCH fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Subframe	Bits/ Slot	Transmitted slots per Subframe
0	15	15	256	30	10	3

1.2 Downlink Shared Control Channel (HS-SCCH)

The HS-SCCH is a fixed rate (60 kbps, SF=128) downlink physical channel used to carry downlink signalling related to HS-DSCH transmission. Figure 2 illustrates the sub-frame structure of the HS-SCCH.

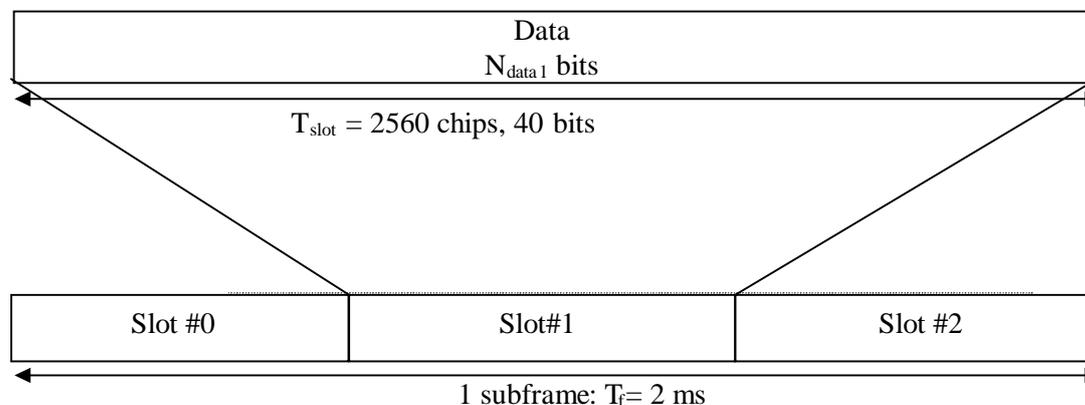


Figure 2: Subframe structure for the HS-SCCH

1.3 High Speed Physical Downlink Shared Channel (HS-PDSCH)

The High Speed Physical Downlink Shared Channel (HS- PDSCH) is used to carry the High Speed Downlink Shared Channel (HS-DSCH).

A HS-PDSCH corresponds to one channelization code of fixed spreading factor SF=16 from the set of channelization codes reserved for HS-DSCH transmission. Multi-code transmission is allowed, which translates to UE being assigned multiple channelisation codes in the same HS-PDSCH subframe, depending on its UE capability.

The subframe and slot structure of HS-PDSCH are shown in figure 3.

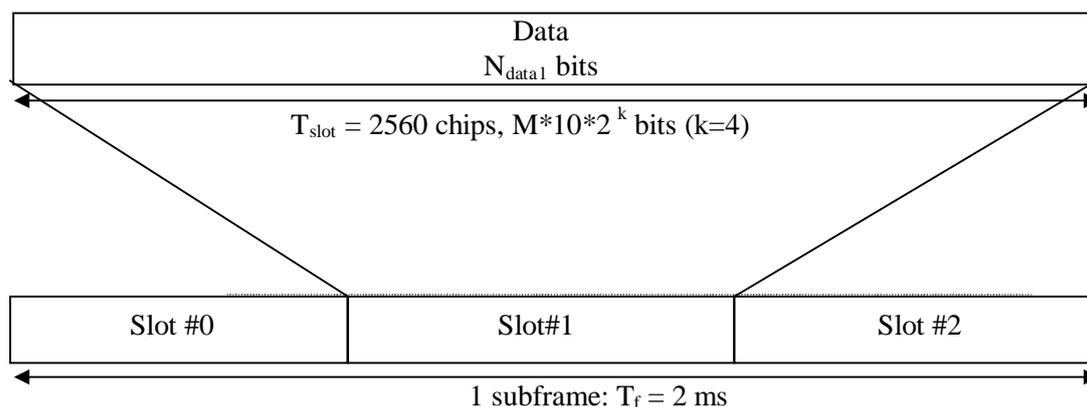


Figure 3: Subframe structure for the HS-PDSCH

An HS-PDSCH may use QPSK or 16QAM modulation symbols. In figure 3, M is the number of bits per modulation symbols i.e. $M=2$ for QPSK and $M=4$ for 16QAM. The slot formats are shown in table 2.

Table 2: HS-DSCH fields

Slot format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ HS-DSCH subframe	Bits/ Slot	Ndata
0(QPSK)	480	240	16	960	320	320
1(16QAM)	960	240	16	1920	640	640

All relevant Layer 1 information is transmitted in the associated HS-SCCH i.e. the HS-PDSCH does not carry any Layer 1 information.

1.4 Timing relationship between physical channels

1.4.1 General

The P-CCPCH, on which the cell SFN is transmitted, is used as timing reference for all the physical channels, directly for downlink and indirectly for uplink.

Figure 4 below describes the frame timing of the downlink physical channels. For the AICH the access slot timing is included. Transmission timing for uplink physical channels is given by the received timing of downlink physical channels, as described in the following subclauses.

The following applies:

- SCH (primary and secondary), CPICH (primary and secondary), P-CCPCH, and PDSCH have identical frame timings.
- The S-CCPCH timing may be different for different S-CCPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{S-CCPCH,k} = T_k \times 256$ chip, $T_k \in \{0, 1, \dots, 149\}$.
- The PICH timing is $\tau_{PICH} = 7680$ chips prior to its corresponding S-CCPCH frame timing, i.e. the timing of the S-CCPCH carrying the PCH transport channel with the corresponding paging information, see also subclause 7.2.
- AICH access slots #0 starts the same time as P-CCPCH frames with $(SFN \text{ modulo } 2) = 0$. The AICH/PRACH and AICH/PCPCH timing is described in subclauses 7.3 and 7.4 respectively.
- The relative timing of associated PDSCH and DPCH is described in subclause 7.5.

- The DPCH timing may be different for different DPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{\text{DPCH},n} = T_n \times 256 \text{ chip}$, $T_n \in \{0, 1, \dots, 149\}$. The DPCH (DPCCH/DPDCH) timing relation with uplink DPCCH/DPDCHs is described in subclause 7.6.
- The start of HS-SCCH subframe #0 is aligned with the start of the P-CCPCH frames. The relative timing between a HS-PDSCH and the corresponding HS-SCCH is described in subclause 1.4.3.

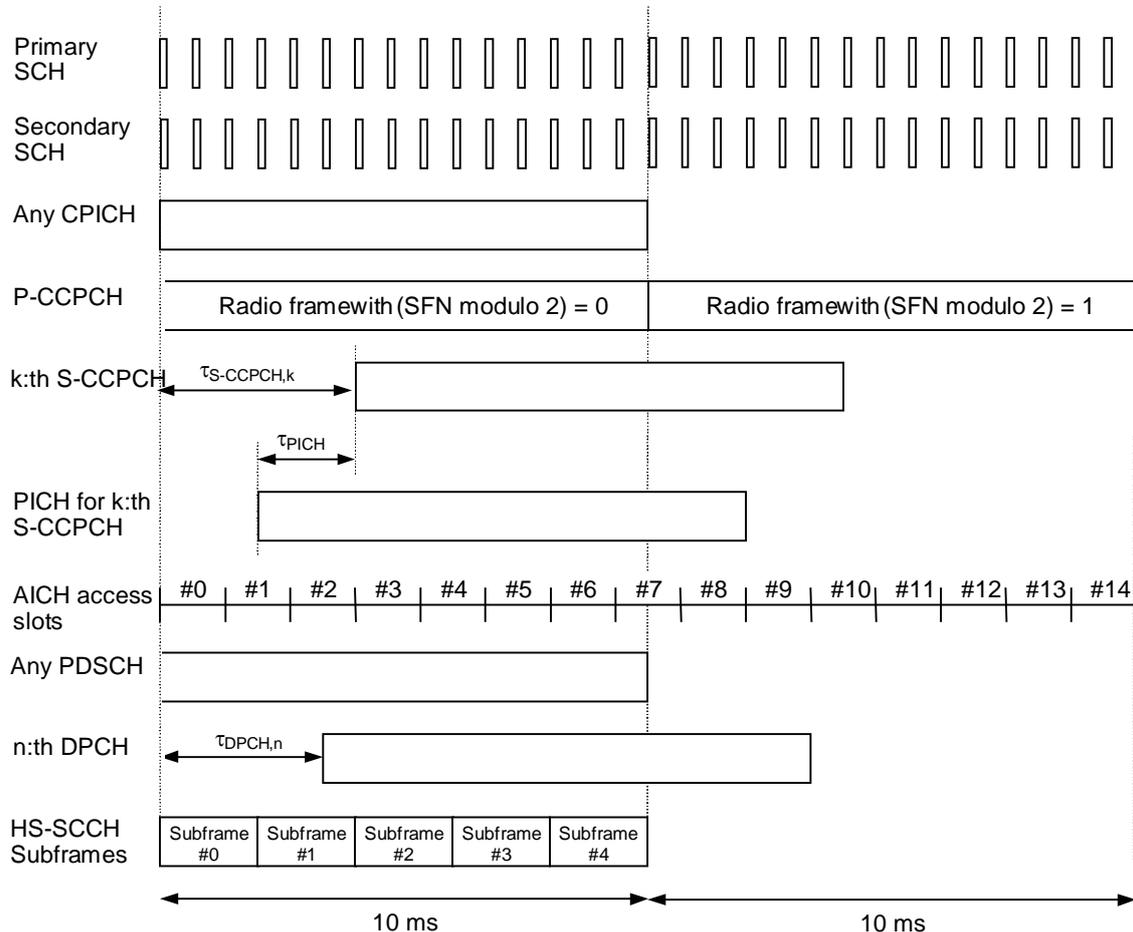


Figure 4: Radio frame timing and access slot timing of downlink physical channels

1.4.2 Uplink DPCCH/HS-DPCCH/HS-PDSCH timing at the UE

Figure 5 shows the timing offset between the uplink DPCH, the HS-PDSCH and the HS-DPCCH at the UE. An HS-DPCCH sub-frame starts $m \times 256$ chips after the start of an uplink DPCH frame that corresponds to the DL DPCH frame from the HS-DSCH serving cell containing the beginning of the related HS-PDSCH subframe with m calculated as

$$m = (\tau_{\text{TX_diff}} / 256) + 101$$

where $\tau_{\text{TX_diff}}$ is the difference in chips ($\tau_{\text{TX_diff}} = 0, 256, \dots, 38144$), between

- the transmit timing of the start of the related HS-PDSCH subframe (see sub-clauses 1.4.3 and 1.4.1)

and

- the transmit timing of the start of the downlink DPCH frame from the HS-DSCH serving cell that contains the beginning of the HS-PDSCH subframe (see sub-clause 1.4.1).

At any one time, m therefore takes one of a set of five possible values according to the transmission timing of HS-DSCH sub-frame timings relative to the DPCH frame boundary. The UE and Node B shall only update the set of values of m in connection to UTRAN reconfiguration of downlink timing.

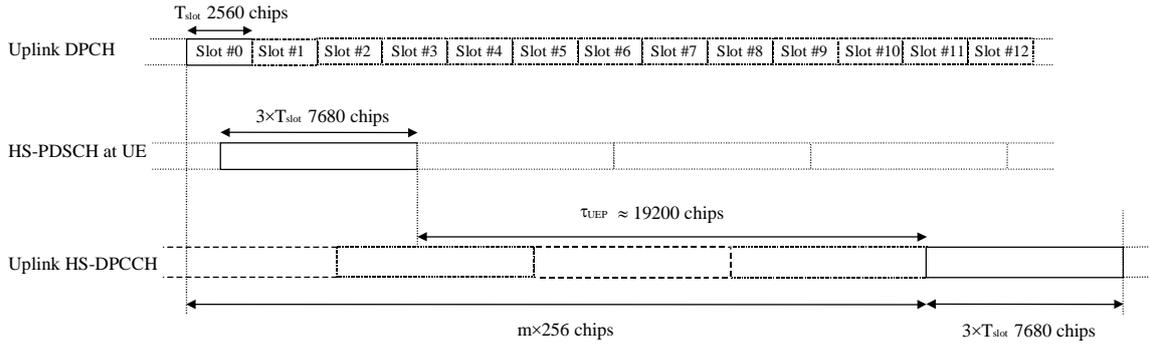


Figure 5: Timing structure at the UE for HS-DPCCH control signalling

1.4.3 HS-SCCH/HS-PDSCH timing

Figure 6 shows the relative timing between the HS-SCCH and the associated HS-PDSCH for one HS-DSCH sub-frame. The HS-PDSCH starts $\tau_{\text{HS-PDSCH}} = 2 \times T_{\text{slot}} = 5120$ chips after the start of the HS-SCCH.

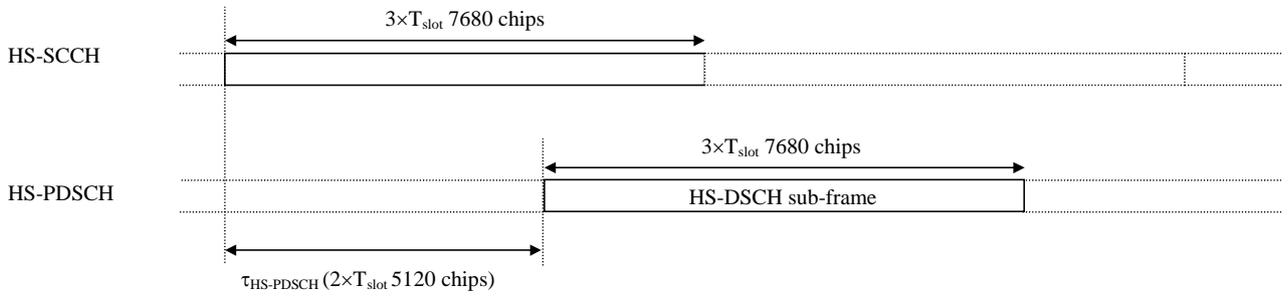


Figure 6: Timing relation between the HS-SCCH and the associated HS-PDSCH.

2 Coding for HS-SCCH

The following information is transmitted by means of the HS-SCCH physical channel.

- Channelization-code-set information (7 bits): $x_{\text{ccs},1}, x_{\text{ccs},2}, \dots, x_{\text{ccs},7}$
- Modulation scheme information (1 bit): $x_{\text{ms},1}$
- Transport-block size information (6 bits): $x_{\text{tbs},1}, x_{\text{tbs},2}, \dots, x_{\text{tbs},6}$
- Hybrid-ARQ process information (3 bits): $x_{\text{hap},1}, x_{\text{hap},2}, x_{\text{hap},3}$
- Redundancy and constellation version (3 bits): $x_{\text{rv},1}, x_{\text{rv},2}, x_{\text{rv},3}$
- New data indicator (1 bit): $x_{\text{nd},1}$
- UE identity (16 bits): $x_{\text{ue},1}, x_{\text{ue},2}, \dots, x_{\text{ue},16}$

2.1 Overview

Figure 7 below illustrates the overall coding chain for HS-SCCH.

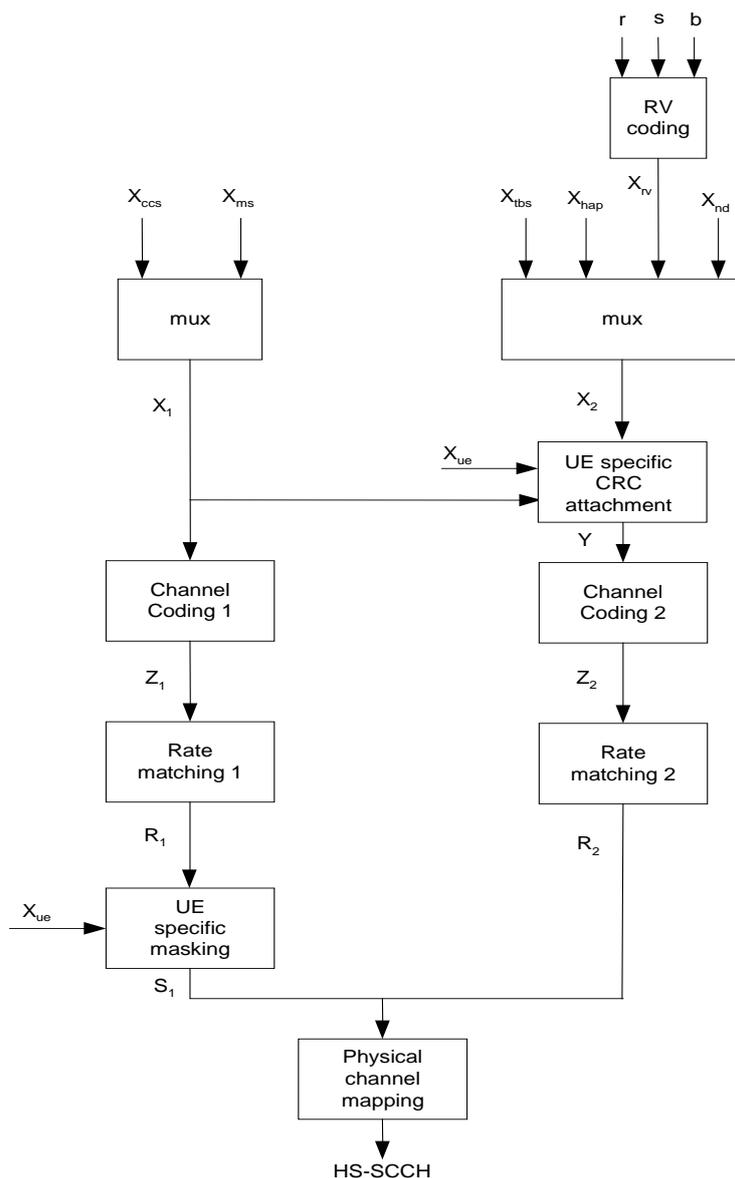


Figure 7: Coding chain for HS-SCCH

2.2 HS-SCCH information field mapping

2.2.1 Redundancy and constellation version coding

The redundancy version (RV) parameters r , s and constellation version parameter b are coded jointly to produce the value X_{rv} . X_{rv} is alternatively represented as the sequence $x_{rv,1}$, $x_{rv,2}$, $x_{rv,3}$ where $x_{rv,1}$ is the MSB. This is done according to the following tables according to the modulation mode used:

Table 3: RV coding for 16 QAM

X_{rv} (value)	s	r	b
0	1	0	0
1	0	0	0
2	1	1	1
3	0	1	1
4	1	0	1
5	1	0	2
6	1	0	3
7	1	1	0

Table 4: RV coding for QPSK

X_{rv} (value)	s	r
0	1	0
1	0	0
2	1	1
3	0	1
4	1	2
5	0	2
6	1	3
7	0	3

2.3 Multiplexing of HS-SCCH information

The channelization-code-set information $x_{ccs,1}, x_{ccs,2}, \dots, x_{ccs,7}$ and modulation-scheme information $x_{ms,1}$ are multiplexed together. This gives a sequence of bits $x_{1,1}, x_{1,2}, \dots, x_{1,8}$ where

$$x_{1,i} = x_{ccs,i} \quad i=1,2,\dots,7$$

$$x_{1,i} = x_{ms,i-7} \quad i=8$$

The transport-block-size information $x_{tbs,1}, x_{tbs,2}, \dots, x_{tbs,6}$, Hybrid-ARQ-process information $x_{hap,1}, x_{hap,2}, x_{hap,3}$, redundancy-version information $x_{rv,1}, x_{rv,2}, x_{rv,3}$ and new-data indicator $x_{nd,1}$ are multiplexed together. This gives a sequence of bits $x_{2,1}, x_{2,2}, \dots, x_{2,13}$ where

$$x_{2,i} = x_{tbs,i} \quad i=1,2,\dots,6$$

$$x_{2,i} = x_{hap,i-6} \quad i=7,8,9$$

$$x_{2,i} = x_{rv,i-9} \quad i=10,11,12$$

$$x_{2,i} = x_{nd,i-12} \quad i=13$$

2.4 CRC attachment for HS-SCCH

From the sequence of bits $x_{1,1}, x_{1,2}, \dots, x_{1,8}, x_{2,1}, x_{2,2}, \dots, x_{2,13}$ a 16 bits CRC is calculated according to Section 4.2.1.1 [TS 25.212]. This gives a sequence of bits c_1, c_2, \dots, c_{16} . This sequence of bits is then masked with the UE Identity $x_{ue,1}, x_{ue,2}, \dots, x_{ue,16}$ and then appended to the sequence of bits $x_{2,1}, x_{2,2}, \dots, x_{2,13}$ to form the sequence of bits y_1, y_2, \dots, y_{29} , where

$$y_i = x_{2,i} \quad i=1,2,\dots,13$$

$$y_i = (c_{i-13} + x_{ue,i-13}) \bmod 2 \quad i=14,15,\dots,29$$

2.5 Channel coding for HS-SCCH

Rate 1/3 convolutional coding, as described in Section 4.2.3.1 [TS 25.212], is applied to the sequence of bits $x_{1,1}, x_{1,2}, \dots, x_{1,8}$. This gives a sequence of bits $z_{1,1}, z_{1,2}, \dots, z_{1,48}$.

Rate 1/3 convolutional coding, as described in Section 4.2.3.1 [TS 25.212], is applied to the sequence of bits y_1, y_2, \dots, y_{29} . This gives a sequence of bits $z_{2,1}, z_{2,2}, \dots, z_{2,111}$.

Note that the coded sequence lengths result from the termination of K=9 convolutional coding being fully applied.

2.6 Rate matching for HS-SCCH

From the input sequence $z_{1,1}, z_{1,2}, \dots, z_{1,48}$ the bits $z_{1,1}, z_{1,2}, z_{1,4}, z_{1,8}, z_{1,42}, z_{1,45}, z_{1,47}, z_{1,48}$ are punctured to obtain the output sequence $r_{1,1}, r_{1,2}, \dots, r_{1,40}$.

From the input sequence $z_{2,1}, z_{2,2}, \dots, z_{2,111}$ the bits $z_{2,1}, z_{2,2}, z_{2,3}, z_{2,4}, z_{2,5}, z_{2,6}, z_{2,7}, z_{2,8}, z_{2,12}, z_{2,14}, z_{2,15}, z_{2,24}, z_{2,42}, z_{2,48}, z_{2,54}, z_{2,57}, z_{2,60}, z_{2,66}, z_{2,69}, z_{2,96}, z_{2,99}, z_{2,101}, z_{2,102}, z_{2,104}, z_{2,105}, z_{2,106}, z_{2,107}, z_{2,108}, z_{2,109}, z_{2,110}, z_{2,111}$ are punctured to obtain the output sequence $r_{2,1}, r_{2,2}, \dots, r_{2,80}$.

2.7 UE specific masking for HS-SCCH

The rate matched bits $r_{1,1}, r_{1,2}, \dots, r_{1,40}$ shall be masked in an UE specific way using the UE identity $x_{ue,1}, x_{ue,2}, \dots, x_{ue,16}$, to produce the bits $s_{1,1}, s_{1,2}, \dots, s_{1,40}$.

Intermediate code word bits $b_i, i=1,2,\dots,48$, are defined by encoding the UE identity bits using the rate $\frac{1}{2}$ convolutional coding described in Section 4.2.3.1 [TS 25.212]. Eight bits out of the resulting 48 convolutionally encoded bits are punctured using the rate matching rule of Section 4.2.7.5 for the HS-SCCH part 1 sequence, that is, the intermediate code word bits $b_1, b_2, b_4, b_8, b_{42}, b_{45}, b_{47}, b_{48}$, are punctured to obtain the 40 bit UE specific scrambling sequence c_1, c_2, \dots, c_{40} .

The mask output bits $s_{1,1}, s_{1,2}, \dots, s_{1,40}$ are calculated as follows:

$$s_{1,k} = (r_{1,k} + c_k) \bmod 2 \quad \text{for } k = 1, 2, \dots, 40$$

2.8 Physical channel mapping for HS-SCCH

The HS-SCCH sub-frame is described in section 1.2.

The sequence of bits $s_{1,1}, s_{1,2}, \dots, s_{1,40}$ is mapped to the first slot of the HS-SCCH sub frame. The bits $s_{1,k}$ are mapped to the PhCHs so that the bits for each PhCH are transmitted over the air in ascending order with respect to k .

The sequence of bits $r_{2,1}, r_{2,2}, \dots, r_{2,80}$ is mapped to the second and third slot of the HS-SCCH sub frame. The bits $r_{2,k}$ are mapped to the PhCHs so that the bits for each PhCH are transmitted over the air in ascending order with respect to k .

3 Coding for HS-DPCCH

Data arrives to the coding unit in form of indicators for measurement indication and HARQ acknowledgement.

The following coding/multiplexing steps can be identified:

- channel coding (see subclause 3.1);
- mapping to physical channels (see subclause 3.2).

The general coding flow is shown in the figure below. This is done in parallel for the HARQ-ACK and CQI as the flows are not directly multiplexed but are transmitted at different times.

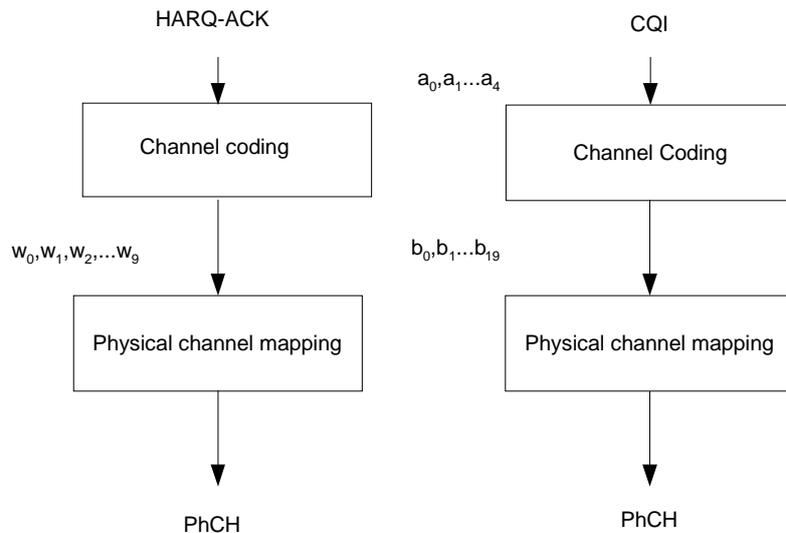


Figure 9: Coding for HS-DPCCH

3.1 Channel coding for HS-DPCCH

Two forms of channel coding are used, one for the channel quality information (CQI) and another for HARQ-ACK (acknowledgement).

3.1.1 Channel coding for HS-DPCCH HARQ-ACK

The HARQ acknowledgement message to be transmitted, as defined in [TS 25.213], shall be coded to 10 bits as shown in Table 5. The output is denoted w_0, w_1, \dots, w_9 .

Table 5: Channel coding of HARQ-ACK

HARQ-ACK message to be transmitted	w_0	w_1	w_2	w_3	w_4	w_5	w_6	w_7	w_8	w_9
ACK	1	1	1	1	1	1	1	1	1	1
NACK	0	0	0	0	0	0	0	0	0	0

3.1.2 Channel coding for HS-DPCCH channel quality information

The channel quality information is coded using a (20,5) code. The code words of the (20,5) code are a linear combination of the 5 basis sequences denoted $M_{i,n}$ defined in the table below.

Table 6: Basis sequences for (20,5) code

i	$M_{i,0}$	$M_{i,1}$	$M_{i,2}$	$M_{i,3}$	$M_{i,4}$
0	1	0	0	0	1
1	0	1	0	0	1
2	1	1	0	0	1
3	0	0	1	0	1
4	1	0	1	0	1
5	0	1	1	0	1
6	1	1	1	0	1
7	0	0	0	1	1
8	1	0	0	1	1
9	0	1	0	1	1
10	1	1	0	1	1
11	0	0	1	1	1
12	1	0	1	1	1
13	0	1	1	1	1
14	1	1	1	1	1
15	0	0	0	0	1
16	0	0	0	0	1
17	0	0	0	0	1
18	0	0	0	0	1
19	0	0	0	0	1

The CQI values 0 .. 30 as defined in [TS 25.213] are converted from decimal to binary to map them to the channel quality information bits (1 0 0 0 0) to (1 1 1 1 1) respectively. The information bit pattern (0 0 0 0 0) shall not be used in this release. The channel quality information bits are a_0, a_1, a_2, a_3, a_4 (where a_0 is LSB and a_4 is MSB). The output code word bits b_i are given by:

$$b_i = \sum_{n=0}^4 (a_n \times M_{i,n}) \bmod 2$$

where $i = 0, \dots, 19$.

3.2 Physical channel mapping for HS-DPCCH

The HS-DPCCH physical channel mapping function shall map the input bits w_k directly to physical channel so that bits are transmitted over the air in ascending order with respect to k .

The HS-DPCCH physical channel mapping function shall map the input bits b_k directly to physical channel so that bits are transmitted over the air in ascending order with respect to k .