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A Temperature-Aware Analysis of SAR ADCs for Smart Vehicle Applications

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Abstract—The challenges of the Internet of Things (IoT) in an urban environment are driven by smart vehicles which need to be able to efficiently sense and communicate with other nearby vehicles. The automotive market have strict circuit performances and reliability requirements for a temperature range of up to 175 °C. This proposal overviews an analysis of latched-comparators performance, considering process variability and temperature variation of previous works. This analysis is then extended to the metastability and performance metrics of successive approximation register (SAR) analog-to-digital converter (ADC) topology. Building blocks necessary for the SAR ADC are designed using an XH018 technology. Post-layout simulation results are drawn to validate the proposed temperature-aware analysis. Besides the known advantages of the Double-Tail comparator, this work demonstrates that such a comparator has a serious drawback under harsh environments. This proposal also shows that, once calibrated and operated at a frequency of around 100 MHz, the SAR ADC performance can be maintained in a wide temperature range. Both SA- and DT-SAR ADC achieve an ENOB of 9.8 bits, which is reduced to 9.6 bits in high-temperature operation. The results also show that background calibration is not required for the SAR ADC operation at the 100 MHz frequency range.

Index Terms—temperature-aware, latched comparators, SAR ADC, reliability, smart vehicle

I. INTRODUCTION

The advent of the Internet of Things (IoT) has brought the need for novel studies to conform to its extensive requirements, driven specifically by the Smart Vehicle industry. Smart vehicles must be able to efficiently sense and communicate with other nearby vehicles, including cars, buses and trucks. For obvious reasons, the design and specification of microelectronic circuits, which are used in these applications, are regulated by many strict security and safety standards. Reliability and robustness in the device operation must be ensured for harsh environments [1], including the required operating temperature range from -40 °C to 175 °C. This temperature range is arguably the most difficult environment challenge for electronics in the automotive industry [2]. Hence, in order to meet the IoT challenge, smart vehicles must integrate high performance electronics over a wide temperature range.

In the domain of vehicle smart sensing, the analog to digital interface is a challenge. Analog-to-digital converters (ADC) should remain reliable even under performance variation [3].

Zurita *et al.* have reported that a successive approximation register (SAR) ADC based on capacitive Digital-Analog Converter (DAC) is the most appropriated solution, achieving the best results in technology nodes below 350 nm [4]. In this proposal, the SAR ADC is designed with state of the art comparator circuits. The most common comparator designs are the StrongArm (SA) [5] and the Double-Tail (DT) latched comparators [6]. Many studies compare both SA and DT topologies, compiling a series of well-defined design parameters and considerations, even proposing changes to better increase the comparators' performances. Literature has also focused on SAR ADC topology improvements, without mentioning the drawbacks of a comparator failure. As the best of our knowledge, they lack the variability analysis of the SAR ADC performance, considering the impact of temperature variation on the comparator behavior.

The aim is then to extend the temperature-aware analysis proposed by Fonseca *et al.* [7] for performance variability in state-of-the-art SAR ADC which employs latched SA and DT comparators. This proposal overviews the temperature effects on MOS devices, covers the comparators design parameters in order to address performance variations (i.e. offset, delay and noise), and extends it including metastability and switch on-resistance variation. Besides, this proposal also evaluates the SAR ADC performance variations (i.e. INL and DNL) under temperature variation (from -40 °C to 175 °C). All circuit design is carried out using XH018 process technology from the XFAB Silicon Foundries. XH018 technology is ideal for system-on-chip (SoC) applications in the automotive market such as control devices inside combustion engine compartments or electric engine housings with temperature range up to 175 °C, as well as embedded low-voltage applications in the communications, consumer and industrial market [8]. Such technology is a SOI process, which uses a deep-trench buried oxide that leads to a very low junction leakage current even at high temperatures. According to foundry models, it is reported 3 pA of leakage current for measured transistors with 10 nA of drain-to-source bias current and 100 pA leakage for 80 μ A bias current at 175 °C.

Sec. II introduces the SAR ADC topology under analysis, revising the state-of-the-art of temperature-aware ADCs. Sec. III presents a detailed analysis of the temperature variations.

Sec. IV presents post-layout Monte Carlo simulations carried out over temperature variation. Finally, conclusions concerning the theory and post-layout simulated results are drawn.

II. BACKGROUND

The operation of ADCs at high temperatures is a well-known problem stated by Sullivan *et al.* in 1981 [9]. According to that work, a temperature-aware ADC design is challenging since only little information concerning the different types of components and their properties at high temperature is available. For aerospace application, as in Sullivan's work, many solutions are already commercially available. However, the challenge reported by Sullivan *et al.* remains valid, because having the required information of device performance and their properties at high temperature is costly, and this cost cannot be afforded by the smart vehicle industry.

Davis and Finvers have published an experimental verification of an ADC for high-temperature applications in a standard CMOS process [10]. The use of standard CMOS processes opens an opportunity to reduce the cost of temperature-aware devices in the smart vehicle market. The reported ADC achieved a signal to noise and distortion (SINAD) ratio of 88 dB at 223 °C, but a sampling frequency of only 256 kHz. However, for smart vehicle applications, a higher sampling frequency is mandatory to provide the demanding functionality in a vehicle computer board.

Recently, Zurita *et al.* have reported that a SAR ADC based on capacitive DAC is the most appropriated solution, achieving the best results in technology nodes below 350 nm [4]. Zurita's ADC is designed using a 180 nm CMOS technology like this proposal. Zurita's ADC has achieved 85.3 fJ/Conversion-step and an ENOB of 9.5 bits. However, a temperature-aware analysis of SAR ADCs remains an unexplored topic.

The SAR ADC's principle is to find by dichotomy the binary representation of the input voltage as illustrated in Fig. 1. The SAR under analysis in this proposal uses charge balancing to compare the input signal to different reference levels in succession. In other words, a switched capacitor network is used to realize both the DAC functionality and the summation. Classic SARs employ a capacitive network using capacitors with a binary ratio of a unitary value. In this proposal, the capacitive network is split, keeping the binary ratio by either connecting capacitors in parallel or by weighting down part of the capacitor bank. This method leads to less thermal noise by introducing an attenuation capacitor connected between the least- and the most-significative capacitor banks. A detailed description of the topology working principle is given in [4].

III. TEMPERATURE DEPENDENT ANALYSIS

A. Temperature Effects

The effects of temperature on system dynamics and behavior have been widely studied. Since 1995, C. Park *et al.* have described the trade-off between mobility (μ) and threshold voltage (V_{TH}) under temperature variation [11]. This trade-off causes a varying temperature dependency on the transistor current. In the 180 nm XH018 XFAB technology, as in other usual CMOS technologies, for transistors operating with a V_{GS}

voltage significantly greater than the threshold voltage, their current will always decrease with temperature [2].

According to Mathiessen's equation and the BSIM device model, the transistor's mobility (μ) and the threshold voltage (V_{TH}) vary with temperature with the following expressions:

$$\mu(T) = \mu_0 \cdot \left(\frac{T}{T_0}\right)^{-\beta_\mu} \quad [2], \quad (1)$$

$$V_{TH}(T) = V_{th0} + \alpha_{V_{th}}(T - T_0) \quad [12], \quad (2)$$

where $\alpha_{V_{th}}$, in mV/K, and β_μ are technology-dependent temperature coefficients.

B. Transmission Gates

Transmission Gates (TG) using CMOS switch topology illustrated in Fig. 2 are passive devices which only consume dynamic or leakage power. However, resistance linearity over signal dynamic range (sig_{DR}) is critical. The on-resistance variation degrades signal quality by introducing non-linearities in the ADC response. Transmission gate design optimization is carried out through simulation-driven results to minimize the on-resistance variation in the transient response.

The transmission gate on-resistance (R_{SW}) is given by:

$$R_{SW} \propto \frac{1}{(\mu_n W_n / L + \mu_p W_p / L)(sig_{DR} - V_{TH})}, \quad (3)$$

assuming V_{TH} NMOS and PMOS equal. Under this hypothesis, one may conclude that the best resistance linearity over sig_{DR} is achieved for $\mu_n \cdot W_n \approx \mu_p \cdot W_p$, this product will be identified from this point on as $W \cdot \mu$. To derive a temperature-sensitive behavior, the on-resistance R_{SW} is derived with respect to the temperature as

$$\frac{\partial R_{SW}}{\partial T} = \frac{\alpha_\mu}{(2W \cdot \mu^2 (V_{TH} - sig_{DR}))} + \frac{\alpha_{V_{th}}}{(2W \cdot \mu (V_{TH} - sig_{DR})^2)}, \quad (4)$$

having $\alpha_\mu = \frac{\partial \mu}{\partial T} \approx -1.5$. According to (4), R_{SW} shall increase as temperature increases (i.e. $sig_{DR} > V_{TH}$) leading to sampling fail for high frequency operation. Under this effect, the voltage stored in the capacitor bank would not achieve the final value sampled from the input-voltage. Thus, R_{SW} variations over temperature cause ADC non-linearities that require a difficult calibration in digital domain. To avoid such non-linearities, a sizing optimization is carried out, and the $W \cdot \mu$ is obtained using electrical simulations.

C. Latched Comparators

In SAR ADCs, latched comparators are one key building block and are responsible for the correct bit decision in time. Temperature effects in latched comparators could cause a decision mistake (e.g. bit-flip) and an increasing delay. There are two usual choices for latched comparators: the StrongArm (SA) and the Double-Tail (DT) architectures. Here, this paper overviews the temperature-aware analysis first presented in [7].

The SA comparator, shown in Fig. 3(a), is the improved version as designed by [5]. These comparators are known by their fast response with a good trade-off in power consumption. The DT-comparator topology analyzed in this proposal,

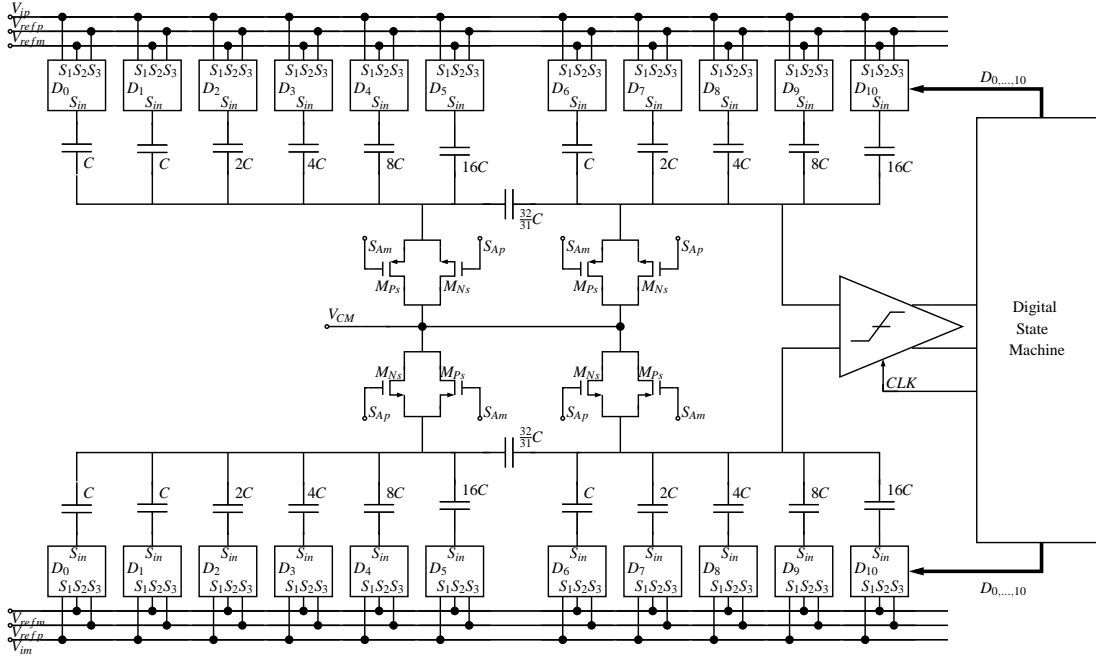


Fig. 1. A SAR ADC based on capacitive network using capacitors with a binary ratio, having least- and most-significant capacitors bank separated by a split capacitor.

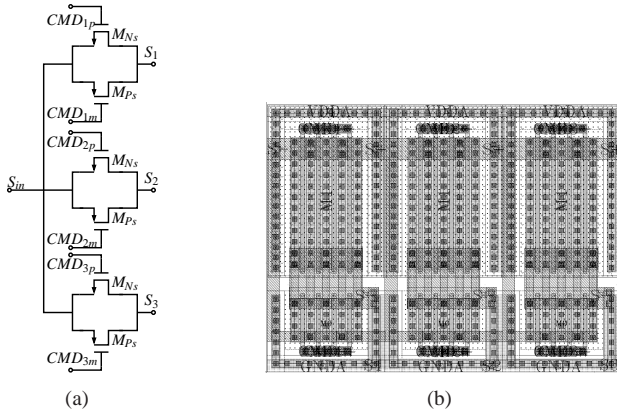


Fig. 2. SAR Transmission Gates using a CMOS switch topology: (a) schematics, (b) layout having $16 \times 12 \mu m^2$.

shown in Fig. 3(b) was first proposed by Schinkel *at al.* in [6]. DT comparators were introduced because of their improved performance, especially in kick-back noise. The DT comparator's behavior can be separated into three phases: pre-charge, decision, and regeneration.

To study the temperature effects, electrical simulations were carried out with approximately the same conditions for the transistors in the differential pairs of both comparators. In other words $V_{GS} = \frac{V_{DD}}{2} = 900 \text{ mV}$ and $V_{DS} = V_{DD} = 1.8 \text{ V}$, while maintaining the same sizing. The extracted temperature coefficients in the XH018 180 nm technology, using n-type transistor, are: $\alpha_{V_{th}} \approx -0.7 \text{ mV/K}$, and $\beta_{\mu} \approx 1.5$. These results are required when deriving the system dependencies in the comparators.

1) *StrongArm Delay*: The proposed temperature-aware analysis is based on a previous proposal presented by Babayan-Mashhadi and Lotfi on the delay analysis of SA and DT comparators [13]. The operation of the SA comparator can be separated into three main phases: a pre-charge, a decision delay and a regeneration phase. The pre-charge phase occurs for $CLK = 0$ and the two latter for $CLK = 1$. In the pre-charge phase, switches S_1 - S_4 are turned on, charging nodes X_1 , X_2 , V_{OUT_p} and V_{OUT_m} to V_{DD} . It will be assumed that these nodes are completely charged by the time CLK rises to 1. This is a very plausible assumption, considering a 100 MHz operating frequency for the comparator.

During the decision delay phase, M_7 turns on, permitting transistors M_1 and M_2 to conduct. Each branch current, i.e. I_{DM1} and I_{DM2} , begins to discharge nodes X_1 and X_2 . Assuming $V_{IN_p} > V_{IN_m}$, the node X_1 will discharge faster until it reaches the voltage level of $V_{DD} - V_{TH}$. Considering a capacitance C_{LX} at the node X_1 this would cause a first delay time t_{o1} described by,

$$t_{o1} = \frac{C_{LX} V_{THN}}{I_{DM1,2}}, \quad (5)$$

Considering that the input difference voltage is too small in this case, then

$$I_{DM1,2} = I_{bias} + g_m \Delta V \approx I_{bias}, \quad (6)$$

where $I_{DM1,2}$ is the total current that passes through either the transistor M_1 or M_2 , g_m is the transistor's transconductance, and I_{bias} is the bias current in the transistors of the differential pair.

Employing the quadratic model for the MOS transistor, results

$$I_{bias} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{CM} - V_{TH})^2, \quad (7)$$

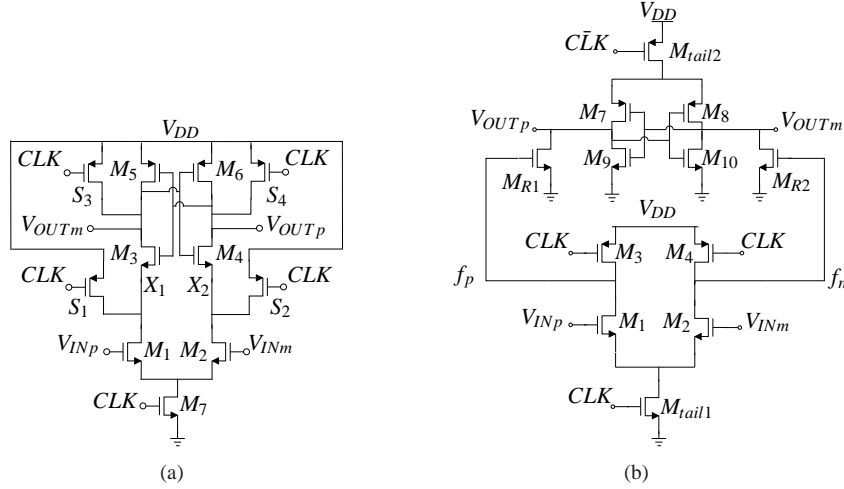


Fig. 3. Comparator Schematic of (a) StrongArm; (b) Double-tail.

where V_{CM} is the common mode bias voltage at the inputs of the comparator.

As soon as X_1 reaches the voltage level of $V_{DD} - V_{THN}$, the transistor M_3 begins to conduct and consequently discharges the node V_{OUTm} . This next step adds an extra delay time t_{o2} as

$$t_{o2} = \frac{C_L |V_{THP}|}{I_{DM1,2}}, \quad (8)$$

where C_L is the capacitance at V_{OUTp} node.

The total time (t_o) that the latch takes to enter in the regeneration phase is then $t_{o1} + t_{o2}$. Considering that $|V_{THP}| \approx V_{THN} = V_{TH}$ and $C_L \approx C_{LX}$, then

$$t_o = t_{o1} + t_{o2} = \frac{2 \cdot C_L V_{TH}}{I_{DM1,2}}. \quad (9)$$

The t_o temperature dependency is obtained by analyzing the two temperature-dependent parameters V_{TH} and μ . The V_{TH} and μ dependencies described in (2) and (1) are used to derive the t_o temperature dependency as

$$\frac{\partial t_o}{\partial T} = 2 \cdot \frac{C_L}{I_{bias}} \left(\alpha_{V_{TH}} - \alpha_{I_{bias}} \frac{V_{TH}}{I_{bias}} \right), \quad (10)$$

where $\alpha_{I_{bias}}$ and $\alpha_{V_{TH}}$ are the temperature coefficients. The value of $\alpha_{I_{bias}}$ can be found using

$$\alpha_{I_{bias}} = \frac{\partial I_{bias}}{\partial T} = \frac{1}{2} g_m \left(-\beta_\mu \frac{(V_{CM} - V_{TH})}{T} - 2 \cdot \alpha_{V_{TH}} \right). \quad (11)$$

In order to prove that t_o delay increases as temperature increases, it is sufficient to prove that

$$\alpha_{V_{TH}} - \alpha_{I_{bias}} \frac{V_{TH}}{I_{bias}} > 0. \quad (12)$$

Considering the typical mean $V_{TH} \approx 400$ mV in the XH018 technology, a g_m in the order of magnitude of hundreds of μS and I_{bias} in the order of magnitude of tens of μA , one may conclude that the condition (12) is met.

2) *Double-Tail Delay*: In the pre-charge phase, $CLK = 0$ turns switches M_3 and M_4 on to respectively charge the nodes f_p and f_n to V_{DD} . It is assumed that these nodes are completely charged by the time when $CLK = 1$. These nodes charged to V_{DD} force the transistors M_{R1} and M_{R2} to conduct. Thus, the two output nodes are forced to ground.

In this case, the decision (t_o) delay can be identified as the time it takes for either the f_p or the f_n node voltage to discharge from V_{DD} to V_{TH} . As soon as M_{tail1} begins to conduct, M_1 and M_2 begin to discharge f_p and f_n , respectively. Considering $V_{INp} > V_{INm}$, f_p node discharges faster than f_n . As soon as f_p reaches the voltage value of V_{TH} , M_{R1} no longer forces the ground voltage on V_{OUTp} , and the comparator latches in its regenerative phase. In order to calculate the decision delay time t_o in this topology, it is considered the variation in the voltage f_p and its final voltage V_{TH} as

$$V_{DD} - \frac{I_D}{C_L} t_o = V_{TH}, \quad (13)$$

where I_D is the current provided by M_1 and C_L is the output node capacitance. Considering a small input differential voltage, $I_{DM1} \approx I_{bias}$, where $_{bias}$ is the bias current of the transistors in the differential pair.

Considering the temperature variation of the current I_{bias} and V_{TH} , the temperature effects on the delay are due to a decrease of V_{TH} and of I_{bias} , that implies a decrease on the discharge rate of the f_p node voltage. This combined effect increases even more the delay in both cases. To clearly demonstrate the delay t_o , the following relation is found

$$t_o = \frac{C_L (V_{DD} - V_{TH})}{I_{bias}}. \quad (14)$$

In order to derive a temperature-sensitive behavior, the total delay t_o is derived with respect to the temperature as

$$\frac{\partial t_o}{\partial T} = \frac{C_L}{I_{bias}} \left(-\alpha_{V_{TH}} - \alpha_{I_{bias}} \frac{(V_{DD} - V_{TH})}{I_{bias}} \right), \quad (15)$$

where the rise in the t_o delay due to temperature increase is proven by showing that

$$-\alpha_{V_{TH}} - \alpha_{I_{bias}} \frac{(V_{DD} - V_{TH})}{I_{bias}} > 0. \quad (16)$$

Considering the same values as previously, the condition in (16) is met and the delay will always increase with temperature. On the instant that V_{DS} drops low enough, the transistor changes its operating region to the ohmic region. From this point, the current will continue to reduce independently of temperature effects. In other words, it can be assumed that delay time always increases when the temperature increases. Theoretically, (15) also shows that the t_o delay in the DT comparator is much more sensitive to temperature variations than in SA comparators.

In both the SA and the DT comparators, one can identify the effects on t_o as the main agent of the system delay degradation. However, it is possible to show how the delay of the regeneration phase (t_{latch}) is also affected by the temperature variations. In fact, both SA and DT comparators have similar t_{latch} degradation. The time it takes for the differential signal to regenerate to a stable value is inversely dependent on the gain of the back to back inverters, as shown by the equation developed in [14],

$$t_{latch} = \frac{C_L}{G_m} \ln \left(\frac{V_{DD}/2}{\Delta V_o} \right), \quad (17)$$

where C_L represents the capacitance of the output node, G_m the transconductance gain of the inverters and ΔV_o the voltage difference between the output nodes. It can then be deduced that, by increasing the temperature, and thus reducing the gain of the transistors, t_{latch} is increased.

3) *Comparator Offset*: Input-referred offset in latched comparators can be evaluated by taking into account two main parts, the offset coming from the mismatch in the differential pair and the one in the latch [15] in the following way

$$V_{OS,i-total} = \sqrt{V_{OS-diffpair}^2 + \frac{1}{G^2} V_{OS-latch}^2}, \quad (18)$$

where $V_{OS-diffpair}$ and $V_{OS-latch}$ are the offsets in each stage and the voltage gain G before the latch. In the case of the SA comparator, this gain comes from the differential pair, but for the DT comparator, it is the differential pair gain multiplied by the gain from M_{R1} or M_{R2} transistors. If one considers that the gain G is significant enough to neglect the effects of the latch offset, a simple differential pair mismatch analysis can be done. The standard deviation of the offset in a differential pair is given by [16]

$$\sigma^2 V_{OS-diffpair} = \frac{\sigma^2 \Delta I_D}{g_m^2}, \quad (19)$$

where $\sigma^2 \Delta I_D$ is given by,

$$\sigma^2 \Delta I_D = \frac{2}{WL} \left[g_m^2 A_{VT0}^2 + \left(\frac{I_D}{K} \right)^2 A_K^2 \right], \quad (20)$$

where $K = \mu C_{ox} \left(\frac{W}{L} \right)$; A_{VT0} is a technology-defined variability constant for the V_{TH} and A_K for the K . One can find the offset of the differential pair as

$$\sigma^2 V_{OS-diffpair} = \frac{2}{WL} \left[A_{VT0}^2 + \left(\frac{I_D}{K g_m} \right)^2 A_K^2 \right], \quad (21)$$

Assuming the comparators' layout is compact enough, the temperature variation equally affects all transistors. In fact, all transistors maintain the same temperature gradient; and temperature effects behave as a common-mode variation. One may assume that A_{VT0} and A_K remain constant with temperature and are process dependent [14]. Although the coefficients multiplying A_K^2 are temperature variant, A_{VT0}^2 will always dominate. As a result, the offset voltage in both topologies is mostly unaffected by temperature variation in the differential pair. Since the differential pair provides the biggest impact on the offset voltage, it is reasonable to conclude that the offset will present a negligible dependence on temperature.

4) *Comparator Metastability*: The fundamental limitation of a SAR ADC toward high speed is the metastability. Metastability is an inability of a latched comparator to produce a valid decision in a certain available time [17]. This error phenomenon is difficult to predict, since it depends on the applied input and the comparator topology. This proposal focuses here in temperature effects that could impact latched comparator characteristics inducing a metastability failure. From this knowledge, it would be possible to determine the SAR ADC speed limitation to avoid a failure. More details about metastability in SAR ADCs can be found in [17].

Comparator metastability is a process for which an initial ΔV_{out} of the cross-coupled inverters is insufficient for output regeneration to reach valid logic levels before the end of the available time (t_{AVL}). The output range variation (ΔV_{OUT}) can be determined as the value for which the delay time exceeds the maximum time to make a decision. Unfortunately, the probability distribution of the differential input voltage and the noise [18] influences the probability distribution of the comparator delay. Thus, the likelihood of metastability is affected.

The input probability distribution depends on the shape of the input voltage waveform [17]. For a Gaussian distribution of the delay at a given ΔV_{in} , the probability of the comparator metastability is given by

$$P(t > t_{AVL}, \Delta V_{in}) = \frac{1}{2} \left(1 - \operatorname{erf} \left(\frac{t_{AVL} - \mu_{delay}(\Delta V_{in})}{\sqrt{2} \sigma_{delay}(\Delta V_{in})} \right) \right), \quad (22)$$

where μ_{delay} is the average of the delay as a random variable; and σ_{delay} the standard deviation of the delay, assuming the law of large numbers. Such μ_{delay} and σ_{delay} are estimated from the delay modeling under temperature variation, presented in Sec. III-C1 and III-C2.

In both SA and DT comparators, the pre-amplification phase effectively multiplies the input range by a dynamic gain of A_P [19]. One should subtract t_o (derived in Sec. III-C1 and III-C2) from system t_{AVL} . Considering that t_o is a Gaussian distributed

random variable [19], errors on the estimation of the delay and its standard deviation can be translated into an error on the metastability probability. This error on the probability is given by

$$\begin{aligned} \varepsilon_{P_{met}} = & \\ & \frac{1}{2} \cdot \int_{-V_{FS}/2}^{+V_{FS}/2} \operatorname{erf} \left(\frac{t_{AVL} - \mu_{delay} + \varepsilon_{\mu}}{(\sigma_{delay} + \varepsilon_{\sigma})\sqrt{2}} \right) P(\Delta V_{in}) d\Delta V_{in} \\ & - \frac{1}{2} \cdot \int_{-V_{FS}/2}^{+V_{FS}/2} \operatorname{erf} \left(\frac{t_{AVL} - \mu_{delay}}{\sigma_{delay}\sqrt{2}} \right) P(\Delta V_{in}) d\Delta V_{in}, \quad (23) \end{aligned}$$

where V_{FS} is the full-scale output-voltage (i.e. V_{DD}), and $P(\Delta V_{in})$ represents the probability to get a specific value of ΔV_{in} given by a Laplace distribution of probability [20].

To derive a temperature-sensitive behavior, metastability probability variation to temperature is estimated by the first derivative as

$$\begin{aligned} \frac{d}{dT} P(t > t_{AVL}, \Delta V_{in}) = & \\ & \frac{\partial}{\partial \mu_{delay}} P(t > t_{AVL}, \Delta V_{in}) \cdot \frac{d\mu_{delay}}{dT} + \\ & \frac{\partial}{\partial \sigma_{delay}} P(t > t_{AVL}, \Delta V_{in}) \cdot \frac{d\sigma_{delay}}{dT}. \quad (24) \end{aligned}$$

According to temperature effects presented in Sec. III-A, carrier mobility and threshold voltage can only decrease. From these phenomena, both SA and DT comparator delay could only increase in the direction of a delay greater than t_{AVL} . Thus, an increasing temperature would increase the metastability probability.

IV. POST-LAYOUT RESULTS

A. SAR Transmission Gates Results

SAR transmission gates are designed using the XH018 180 nm technology which is measured and modeled for the -40 °C to 175 °C temperature range [8]. NMOS transistor sizing is $8 \mu\text{m}$ over 180 nm using 4 fingers. PMOS transistor sizing is $24 \mu\text{m}$ over 180 nm using 4 fingers. Fig.2(b) shows the SAR transmission gate layout, having an area of $16 \times 12 \mu\text{m}^2$. This sizing favored a better linearity in high temperature, where the increasing on-resistance limits the SAR's frequency operation. Post-layout simulation results presented in Fig. 4(a) validates the design choice and confirms the expected trade-off. A 1001-points Monte Carlo post-layout simulation over a 11-points temperature sweep in a range from -40 °C to 175 °C is presented in Fig. 4(b) for R_{SW} mean ($\mu_{R_{SW}}$) and worst case (WC) condition at $\mu_{R_{SW}} + 3\sigma_{R_{SW}}$. Fig. 4(b) highlights an increasing resistance over temperature with a linear-dependency, which validates the behavior in (4). The resulting R_{SW} is always lower than 180Ω .

B. Latched Comparators Results

Both SA and DT comparators are designed using the XH018 180 nm technology which is measured and modeled for the -40 °C to 175 °C temperature range [8]. Table I presents transistor sizing for SA (see Fig 3(a)) and DT comparators

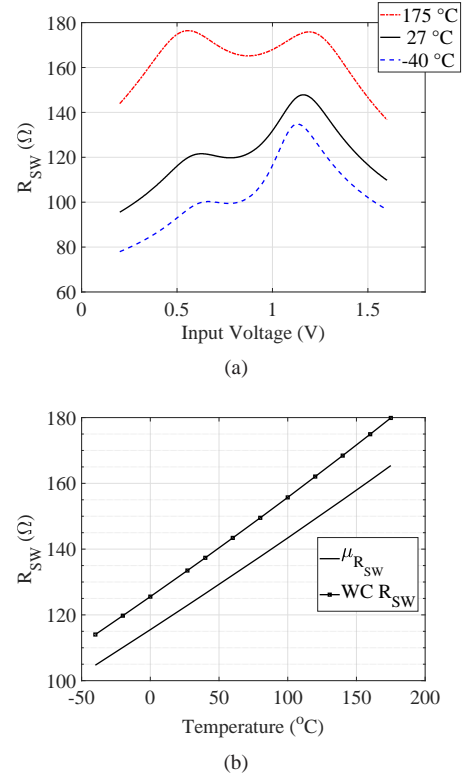


Fig. 4. SAR transmission gates on-resistance (R_{SW}) for: (a) 1001-points input-voltages post-layout simulation for a temperature variation of -40 °C (dashed blue line), 27 °C (continuous black line), and 175 °C (dashed-dotted red line); (b) 151-points Monte Carlo post-layout simulation over a 11-points temperature sweep in a range from -40 °C to 175 °C for R_{SW} mean (continuous black line) and worst case (WC) (square marks) for 3σ .

(see Fig 3(b)) [7]. The layout of both comparator topologies is implemented using state of the art techniques. To efficiently compare both topologies, the layout is carried out minimizing mismatch, achieving a similar area, and placing I/O pins at the same positions. Fig. 5(a) shows the SA comparator layout, having an area of $49 \times 10 \mu\text{m}^2$; and Fig. 5(b) shows the DT comparator layout, having an area of $52 \times 10 \mu\text{m}^2$.

TABLE I
TRANSISTOR SIZING OF SA AND DT COMPARATORS (W X L).

	SA [5]		DT [6]
M_{1-2}	$14.4 \mu\text{m} \times 720 \text{ nm}$	M_{1-2}	$14.4 \mu\text{m} \times 720 \text{ nm}$
M_{3-6}	$7.2 \mu\text{m} \times 720 \text{ nm}$	M_{3-4}	$1.1 \mu\text{m} \times 180 \text{ nm}$
M_7	$1.1 \mu\text{m} \times 180 \text{ nm}$	$M_{R1,2}$	$3.6 \mu\text{m} \times 720 \text{ nm}$
S_{1-4}	$1.1 \mu\text{m} \times 180 \text{ nm}$	M_{7-10}	$7.2 \mu\text{m} \times 720 \text{ nm}$
		$M_{tail1,2}$	$1.1 \mu\text{m} \times 180 \text{ nm}$

To prove the temperature dependency of t_o described in Subsec. III-C1 and III-C2, a first experiment is drawn based on a post-layout transient simulation. The simulation parameters are: 100 MHz clock, a 1 ps strobe period, a common mode voltage of 900 mV and a differential voltage of 10 mV between input nodes. At the clock's rising edge, the simulation time is started as 0 ns in the X-axis; and it runs until 1 ns (sufficient time to observe t_o for a 10 mV differential input). For the SA comparator, X_1 and V_{OUTm} nodes are inspected (Y-axis). For the DT comparator, f_p and V_{OUTp} nodes are inspected (Y-axis).

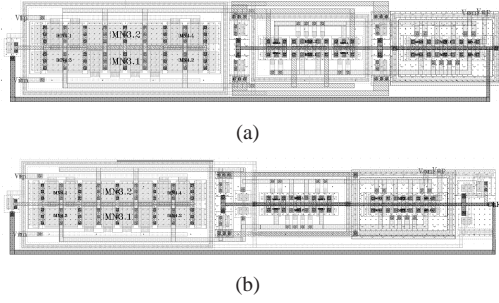


Fig. 5. Latched comparators' layout of (a) SA having an area of $49 \times 10 \mu\text{m}^2$ and (b) DT having $52 \times 10 \mu\text{m}^2$.

It is expected that X_1 and f_p discharge until t_o according to (9) for SA comparator and (14) for DT comparator. Fig.6 shows SA and DT post-layout simulation results for temperatures of -40°C (dashed blue line), 27°C (continuous black line), and 175°C (dashed-dotted red line).

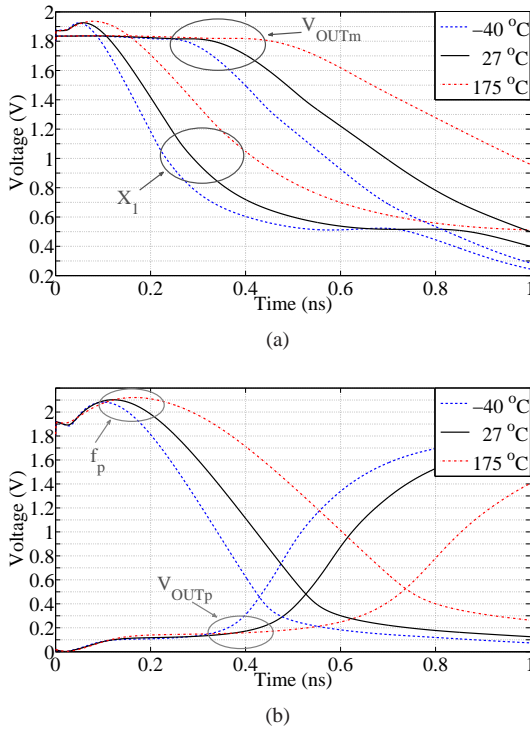


Fig. 6. Post-layout transient simulation of (a) X_1 and V_{OUTm} for SA; and (b) f_p and V_{OUTp} for DT comparators in a temperature variation of -40°C (dashed blue line), 27°C (continuous black line), and 175°C (dashed-dotted red line).

Fig. 6(a) highlights SA operation when decision is being taken. One can notice that the V_{OUTm} begins to latch around the same instant of time as the node X_1 achieves the voltage level $V_{DD} - 2 \cdot V_{TH}$. This voltage level represents that the node X_1 has discharged two times the value of V_{TH} , when V_{outm} decreases to $V_{DD} - V_{TH}$. This point indicates the beginning of the latching phase; and it marks t_o for SA comparator. Among temperature variation curves, it is remarkable the t_o increase due to a decreasing in the discharge rate and in the transistor V_{TH} . This validates the analysis presented in Subsec. III-C1 derived in (10).

Fig.6(b) highlights DT operation while f_p is discharging and V_{OUTp} is rising. The delay t_o can be identified as the time when the f_p node voltage reaches around one V_{TH} . Also, DT comparator latching is delayed as temperature increases due to the decrease in the discharge rate and in the threshold voltage. This validates the analysis presented in Subsec. III-C2, derived in (15).

Since latched comparators are time-varying circuits, the following experiments are run using a post-layout periodic-steady-state simulation. The test-bench used for the presented results was inspired by [21] and [22]. Delay, offset, and power consumption are evaluated in a 151-point Monte Carlo simulation over a 11-point temperature sweep in a range from -40°C to 175°C . The test-bench proposed in [21] can put latched comparator as close as possible of its metastable operation. In this case it achieves the maximum delay for an input differential voltage equal to the comparator offset voltage. Power consumption is obtained by the RMS power consumed for one cycle in a periodic-steady-state regime.

Fig. 7 presents the statistical results of the post-layout comparator delay in both architectures. The data is represented as a plot of the average delay values with an error bar representing three times the standard deviation for each temperature point. While temperature increases, an almost linear increase of the mean delay is noticeable. This behavior was predicted in the previous transient simulations and it is in agreement with the theoretical analysis presented in (10) and (15). From a linear fit, a delay temperature-coefficient of 6.3 ps/K for the SA comparator and 6.29 ps/K for the DT comparator are found. In fact, both SA and DT comparators delays vary with the same temperature coefficient. However, the DT comparator is always slower due to its larger t_o for all temperatures. The temperature effect in delay standard deviation is diminished in the DT comparator, this may be due to the much faster regeneration phase as compared to the SA comparator. Additionally, a worse case delay greater than 2.5 ns (a quarter of clock period) is found. These results might suggest a comparator failure at high-temperature operation.

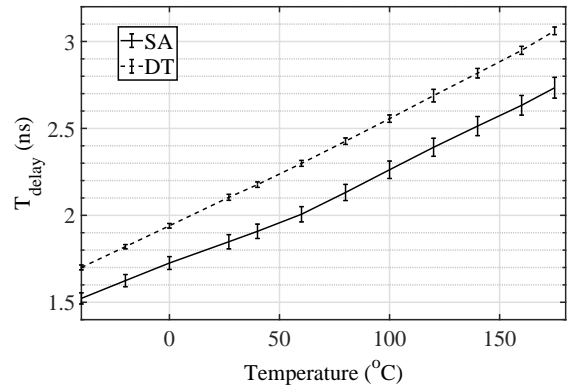


Fig. 7. A 151-points Monte Carlo post-layout simulation over a 11-points temperature sweep in a range from -40°C to 175°C for SA and DT comparator mean delay with a 3σ error bar.

The average offset of both comparators is around zero as expected, that is why Fig. 8 shows only the standard deviation

of the comparators' input-referred offset ($3\sigma V_{OS,i-total}$). The $3\sigma V_{OS,i-total}$ data over temperature does not change significantly. This behavior validates the theory as predicted in (21). One may conclude that the SA $3\sigma V_{OS,i-total}$ is less sensitive to temperature variation. Even if the SA presents a higher $3\sigma V_{OS,i-total}$ than the DT, due to the additional gain provided by the $M_{R1,2}$ transistors, DT $3\sigma V_{OS,i-total}$ variation is three times bigger than SA $3\sigma V_{OS,i-total}$ variation over the temperature range. In order to have a complete understanding of the input-referred offset, post-fabrication testing must be done. The input-offset's variability constants in (21) present a strong process dependency.

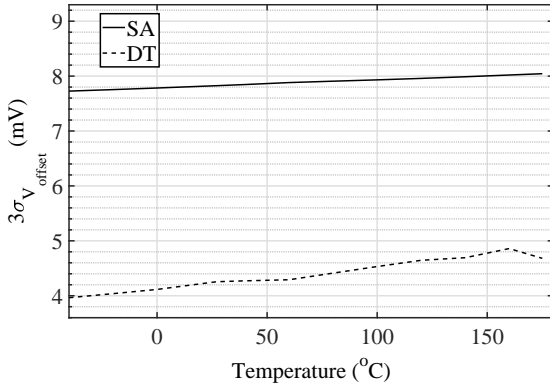


Fig. 8. A 151-points Monte Carlo post-layout simulation over a 11-point temperature sweep in a range from -40°C to 175°C for SA and DT comparator $3\sigma V_{offset}$.

In high-temperature conditions, thermal noise becomes a major issue for a correct decision as it is statistically added to the comparator offset. The output-referred noise is estimated from a periodic noise analysis. Input-referred noise is estimated from the output-referred noise and the comparator gain. This gain is obtained from a periodic AC analysis evaluated at the instant the comparator achieves its decision threshold (i.e. $V_{DD}/2$) at the output nodes. Details of the test-bench setup are presented in [21] and [22].

Fig. 9 presents the mean and the worst case (WC) of SA and DT input-referred noise, obtained from a 151-points Monte Carlo post-layout simulation over a 11-point temperature sweep. The WC is the defined by $\mu_{n,i} + 3\sigma_{n,i}$. Since thermal noise is linearly dependent on temperature, SA and DT input-referred noise increase linearly; but the standard deviation increases slightly faster than the mean. The DT presents more noise than the SA; and DT noise increases at a much faster rate. Considering noise as an additive source of decision errors such as offset voltage, the lower offset of the DT comparator is payed off by a higher noise. This trade-off is due to the extra DT transistors increasing gain, reducing offset voltage, but generating more noise. Indeed, thermal noise under temperature instability may vary the input voltage, incurring in a bit-flip and a Single Event Upset (SEU) [1]. At the best of our knowledge, this drawback is first revealed in this work.

To summarize the SA and DT performance comparison, Table II draws the performance trade-offs under temperature

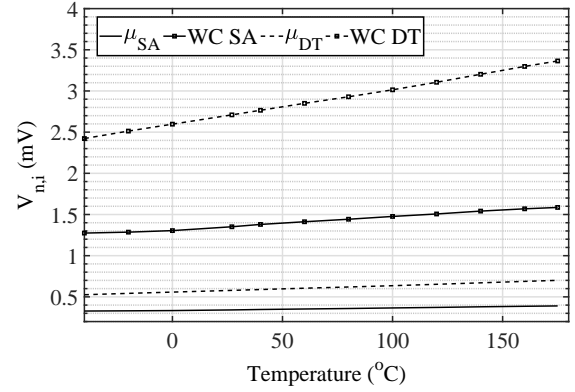


Fig. 9. A 151-points Monte Carlo post-layout simulation over a 11-points temperature sweep in a range from -40°C to 175°C for SA (solid line) and DT (dotted line) comparator input-referred noise mean and worst case (WC) (square marks).

variation. A linear fit of the presented post-layout simulations over a 11-point temperature sweep is done to determine a temperature coefficient for each SA and DT comparator characteristic. One may conclude that the DT comparator achieves a smaller offset in the expense of power consumption and noise. DT offset, and noise have a bigger temperature coefficient than SA. Both SA and DT comparator's delays are equally sensitive to temperature variation. At high temperatures, however, the variation of the comparators' characteristics may incur in a circuit failure. However, the DT comparator is found to be less reliable than the SA comparator at these temperatures.

TABLE II
PERFORMANCE COMPARISON OF COMPARATORS IN 180NM TECHNOLOGY AND 1.8V SUPPLY VOLTAGE

Performance	SA [5]	DT[6]
Total Delay/10 °C	63 ps	62.9 ps
$\sigma V_{OS,i-total}/10^{\circ}\text{C}$	4.88 μV	13.9 μV
$\sigma_{n,i} \sigma/10^{\circ}\text{C}$	4.1 μV	11.8 μV
$\sigma_{n,i} \mu/10^{\circ}\text{C}$	3.0 μV	8.0 μV
Average Power Consumption	0.35 mW	1.7 mW

C. Metastability Results

Fig. 10 depicts the probability for SA and DT comparators to enter the metastable zone. As expected, increasing temperature decreases time in regeneration phase, and the gain before the latch. The Probability Density Function (PDF) is shifted to lower clock frequencies according to (24). As expected, the probability for SA and DT comparators to enter the metastable zone rises to 1 with the increase of the clock frequency. According to (23), the estimated PDF error at 175°C is 10^{-13} for SA comparator, and 10^{-9} for DT comparator. For reliable operation up to 175°C , a maximum clock frequency of 100 MHz is assumed, which leads to a negligible probability for DT and SA comparators to enter the metastable zone, and a negligible probability of a bit-flip (i.e. negligible SEU).

Fig. 10 highlights that temperature effect shifts the PDF, reducing the maximum clock frequency. Fig. 10 also demonstrates that the transition from low to high probability is never

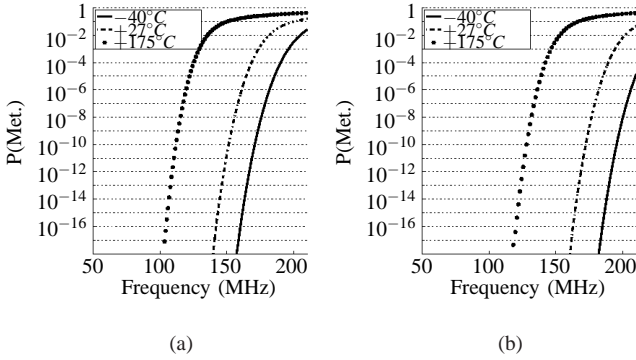


Fig. 10. Probability for (a) SA and (b) DT comparators to enter the metastable zone for temperatures of $-40\text{ }^{\circ}\text{C}$, $+27\text{ }^{\circ}\text{C}$, and $+175\text{ }^{\circ}\text{C}$; using ΔV_{in} in $\pm 450\text{mV}$ range.

instantaneous, and its slope does not depend on temperature. Fig. 10 suggests that temperature effect generating metastability could be topology independent. Thus, an appropriate technology choice would improve comparator performance in respect of metastability. Further investigations should be carried out to elucidate such characteristics using different process technologies. Such study is out of the scope of this proposal.

D. SAR ADC Results

The SAR ADCs under analysis are designed using the XH018 180 nm technology latched comparators. Fig. 11 illustrate the SAR ADC layout having a $243 \times 195\ \mu\text{m}^2$ footprint. From here on, the SAR using SA and DT are named SA-SAR and DT-SAR, respectively. Both versions have the same die area, since both latched comparators have a similar layout footprint. SAR transmission gates are designed according to the results presented in Sec. IV-A. The binary capacitive network is designed for a normalized $C = 106.8\ \text{fF}$, having a $195 \times 100\ \mu\text{m}^2$ layout footprint.

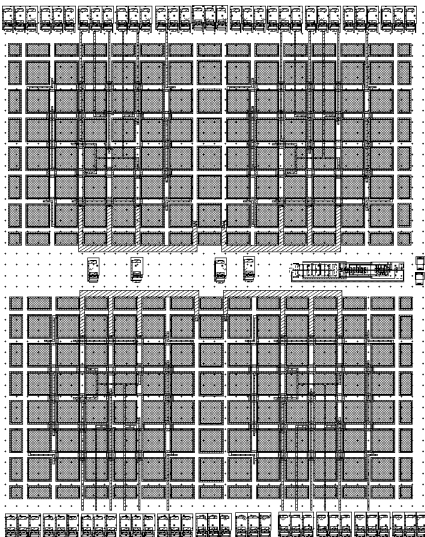


Fig. 11. SAR ADC layout with sizing of $243 \times 195\ \mu\text{m}^2$. Digital State Machine and metal interconnections are not presented for the sake of legibility.

The SAR ADC is post-layout simulated for a normalized input-voltage varying from -1 to $1\ \text{V}$ at $27\text{ }^{\circ}\text{C}$, with a clock frequency of $100\ \text{MHz}$. SAR outputs results are foreground calibrated from calibration weights computed using MatLab [23]. The resulting calibration weights are then applied to $-40\text{ }^{\circ}\text{C}$ and $175\text{ }^{\circ}\text{C}$ post-layout simulation results. This is a standard calibration technique for smart vehicle application. A common improvement would be applying a background calibration technique which continuously adjusts calibration weights over temperature. The following results have proved that background calibration is not required for this proposal. From these results, the differential non-linearity (DNL) and the integral nonlinearity (INL) are estimated.

Fig. 12(a) presents the SA-SAR DNL: $+0.5/-0.15\ \text{LSB}$ at $27\text{ }^{\circ}\text{C}$, $+0.33/-0.08\ \text{LSB}$ at $-40\text{ }^{\circ}\text{C}$, and $+0.77/-0.14\ \text{LSB}$ at $175\text{ }^{\circ}\text{C}$. Fig. 12(b) presents the DT-SAR DNL having: $+0.49/-0.16\ \text{LSB}$ at $27\text{ }^{\circ}\text{C}$, $+0.34/-0.08\ \text{LSB}$ at $-40\text{ }^{\circ}\text{C}$, and $+0.83/-0.16\ \text{LSB}$ at $175\text{ }^{\circ}\text{C}$. According to estimations found in Sec. IV-A, high-temperature operations increases R_{SW} of the transmission gates, which then increases SAR DNL. Similar behavior is found for both SA-SAR and DT-SAR.

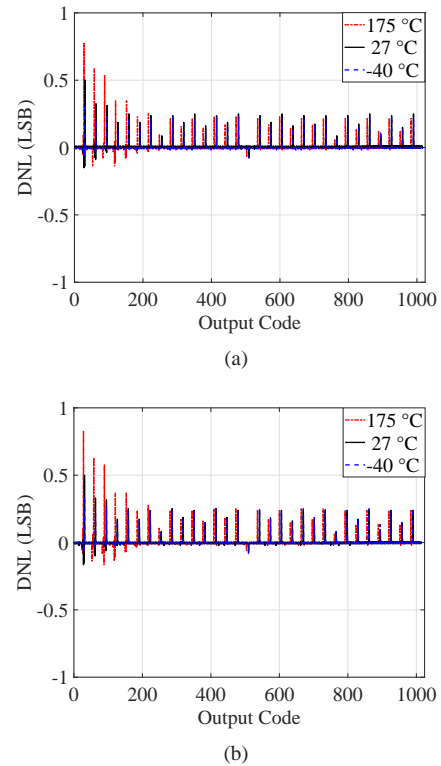


Fig. 12. Post-layout simulated DNL error for a temperature variation of $-40\text{ }^{\circ}\text{C}$ (dashed blue line), $27\text{ }^{\circ}\text{C}$ (continuous black line), and $175\text{ }^{\circ}\text{C}$ (dashed-dotted red line): (a) SA-SAR results, (b) DT-SAR results.

Fig. 13(a) presents the SA-SAR INL having: $+0.49/-0.5\ \text{LSB}$ at $27\text{ }^{\circ}\text{C}$, $+0.24/-0.21\ \text{LSB}$ at $-40\text{ }^{\circ}\text{C}$, and $+0.71/-0.48\ \text{LSB}$ at $175\text{ }^{\circ}\text{C}$. Fig. 13(b) presents the DT-SAR INL: $+0.48/-0.48\ \text{LSB}$ at $27\text{ }^{\circ}\text{C}$, $+0.47/-0.19\ \text{LSB}$ at $-40\text{ }^{\circ}\text{C}$, and $+0.71/-0.45\ \text{LSB}$ at $175\text{ }^{\circ}\text{C}$. INL results highlight an increasing non-linear error. Such non-linearities could not be calibrated using the calibration technique aforementioned [23]. For $175\text{ }^{\circ}\text{C}$, the drop-off in INL occurred at an output code of around 800,

about 100 before 27 °C. Between 27 °C and −40 °C, the difference was of around 50 in the output code. At the 1024 output, INL achieved values over 1 LSB for all temperatures, although this value was achieved for a much smaller output for the highest temperature. Thus, both SA-and DT-SAR SAR achieve an ENOB of 9.8 bits, which is reduced to 9.6 bits in high-temperature operation.

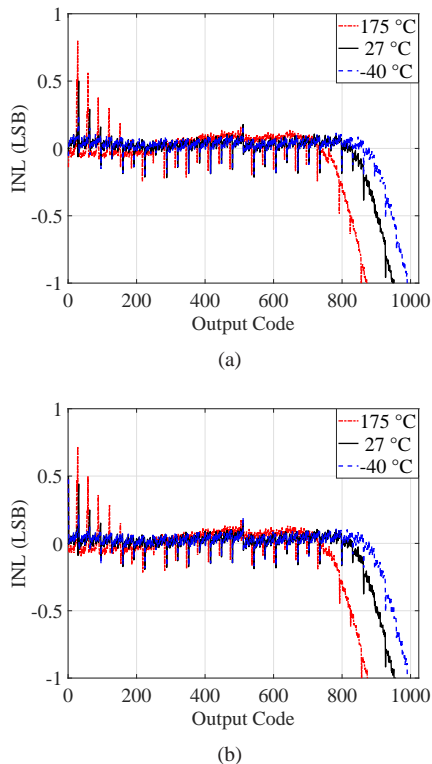


Fig. 13. Post-layout simulated INL error for a temperature variation of −40 °C (dashed blue line), 27 °C (continuous black line), and 175 °C (dashed-dotted red line): (a) SA-SAR results, (b) DT-SAR results.

V. CONCLUSIONS

This work highlights a temperature-aware analysis of performance variability in latched SA and DT comparators of previous work. This analysis is then extended to the metastability and performance metrics of a SAR ADC topology. Post-layout simulations validated the delay analysis, which demonstrated a high sensitivity to temperature variation, incurring in circuit failure at high temperatures. Offset voltage was found to be less sensitive to temperature, however, it is overcome by input-referred noise. As for the metastability, initial analysis showed that a clock frequency of 100 MHz is sufficiently immune to temperature variations to maintain an acceptable performance in the temperature range. For DNL and INL performance metrics, It is showed to be consistent in both SA and DT topologies, but still somewhat less performant, a difference of around 0.3 LSB at 175 °C is found. Both SA-and DT-SAR SAR achieve an ENOB of 9.8 bits, which is reduced to 9.6 bits in high-temperature operation. This work has found that the DT is less reliable than the SA, which is only avoidable by limiting the clock frequency (around 100 MHz). Once

calibrated and operated at a frequency where delay and offset effects are negligible and the probability of metastability is low. Thus, the performance reliability can be maintained in a wide temperature range. The results have also proved that background calibration is not required for this topology, and a foreground calibration is sufficient.

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