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Study and optimization of a 600V Pseudo-vertical GaN-on-silicon rectifier by finite element simulations

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Keywords: GaN rectifier, Finite Element Simulation, GaN on Silicon

Abstract. This work presents the impact analysis of physical and geometrical parameters on the on-resistance and the breakdown voltage in order to optimize a 600 V pseudo-vertical GaN/Si Schottky rectifier. The results by finite element simulations indicate that the most influent parameter on the resistance is the thickness of the n^+ layer. Regarding reverse specifications, simulations show that a good efficiency of the "Mesa + Guard Ring" is achieved for a guard ring doping concentration higher than $N_a=5\times10^{17}$ cm^{-3}.

Introduction

Real performance breakthroughs have been demonstrated for high voltage, high power, high temperature and high frequency devices by using wide band-gap semiconductors, such as 4H-SiC, GaN and AlGaN, over the previously existing devices based on group-IV and III-V lower band-gap semiconductor material [1]. One of the key devices for high power switching converter is a fast rectifier. 4H-SiC based Schottky diodes are now commercially available from many companies with breakdown voltage up to 1,7 kV. However, bulk SiC substrates are expensive and the hetero-epitaxial SiC layers on low cost substrates have many crystal defects. These are the main reasons for the on-going research programs toward GaN based-rectifiers on Silicon substrate for medium voltage range applications (600 V < V_{br} < 1.2 kV).

The insulating buffer between the Si substrate and GaN epilayer limits the rectifier architecture to a lateral structure. There exist two types of GaN based rectifier architectures. The first one derived from a High Electron Mobility Transistor (HEMT) structure where the gate becomes anode and the Drain/Source becomes cathode. If this architecture offers interesting prospects for low resistance devices due to the high mobility of the 2DEG electron gas at the AlGaN/GaN interface, the HEMT based rectifier suffer from many points of vulnerability like current collapse phenomenon [2], lag effect [3] and the lack of an efficient edge-termination [4].

Recent advances on the development of thick n-type GaN epilayers (slightly and highly Si doped) on Si substrate and on the deep GaN etching [5] offer new prospects for the development of a pseudo-vertical GaN rectifier architecture (see Fig. 1). The advantages of such device architecture are numerous. The use of pseudo-vertical design allows a significant reduction of the GaN Schottky diode on-resistance due to the vertical current conduction in the drift region under forward bias. Then, a vertical extension of the electric field in the drift region under reverse bias is expected with a good efficiency of the "mesa + guard ring" edge-termination [6]. This work presents the optimization of a pseudo-vertical GaN Schottky rectifier specifications by finite element simulations. Both geometrical and GaN doping parameters have been varied in order to decrease the on-state resistance and increase the breakdown voltage.

Device simulation description

The optimization of the pseudo-vertical structure have been achieved by finite element simulations using SYNOPSYS SENTAURUS™ software with a breakdown voltage target of V_{br} > 600 V.

Fig. 1 reports the schematic half cross-section view of the simulated device. The epitaxial configuration of this structure contains a n^+-GaN layer followed by a n-type doped GaN layer, both Si doped. The doping concentrations are $N_{d\text{-}n}=7.5\times10^{15}$ cm^{-3} and $N_{d\text{-}n+}=5\times10^{18}$ cm^{-3} for the n-layer and the n^+-layer, respectively. The doping level and the thickness (6 µm) of the n layer has been selected from analytical calculations and corresponds to the best R_{on}/V_{br} trade-off on a 1D vertical structure. On the contrary, the doping concentration of the n^+ layer has been selected in agreement with the actual state of the art of thick n^+-GaN layer growth on Si substrate.

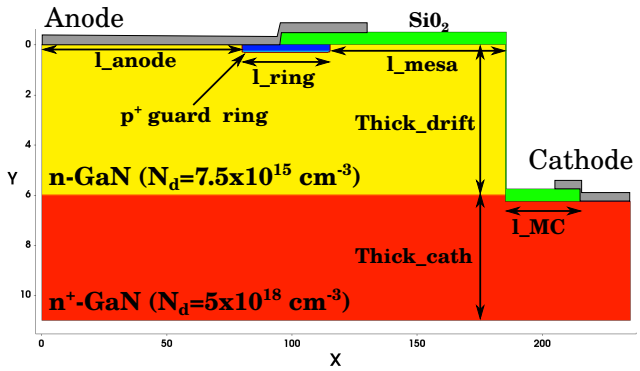

Fig. 1. Half cross-section view of the simulated pseudo-vertical GaN-on-Silicon Schottky rectifier.

An electrode and a p^+ guard ring edge termination compose the anode finger. The cathode is contacted via a deep mesa etching. The tuned parameters for the integrated specific on-resistance improvement are the anode lengh (*l_anode*), the n^+ layer thickness (*thick_cath*) and the spacing between the mesa edge and the cathode (*l_MC*). For the breakdown voltage improvement, the tuned parameters are the width and the doping level of the p^+ guard ring (*l_ring*, $N_{a\text{-}ring}$) and the spacing between the guard ring and the mesa edges (*l_mesa*).

All simulations have been performed with a Schottky barrier height and a specific ohmic contact resistance of Φ_b=1 eV [6] and $\rho_c = 10^{-5}$ Ω.cm^2 [7, 8], respectively. These parameters have been both collected from the literature and compared to values extracted on existing devices from our current project.

Results and discussion

Improvement of the integrated on-resistance. From all studied parameters, the most influent one is the n^+ layer thickness. As can be seen on Fig. 2, the rectifier resistance strongly decreases by increasing the n^+ layer thickness from R≈16 Ω.mm for *thick_cath* = 1 µm down to R ≈ 2.3 Ω.mm for *thick_cath* = 10 µm that corresponds to an average resistance reduction of 1.4 Ω.mm/µm (here µm corresponds to *thick_cath* increase). Then the average resistance gradient decrease to 0.03 Ω.mm/µm for 10 < *thick_cath* < 50 µm. This behavior demonstrates that below a minimum value of the n^+ layer thickness, here *thick_cath*=10 µm, the rectifier resistance mainly comes from the n^+ layer sheet resistance. Moreover, if the resistance of the n^+ layer is too high, a strong debiasing of the n^+ layer occurs below the Schottky contact (0 < X < *l_anode*) that leads to a bad verticalization of the structure.

This behavior is well illustrated on Fig. 3, which displays the evolution of the normalized current density in the drift layer at Y=0.5 µm (see Fig. 1) for V_{ak}=1.5 V and various n^+ layer thicknesses. Basically, the current density in the n layer along the X axis can be written, as follows:

$$J_{drift}(x) = \frac{[V_a - V_{drift}(x)]}{R_{drift} \times l_anode} \quad (1)$$

with V_a the potential below the Schottky contact, V_{drift} the potential of the bottom side of the n layer and R_{drift} the resistance of the n layer. Since V_a is constant for 0 < X < *l_anode*, the evolution of the current density along the X-axis is also the image of the potential at the bottom side of the drift layer.

One can see on Fig. 3 that for *thick_cath* = 40 µm the normalized current density is higher than J_{drift} = 0.85 for the whole contact area while for *thick_cath* = 2 µm, a normalized current density higher than J_{drift} = 0.5 is only observed for l_anode-X < 25 µm. This observation demonstrates that for one specific n^+ layer configuration, it exists an optimal *l_anode* value for limiting the integrated on-resistance value.

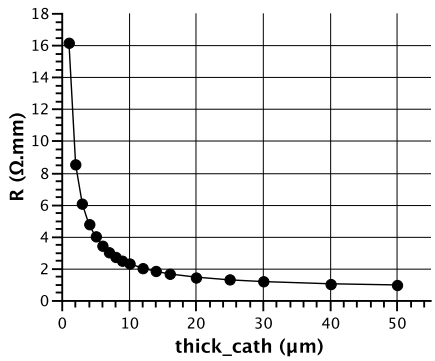

Fig. 2. Simulated rectifier resistance as a function of *thich_cath*.

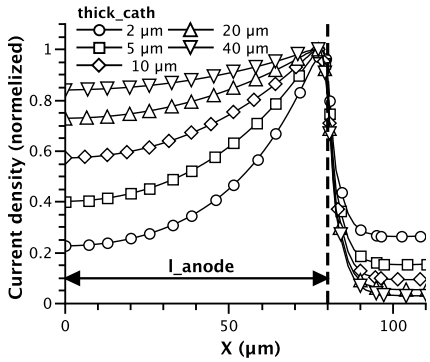

Fig. 3. Evolution of the current density at V_{ak}=1.5 V at 0.5 µm below anode contact for different *thick_cath* values.

Fig. 4-a displays the evolution of the resistance and the integrated specific on-resistance of the diode as a function of the Schottky contact length (*l_anode*) for *thick_cath* = 2, 5 and 10 µm. For all *thick_cath* configurations, the resistance value decreases by increasing *l_anode* value. However, the resistance gradient is higher for small *l_anode* length. This behavior leads to a minimum integrated on-resistance value with an optimal contact length. This optimal anode length increases with the n^+ layer thickness. Thus, minimum specific on resistance values of $R_{on\text{-}min}$ = {16.3, 8.4, 5.3} mΩ.cm^2 are observed for *thick_cath* = {2, 5, 10} µm and *l_anode* = {20, 40, 60} µm.

Fig. 4-b exhibits the evolution of the resistance and the integrated specific on-resistance of the diode as a function of the spacing between mesa edge and cathode contact (*l_MC*) for 3 n^+ layer thicknesses. As expected, R and R_{on} behaviors both increase linearly with increasing *l_MC* and the influence of *l_MC* on R and R_{on} is lower for a thick n^+ layer.

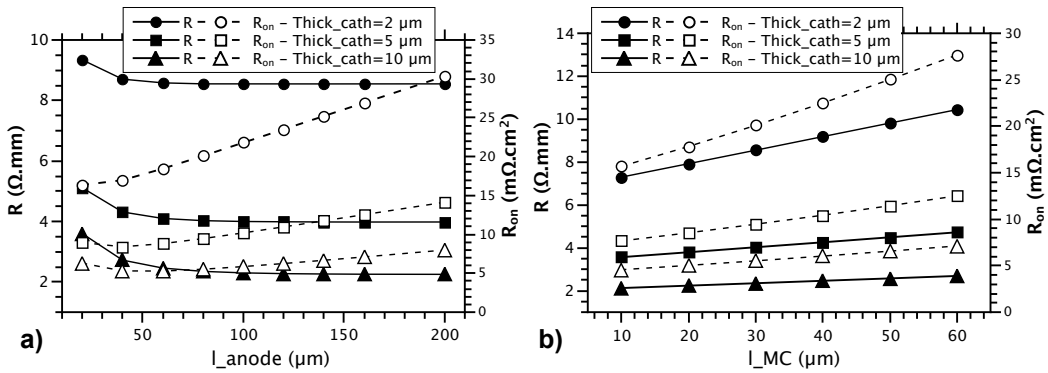

Fig. 1. Simulated resistivity (R) and specific on-resistance (R_{on}) as a function of a) *l_anode*, b) *l_MC*.

From a theoretical point of view, the pseudo-vertical GaN/Si structure offers interesting prospects for the fabrication of a high power density fast rectifier. Unfortunately, the stress induced by high Si doping epitaxy limits the maximum n^+ layer thickness to 2-3 µm. This limitation makes GaN/Si pseudo-vertical rectifier not competitive face to 4H-SiC rectifier.

Improvement of the breakdown voltage. The most influent parameter for breakdown voltage improvement is the guard ring doping concentration (GRDC). One can see on Fig. 5-a that for low GRDC, the breakdown voltage is V_{br}=755 V and corresponds to the value for a "mesa only" edge termination. This value agrees with the breakdown voltage measured on similar rectifier architecture with resistive guard ring by Alquier *et al.* [6]. Then by increasing the GRDC to $N_a=6\times10^{17}$ cm^{-3}, the breakdown voltage reaches V_{br}=1590 V and keeps constant up to $N_a=4\times10^{18}$ cm^{-3}. Finally, the breakdown voltage decreases for higher GRDC. This behavior is explained by the evolution of the electric field below the guard ring (Fig 5-b). For small GRDC, the electric field is not well stretched along the periphery and thus increases inside the guard ring. On the contrary, for medium GRDC the electric field keeps constant below the guard ring. For high GRDC, the guard ring has less and less efficiency and the periphery protection relies only on the field plate.

The large process window in term of GRDC is promising for the realization of an efficient edge termination for GaN power devices even if improvement on the activation of implanted Mg elements is needed [9].

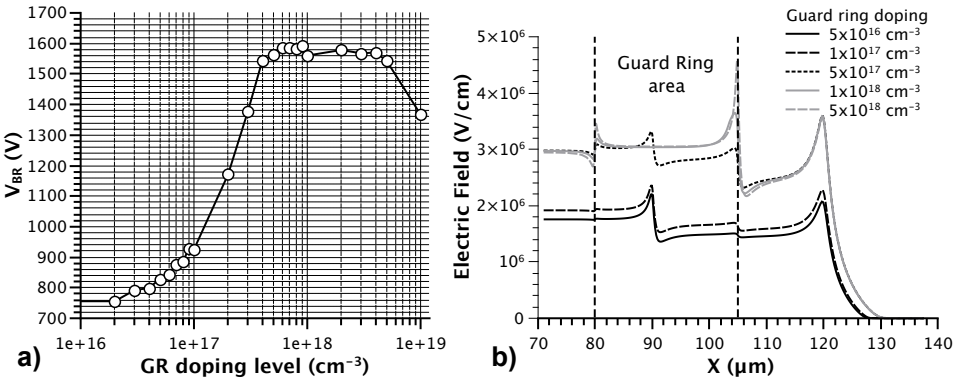

Fig. 5 a) Simulated breakdown voltage as a function of the guard ring doping concentration – b) Evolution of the electric field at Y= 0.6 µm for different guard ring doping concentrations

Summary

The behavior of the GaN pseudo-vertical Schottky diode protected by one p^+ guard ring and mesa etching has been studied using 2D simulations. The influence of the geometrical and physical parameters on the specific on-resistance and on the breakdown voltage has been analysed.

The advantage of the pseudo-vertical architecture is the possibility to get an efficient edge-termination for GRDC higher than $N_a=6\times10^{17}$ cm^{-3}. However, the main drawback is the need of a thick (> 10 µm) n^+ layer to reach low enough specific on-resistance. Unfortunately, the thickness of the n^+ layer is limited to 2-3 µm due to the stress induced by the high doping concentration. As a results, it appears that the pseudo-vertical GaN rectifiers is not competitive face to 4H-SiC Schottky rectifier (Ron ~ 1mΩ.cm^2) at the actual state of the art of the GaN epitaxy technology.

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