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Two-stage unbuffered CFA based non-inverting resistive-feedback amplifier: a study based on the description of the operational transconductance conveyor (OTC).

H. Barthélemy, R. Vauché, V. Giès, S. Bourdel, J. Gaubert

Abstract

A study of the non-inverting amplifier based on a two stages CMOS unbuffered *current-feedback-amplifier* (UCFOA) is proposed in this paper. Using a small-signal equivalent circuit (macro-model) of the non-inverting amplifier, a theoretical explanation of the closed loop gain is given. The opamp phase margin and its bandwidth have been estimated from the quality factor Q of resonance and using a novel description of the UCFOA input stage called *Operational Transconductance Conveyor* (OTC). The OTC description can be viewed as an extension of type II second generation current conveyors. Based on the fundamental parameters of the proposed OTC, a theoretical approach given in this paper explains how to evaluate precisely the value of the UCFOA compensation capacitance. PSPICE was used to simulate both the theoretical macro-model and the CMOS configuration from a $0.35\mu\text{m}$ typical BSIM3V3 transistor models.

Index Terms — opamp, current feedback amplifier, transconductance amplifier, diamond transistor, current conveyor

1. INTRODUCTION

Since the discovery of the negative feedback amplifier by HS Black [1,2], a few number of feedback amplifier topologies arose from industry. This is due to the fact that these topologies are synthesized from the Voltage Controlled Current Sources (VCCS) which can be electrically simulated, historically by

vacuum tubes and more recently by Bipolar Junction Transistors (BJT) or Metal Oxide Semiconductor (MOS) transistors. Today, two main types of voltage output operational amplifiers are available on the market: *i)* Voltage Feedback Operational Amplifier (VFOA) [3,4] and *ii)* Current Feedback Operational Amplifier (CFOA) [5-8]. The first sold VFOA was the K2-W operational amplifier produced in 1952 [2] and the concept of the current-feedback was introduced around 1942 [9], while the first silicon integrated CFOA topology was probably firstly suggested by D. J. Hamilton in 1964 [10]. The first commercial silicon CFOA called CLC103, was produced by Comlinear corporation in 1982 [11], 20 years after the first commercial silicon VFOA developed by Wildlar and Talbert [4]. The CFOA and the VFOA provide both a voltage type output. However, when their output voltage amplifier (output voltage buffer) is not implemented, they are called unbuffered VFOA (UVFOA) and unbuffered CFOA (UCFOA) and provide both a current type output (*high output impedance*).

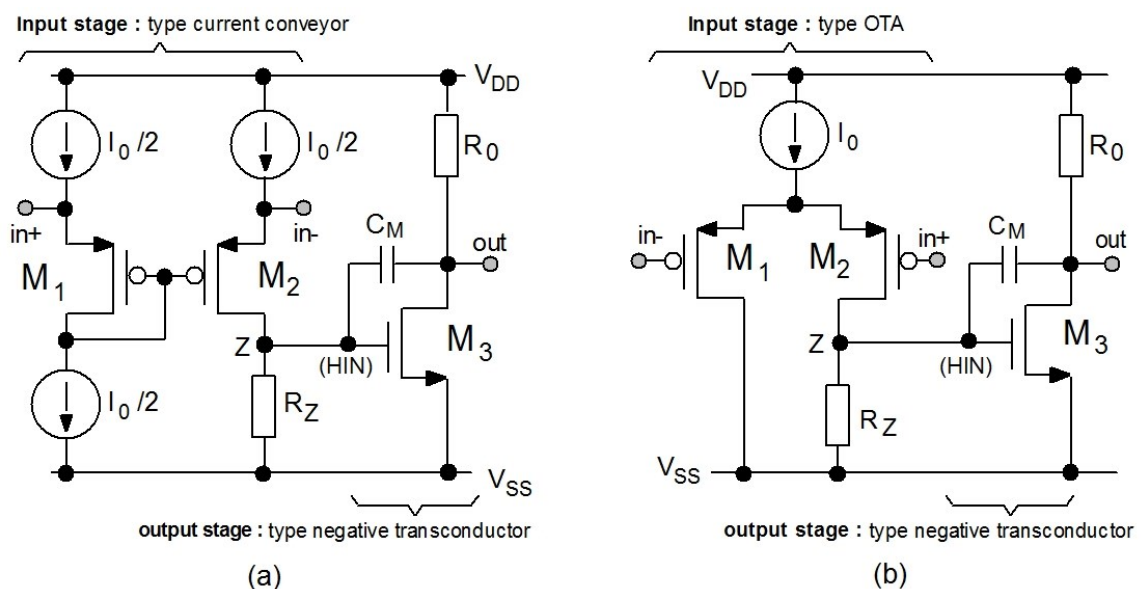


Fig.1. Typical two stages UVFOA and UCFOA CMOS topologies: **(a)** UVFOA : two stage CMOS Miller OTA (ref. [16] with $C_M=0$) **(b)** UCFOA two stage current mode operational amplifier.

Since the emergence of the CMOS technology, most of loading impedances are capacitive. In this case, the unbuffered operational amplifier could also provide a higher DC open loop gain voltage. For this reason, most analog IC designers use unbuffered feedback operational amplifiers [12] instead of classical output voltage operational amplifiers. The Unbuffered VFOA (UVFOA) can be considered as an Operational Transconductance Amplifier (OTA) since its input impedances are high [13-15]. However, the Unbuffered CFOA (UCFOA) can only be considered as a non-ideal OTA since its negative input node does not provide a high input impedance [6-8]. Thus, use of the OTA acronym for UCFOA can create a misunderstanding. For this reason, the term “Operational Transconductance Conveyor” (OTC) is used in this paper to describe the UCFOA topologies. This proposed Operational

Transconductance Conveyor (OTC) is also an extension of the type II current conveyors and that it will be useful in analog signal processing. Here, using VFOA, CFOA, OTA and OTC acronyms, Table I summarizes the input and output types for the four operational amplifiers previously discussed.

TABLE I
Mains opamps topologies
(I : CURRENT TYPE V: VOLTAGE TYPE)

Opamps	Inputs		Output (out)
	(in+)	(in-)	
<i>Voltage output types</i>			
VFOA	V	V	V
CFOA	V	I	V
<i>Current output types (unbuffered opamps)</i>			
OTA	V	V	I
OTC	V	I	I

Part (a) of Fig. 1 shows a typical CMOS configuration of a two-stage Miller OTC (two-stage UCFOA) which is used in [16] to implement a high frequency gyrator. This circuit is part of the CFOA family since the node $in-$ is not voltage buffered and also, it exists an AC current flowing through the node $in-$ and the source of M_2 . Part (b) of Fig. 1 shows the CMOS classical two-stage Miller OTA (two-stage UVFOA) using a traditional pair of two transistors (M_1 and M_2). This circuit is part of the VFOA family since the nodes $in+$ and $in-$ are connected to MOS gates. For both of them, the node Z is a High Impedance Node (HIN) which allows an operational amplifier with high transconductance gain to be achieved thanks to the second stage.

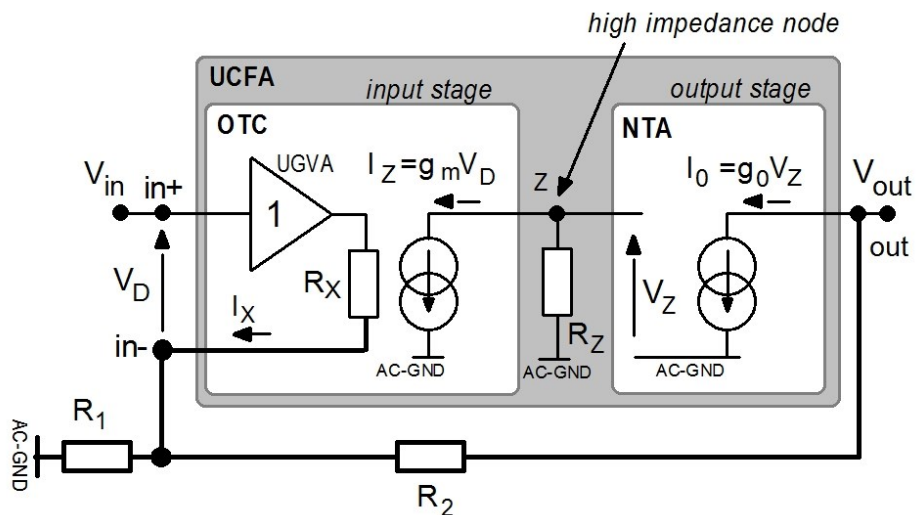


Fig. 2. Electrical description of the two stages unbuffered current feedback amplifier (Ideal UCFOA for $R_x=0$ and $R_z \rightarrow \infty$), the Miller capacitance is not represented.

The purpose of this paper introduces a general approach to study a non-inverting amplifier based on two-stage UCFOA for which the topology is shown in Fig. 2. The study proposed here will differ from traditional ones because the opamp output is not voltage buffered. The circuit is composed of an input

stage (OTC), a high impedance R_z at node Z (HIN), and a single output voltage controlled current source called here Negative Transconductance Amplifier (NTA). In this representation, the node $in+$ of the UCFOA is voltage buffered by a Unit Gain Voltage Amplifier (UGVA). Moreover, the node AC-GND is supplied at the DC common mode-voltage of the operational amplifier. This common mode voltage is generally chosen to obtain the maximum dynamic for output voltage. This leads to set V_{AC-GND} to $(V_{DD}+V_{SS})/2$ where V_{DD} and V_{SS} are respectively the positive and negative supply voltages of the operational amplifier. Then V_{AC-GND} is equal to $V_{DD}/2$ (resp. 0V) when V_{SS} is set to 0V (resp. $-V_{DD}$). Finally, an ideal UCFOA is obtained when R_x is null and R_z infinite.

In section II, a discussion about the OTC is given. Using as a case study, a two-stage Miller OTC is presented and simulated in section III. In section IV, a theoretical analysis of the non-inverting amplifier is proposed. This analysis and theory are based on the proposed equivalent macro-model of the CMOS configuration using small-signals. Simulation results, discussions, and comparison with theory are given in section V before the conclusion in section VI.

2. OPERATIONAL TRANSCONDUCTANCE CONVEYOR

In Fig.2, when the current ratio $|I_z/I_x|=1$, the OTC can be designed from different popular active elements like the 2nd generation Current Conveyor (CCII) [17], the 2nd generation current-controlled current conveyor (CCCII) [18] or the diamond transistor [6,8] for examples. Using the OTC description allows us to consider all possible topologies in terms of current gain (I_z/I_x), i.e. equal or different than 1, in conjunction with different values of the equivalent resistance R_x . Using a proposed symbol for the OTC (input stage) and the NTA symbol (output stage) as ideal active elements, Fig.3a shows the non-inverting amplifier configuration.

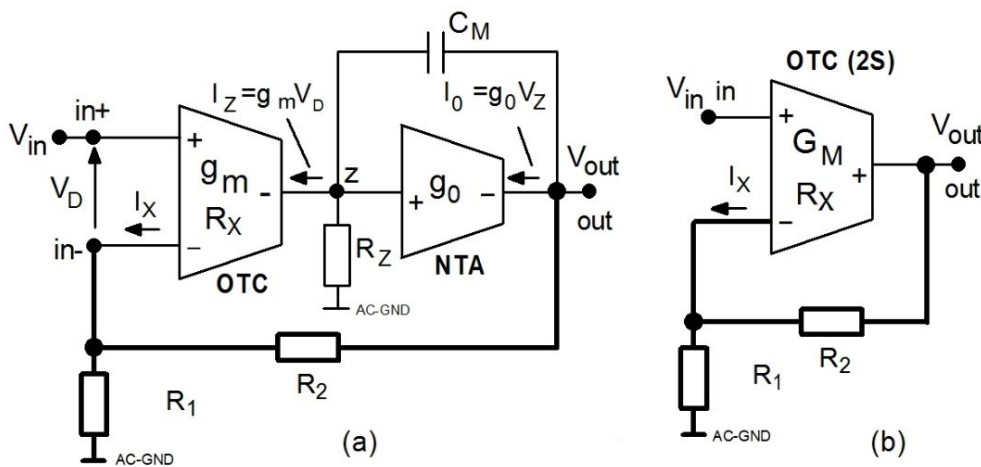


Fig. 3. Two-stage Miller UCFOA based non-inverting amplifier **(a)** Equivalent circuit using a one-stage OTC as input stage and NTA as output stage **(b)** equivalent circuit based on a two stages high G_M OTC (Miller OTC).

Equation (1) shows that the two-stage OTC has the same order of magnitude than a classical two-stage Miller OTA. Its transconductance gain G_M which is given by:

$$G_M = g_0 \cdot g_m \cdot R_Z \quad (1)$$

has the same order of magnitude than a classical two-stage Miller OTA. From Fig. 2, the following formula of I_X :

$$I_X = V_D / R_X \quad (2)$$

and I_Z :

$$I_Z = g_m V_D \quad (3)$$

can be obtained. By defining a parameter α equals to the current gain between I_X and I_Z as follows:

$$\frac{I_Z}{I_X} = \alpha \quad (4)$$

the parameter α can be expressed from (2) and (3) as a function of g_m and R_X which gives:

$$\alpha = g_m \cdot R_X \quad (5)$$

Table II gives some examples of correspondences with popular active elements according to R_X and α values. As mentioned previously, the OTC also offers the great advantage of taking into account every R_X and current gain α compared for example with CCII [6,17,18], or diamond transistor [6]. Thus, in the same way that an OTA is a universal active element which permits to describe the VFOA input stage, an OTC permits to describe all CFOA input stage.

TABLE II
OTC example of correspondences for $|\alpha|=1$ and $|\alpha|>1$

α	R_X	g_m	
-1	0	∞	OTC = CCII+ [17]
+1	0	∞	OTC = CCII- [17]
-1	$R_X > 0$	$ \alpha /R_X$	OTC = CCCII+ [18] (diamond transistor [8])
+1	$R_X > 0$	α/R_X	OTC = CCCII- [18]
<0	$R_X > 0$	$ \alpha /R_X$	OTC (positive output)
>0	$R_X > 0$	α/R_X	OTC (negative output)

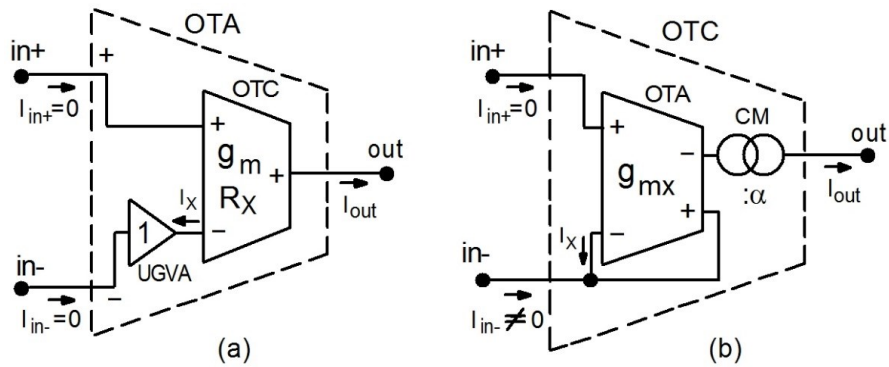


Fig.4. Example of: **(a)** OTC based OTA and UGVA **(b)** OTA based OTC and CM (Current Mirror).

To underline the difference between the OTA and the OTC, an OTA configured with an internal OTC, and an OTC configured with an internal OTA are respectively shown in part (a) and (b) of Fig. 4. It is possible to observe that in part (a) of Fig. 4, the OTA transconductance g_m is the same than the internal OTC, whereas in part (b) of Fig. 4, the OTC transconductance gain g_m is given by $g_m = |\alpha| \cdot g_{mx}$ where α is the gain of the current Mirror (CM) and it is the same coefficient α used to define the OTC. The commercial CFOA [6-8] exhibit very low R_x in BJT technologies compared to CMOS technologies operating at low-power. Consequently, the stability condition could differ in CMOS applications since it is not possible to always consider R_x very low [6-8].

3. STUDY OF A TWO-STAGE CMOS MILLER OTC

To illustrate the configuration shown in Fig.2 (or Fig.3), a CMOS Miller OTC loaded by the C_L capacitance is shown in Fig.5. Note that a class AB equivalent output could be constructed by designing an additional high impedance node at the drain of M_2 [16]. All simulation was performed for $V_{DD} = -V_{SS} = 1.5V$.

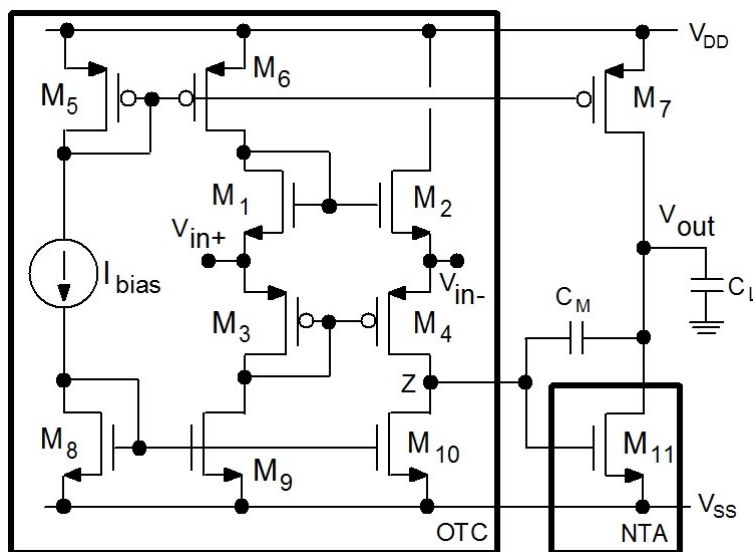


Fig.5. A CMOS two-stage Miller OTC.

In Fig.5 M_1 to M_{10} (except M_7) simulate the OTC input stage (nodes $in+$, $in-$ and Z) and M_{11} (biased by M_7) simulates the NTA (node Z and out). By considering M_1 identical to M_2 , M_3 and M_4 , their respective transconductance gain g_{m1} , g_{m2} , g_{m3} , and g_{m4} are identical for a given temperature. At a small-signal amplitude and a low frequency of operation, the AC source-drain current of M_4 is half of the AC current I_x passing through the node $in-$ [18]. Consequently, the corresponding value of α is $\alpha=+0.5$ for this topology.

Table III summarizes the MOS transistor size used for all the PSPICE-BSIM simulations of the circuit in Fig.5 [19]. In Table III, an estimation of the drain and source areas (AD, AS) and perimeters (PD,PS) permits to take into account the MOS junction capacitance effects [20]. The transistor sizes proposed here have been fixed to provide similar transconductance and power consumption than the low power CMOS Miller OTA studied in [21].

TABLE III
Transistors sizes and equivalent drain and source areas (AD, AS) and perimeters (PD, PS) [16].

Transistors	W (μm)	L (μm)	AD=AS (m^2)	PD=PS (m)
M_1, M_2	108	1.5	189E-12	110E-6
M_3, M_4	54	1.5	94E-12	56E-6
$M_5, M_6, M_8, M_9, M_{10}$	15	1.5	26E6-12	17E-6
M_7	237	1.5	415E-12	240E-6
M_{11}	154	1.5	270E-12	157E-6

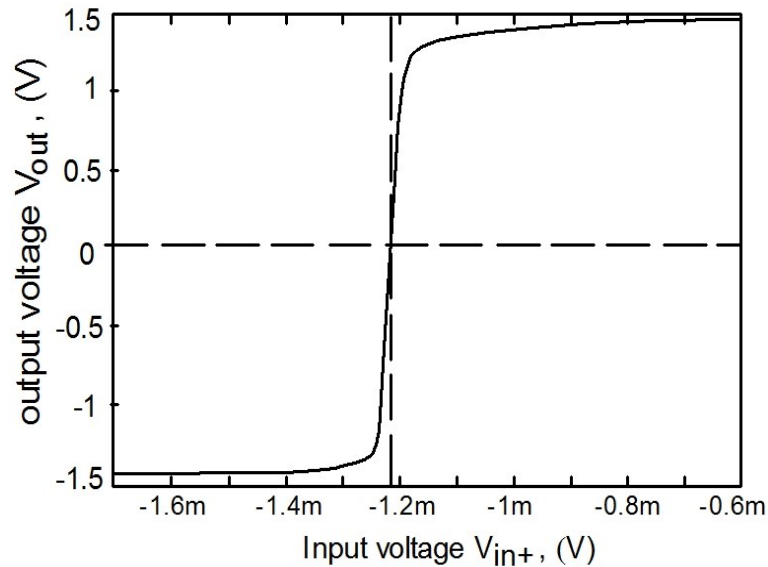


Fig.6. DC characteristics of the two stages Miller OTC in Fig.8, $V_{in-}=0V$.

TABLE IV

Main PSPICE simulated characteristics of the Two Stage Miller OTC in Fig.5
for $V_{DD}=-V_{SS}=1.5V$, $I_{BIAS}=17\mu A$.

Parameters	value	Units
A_{OPL}	58 000	[V/V]
THD% (out- 600mVpp)	6.2	%
TRMC (dB)	50.3	dB
G_M	632	$[m\Omega^{-1}]$
V_{OFF} @ in+ ($V_{in-}=0$)	-1.2	[mV]
GBW ⁽¹⁾ ($G_0=1$) ($V_{out}=V_{in-}$) $C_M=50fF$	94	[MHz]
Z_{IN+}	565k Ω //0.7pF	
Z_{IN-}	$R_X=1829.6$	$[\Omega]$
Total power supply	988	$[\mu W]$

(1) C_M is fixed to have no overshoot.

The simulated DC differential characteristic of the operational amplifier is shown in Fig. 6 for $V_{in-}=0$ and Table IV summarizes the main simulated performances (at this stage C_M was fixed here from simulation only. The DC input offset of -1.2mV seen in Fig. 6, which is high compared with a classical operational amplifier based on the traditional differential pair of two transistors [14], is mainly due to the diodes made by the transistors M_1 and M_3 since their drain are connected to their gate. In Table IV, A_{OPL} is the operational amplifier DC open-loop voltage gain and can be written as follows:

$$A_{OPL} = g_0 \cdot g_m \cdot R_Z \cdot R_0 = G_M \cdot R_0 \quad (6)$$

where R_0 is the equivalent output resistance of the operational amplifier, which is approximately equals to the parallel association of drain-source resistors R_{DS} of M_7 and M_{11} . AOPL is the open loop voltage gain when not output current occurs, which will not be the case of the unbuffered opamp in Fig.3.

4. THEORETICAL ANALYSIS OF THE NON-INVERTING AMPLIFIER CONFIGURATION

This section presents a theoretical analysis of the non-inverting amplifier using a two-stage Miller OTC (UCFOA). The objective of this section is to present a versatile opamp macro-model and its associated theory. We also aim at being able to estimate the value of the compensation capacitance C_M for a wanted phase margin and to demonstrate that " R_X " and " α " are the keys design parameters. The non-inverting amplifier configuration is kept in the part (a) of Fig.7 while the part (b) of Fig.7 shows the proposed equivalent macro-model of the non-inverting amplifier. This proposed macro-model takes

into account the main parasitic elements that appear when the OTC presented in the previous section is designed in CMOS technologies.

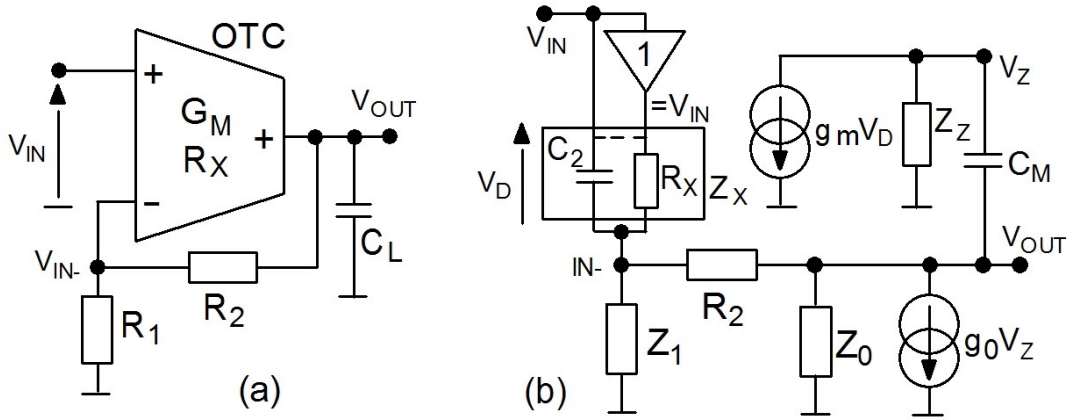


Fig.7. OTC based Non-inverting amplifier **(a)** Circuit **(b)** Proposed equivalent macro-model including the main parasitic elements of the circuits in Fig.8.

The impedances of the OTC macro-model in Fig.7b are defined as follows:

$$Z_X \cong R_X // C_2 s \quad (7)$$

$$Z_Z = R_Z // C_Z s \quad (8)$$

$$Z_1 = R_1 // C_1 s \quad (9)$$

$$Z_0 = R_0 // C_0 s \quad (10)$$

where Z_0 is the equivalent output impedance of the NTA.

Table V gives the correspondences between the macro-model and the transistors small-signal parameters. Parameters of the macro-model has been extracted from the PSPICE “.AC” simulation of the CMOS configuration around the DC operating point which is fixed in our case by the DC bias current I_{bias} and the voltage supplies V_{DD} and V_{SS} ($I_{bias}=17\mu A$). Expressions of R_Z and C_Z consider that the voltage variations at node *in-* in Fig.5 are very small regarding the voltage variations at node Z (high impedance node). For a transistor M_i , R_{DSi} is the output resistance, g_{mi} is the gate-source transconductance, C_{DBi} and C_{GSi} are respectively the drain-bulk and gate-source equivalent capacitances.

Note that the parasitic resistance in parallel with R_1 has been neglected and we assume that the effect of the time constant ‘ $R_X C_2$ ’ and ‘ $R_1 C_1$ ’ are far outside the frequencies of operation. Based on these considerations and after analytical calculation, the voltage transfer function (*closed-loop voltage gain*) is given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_0 \frac{(1-t_0s)}{(1+t_Zs)(1+t_{02}s)}}{1 + A_0 \frac{(1-t_0s)}{(1+t_Zs)(1+t_{02}s)} \frac{1}{K_0} (1+t_Xs)} \quad (11)$$

where:

$$K_0 = 1 + \frac{R_2}{R_1} \quad (12)$$

$$t_0 = \frac{C_M}{g_0} \quad (13)$$

$$t_{02} = R_{02}(C_M + C_0) \quad (14)$$

$$t_X = \frac{(R_2 + K_0 R_X) \cdot C_M}{\alpha} \quad (15)$$

$$t_Z = R_Z(C_M + C_Z) \quad (16)$$

$$A_0 = \frac{\alpha g_0 R_{02} R_Z}{([R_2 / K_0] + R_X)} \quad (17)$$

and:

$$R_{02} = (R_0 // R_2) = \frac{R_0 R_2}{R_0 + R_2} \quad (18)$$

The analytical calculations given above have been performed considering the following conditions:

- R_X is non zero
- $R_1 / D \ll 1$ and $[R_1 R_X / (D R_2)] \ll 1$ with $D = R_1 R_2 + R_X [R_1 + R_2]$

In (11) A_0 is the DC open loop gain and is different to the DC open-loop gain of the opamp A_{OPL} given in equation (6) because the resistive feedback consumes a current that could not be neglected. Since the time constant $t_0 = C_M / g_0$ appears at very high frequency, the expression of V_{OUT} / V_{IN} can be reduced to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{K_{OR}}{1 + [\frac{K_0}{A_0} (t_{02} + t_Z) + t_X]s + \frac{K_0}{A_0} t_{02} t_Z s^2} \quad (19)$$

where

$$K_{OR} = A_0 / [1 + \frac{A_0}{K_0}]_{A_0 \rightarrow \infty} = K_0 \quad (20)$$

Here, K_{OR} is the effective DC gain of the transfer function and $K_0 = 1 + (R_2 / R_1)$ is the ideal DC gain when A_0 tends to infinity. Equation (19) shows that the non-inverting amplifier operates like a second order low-pass frequency filter for which the Q factor of resonance can be used as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{K_{OR}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}} = \frac{K_{OR}}{1 + \frac{jf}{f_1} - \frac{f^2}{f_0^2}} \quad (21)$$

with:

$$Q = \frac{f_1}{f_0} = \frac{\sqrt{A_0 K_0 t_{02} t_Z}}{K_0 (t_{02} + t_Z) + A_0 t_x} \quad (22a)$$

or

$$Q(C_M) = \frac{\sqrt{A_0 K_0 R_{02} R_Z (C_M + C_0) C_M}}{\alpha [K_0 (R_{02} + R_Z) + A_0 (R_2 + K_0 R_X)] C_M + \alpha K_0 (R_{02} C_0 + R_Z C_Z)} \quad (22b)$$

$$f_1 \approx \frac{1}{2\pi} \frac{A_0}{K_0 (t_{02} + t_Z) + A_0 t_x} \quad (23)$$

and:

$$f_0 \approx \frac{1}{2\pi} \sqrt{\frac{A_0}{K_0 t_{02} t_Z}} \quad (24)$$

The phase margin (Φ_M) of the effective open-loop gain can then be calculated [22], we have:

$$\phi_M = \tan^{-1} \left[\frac{\sqrt{2}}{\sqrt{\sqrt{1+4Q^2} - 1}} \right] \quad (25)$$

or

$$\phi_M = \tan^{-1} \left[\frac{\sqrt{2}}{\sqrt{\sqrt{1 + \frac{4A_0 K_0 t_{02} t_Z}{[K_0 (t_{02} + t_Z) + A_0 t_x]^2}} - 1}} \right] \quad (26)$$

Equations (22) and (26) allow to estimate the resonance factor and the phase margin. Note that equation (26) shows that the phase margin (ϕ_M) is function of A_0 and not of not A_{OPL}

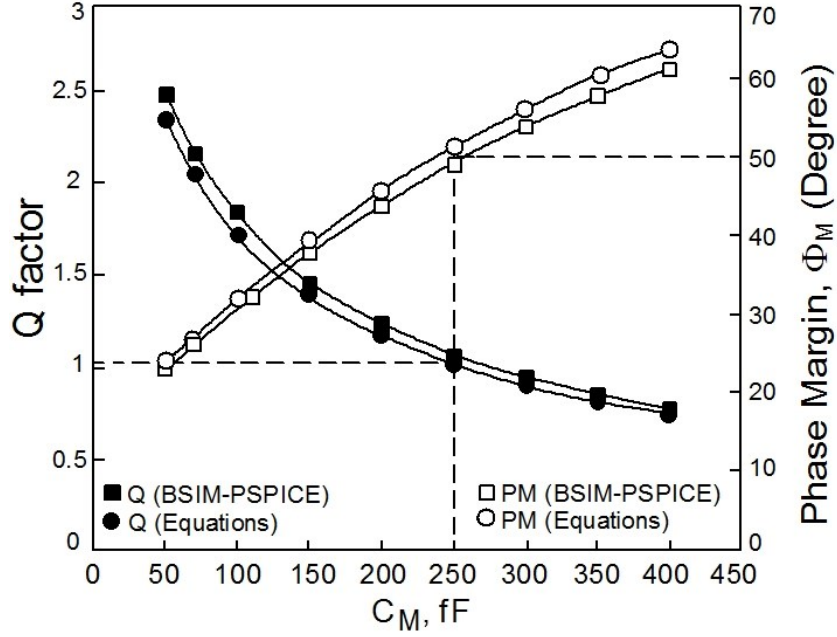


Fig.8. Phase margin and Q factor versus C_M in case of $G_0=6$. $R_2=5k\Omega$, $R_1=1k\Omega$ from BSIM 3V3 simulation and from calculation.

5. SIMULATIONS RESULTS AND DISCUSSIONS

Most of parameters can be deduced from simulation at the resonance frequency. For this reason, simulations at Q higher than $1/\sqrt{2}$ help to validate the theoretical approach since the resonance exists and is visible. From PSPICE simulations (macro-model or CMOS-BSIM), the Q factor has been obtained from a coefficient m at the frequency of resonance by solving [22]:

$$4mQ^4 - 4Q^2 + 1 = 0 \quad (27)$$

with:

$$m = \left(\frac{K_{OR}}{K_{MAX}} \right)^2 \quad (28)$$

where K_{MAX} is the maximum voltage gain at the resonance frequency f_R , and K_{OR} the simulated DC effective closed loop voltage gain. When Q is higher than $1/\sqrt{2}$, the relation between f_R and f_0 is given by [22]:

$$f_R = f_0 \sqrt{1 - \frac{1}{2Q^2}} \quad (29)$$

and the -3dB bandwidth by:

$$f_C = \sqrt{\frac{(2Q^2 - 1) + \sqrt{8Q^4 - 4Q^2 + 1}}{2Q^2}} f_0 \quad (30)$$

TABLE V

Equivalence between the macro-model, C_L and the transistor small-signal parameters obtained from PSPICE (Fig.5),

$$V_{DD} = -V_{SS} = 1.5V, I_{BIAS} = 17\mu A.$$

R_X	$(g_{m2} + g_{m4})^{-1}$	1829 Ω
R_Z	$R_{DS4} // R_{DS10}$	1110 k Ω
R_0	$R_{DS7} // R_{DS11}$	92.6 k Ω
g_0	g_{m11}	$2.65e-3 \Omega^{-1}$
C_Z	$C_{DB4} + C_{DB10} + C_{GS11}$	1.05 pF
C_0	$C_{DB7} + C_{DB11} + C_L$	10.8 pF
α	I_z / I_x	0.39
G_M	$G_M \cong g_0 \cdot g_m \cdot R_Z$	632 m Ω^{-1}

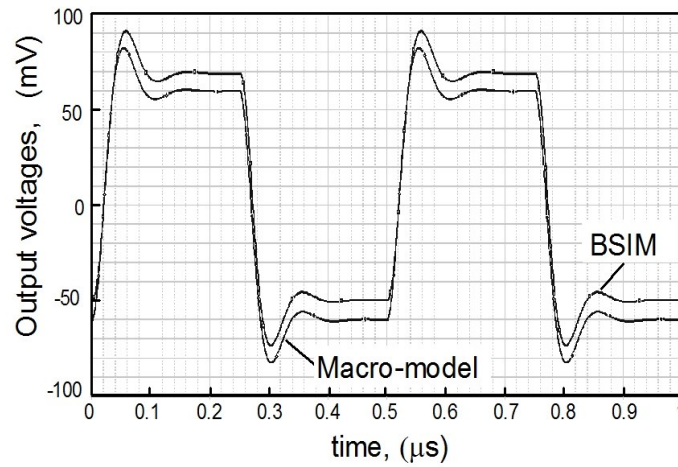


Fig.9. Transient output response of the non-inverting OTC with a 2MHz, 20mV peak-to-peak input pulse voltage at node in+, $G_0=6$, $R_2=5k\Omega$, $R_1=1k\Omega$, $C_M=250fF$, $Q \sim 1$.

Fig.8 shows the equivalent Q factor and phase margin versus the capacitor C_M obtained from the presented theory and from simulation of the CMOS configurations in Fig.5 when $R_2=5k\Omega$ and $R_1=1k\Omega$ ($K_0=6$). In Fig. 8, "Equations" label means that Q and φ_M have been calculated from equation (26) and by using the parameters of the macro-model given in Table V. Moreover, the Q factor has been computed from the simulated values of the ratio $m=K_{OR}/K_{MAX}$ and by solving (27) and (28). The values of Q and C_M extracted from simulation of the macro-model and or computed from equations are very close to the one obtained by simulation of the CMOS configuration using the BSIM models. To underline this accuracy of the proposed macro-model and theory, Fig.9 shows the simulated transient response of the CMOS-BSIM (Fig. 5, Table III) and MACRO-MODEL (part (b) of Fig.7, Table V). Note that the proposed macro-model is valid at AC small signal amplitude only, consequently this simulation of the macro-model shows any DC offset voltage.

Finally Table VI summarizes the main performances of the non-inverting amplifier when the phase margin is around 50° (Q factor around $Q=1$), $G_0=6$ with $R_2=5k\Omega$ and $R_1=1k\Omega$. In this case, the

compensation capacitor has been fixed to 250fF (see Fig.8) which corresponds to the one expected in theory. Note that Fig.8 confirms that calculation (theory) and CMOS simulation match very well for different value of C_M between 50pF and 400pF.

TABLE VI
Main Performances of the Non-Inverting Amplifier $R_2=5K\Omega$, $R_1=1K\Omega$ AND $C_M=250FF$

	Equations		BSIM	
	Theoretical	Macro-model .AC PSPICE	.AC PSPICE	
f_c (-3dB)	13.7	14	14	[MHz]
f_R	7.69	8.11	8.11	[MHz]
K_{MAX}	7	7.18	7.18	[V/V]
K_{OR}	5.98	5.98	5.94	[V/V]
Q	1.02	1.06	1.07	-
<i>Calculation using the theoretical equations</i>				
R_{O2}	4.74k			[V]
A_{OPL}	57.9k			[V/V]
G_M	626			[m Ω^{-1}]
A_0	2040			[V/V]
Φ_M	51.5			[Deg.]

6. CONCLUSION

This paper has introduced the operational transconductance conveyor and proposed a study of the non-inverting amplifier based on a CMOS unbuffered current-feedback-amplifier. A precise macro-model has been used and compared with theory and with an equivalent CMOS topology. We have shown that the theoretical approach which consists in the definition of the Q factor allows to set the Miller capacitance with precision, regarding the phase margin. The correlation between the Q factor extracted from simulations and the Q factor computed from theory shows relevance of the proposed approach. We hope that this study and its associated theory using the OTC description will be useful for analog designers, especially for understanding the frequency performances of the operational current feedback amplifiers. Moreover the Operational Transconductance Conveyor (OTC) is an extension of all actual type II current conveyors (CCII, CCCII, diamond transistor).

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