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Design of Pulse Synthesizers for the Convergence of IR-UWB Solutions

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Abstract—This paper presents some techniques to synthesize pulses in the context of IR-UWB. Pulse synthesizers are good candidates when different kinds of pulses are needed to comply with different standards or when the shape of the pulses needs to be modified. Two different approaches are described here. Voltage Controlled Delay Line (VCDL) based pulsers are first described. For this family, two kinds of combiners are presented : differential pairs based and H-bridge based. The second one achieves a larger output dynamic but is limited by the use of the VCDL. A second type of H-bridge based synthesizer using VCO is presented. Using both a VCO and a H-Bridge offers the largest synthesis capabilities. It allows large voltage pulses to be synthesized and the pulse duration is not limited. All proposed architectures has been implemented and their measured performances are given for comparison.

Index Terms— Pulse generation, FCC, Transmitters, Impulse Radio, Ultra-wideband (UWB), Pulse shaping circuit.

I. INTRODUCTION

Communication in the UWB band is regulated by the FCC since it has been authorized in 2002 in the 3.1GHz to 10.6GHz frequency band. Several standards have emerged such as the 802.15.4a for PAN applications, the 802.15.4f for asset tracking or the 802.15.6 for WBAN. Dedicated systems have also been developed for localization or biomedical applications but most of these applications needs low power communication systems to operate.

A general trend in communications systems is the convergence of several applications in an unique device. This allows cost reductions and increase the functionality of the devices. To reduce power consumption, functions must be shared by several sub-systems. To do so, these functions must be reconfigurable to meet various requirements. This is especially a bottleneck for RF devices which are often based on passive elements which are not tunable such as inductors. In IR-UWB, reconfigurable front-end means to be able to generate and detect pulses having different shapes, durations and central frequencies. The very wide bandwidth of the systems can be an advantage, especially on the receiver side. Non-coherent receivers are able to detect a large variety of pulses in different frequency bands. By varying the integration

time of the detector; Non-Coherent receivers can detect pulses with different bandwidths and shapes. In coherent receivers, since the correlation is little affected by the pulse shape [1], the most critical point is to control the central frequency and the width of the local pulse used for correlating the received signal. However, this ability is inherent of a correlation receiver and is not a bottleneck. On the transmitter side, the generation of a large variety of pulses is more difficult. The basic parameters to be controlled are the central frequency and the pulse width. To do so, LO switching techniques can be used. It allows the width and the central frequency of the pulse to be controlled. However, adjusting the pulse shape is more difficult whereas it highly affects the spectrum and especially the side lobes which reduces the Adjacent Chanel Power Ratio (ACPR). Several solutions have been proposed to shape the pulse by modulating the pulse magnitude with a shape function [2]. These techniques suffer from a lake of tuning abilities since they are designed to achieve a given pulse shape. Moreover, the performances of the modulator depend on the operating frequency and it is difficult to maintain a constant shape over a very wide frequency band of operation. To overcome this drawback, pulse synthesizing techniques have emerged [3]. By using a pulse synthesizer, it is possible to change the shape of a pulse to comply with different standards which have different requirement regarding the pulse spectrum and the ACPR as shown in Fig. 1.

The principle of pulse synthesizing is to control the width (τ_p) and the magnitude (g_n) of each elementary pulse ($e_n(t)$) that makes the emitted pulse $s(t)$ has given by (1) and represented in Fig. 3.

$$s(t) = \sum_{n=0}^{N-1} g_n \cdot e_n \left(t - \sum_{p=1}^{n-1} \tau_p \right) \quad (1)$$

In this paper we present several implementations of pulse

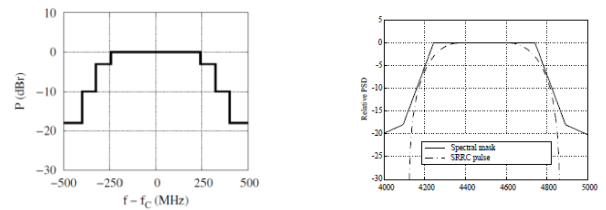


Fig. 1. Pulse Shaping for 802.15.4a and 802.15.6

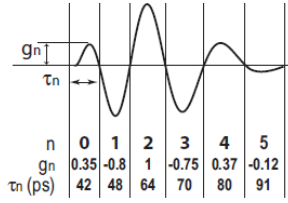


Fig. 3. Principle of pulse synthesizing

synthesizers and we discuss their performances and their limitations. In the first section, synthesizers based on Voltage Controlled Delay Line (VCDL) are presented. In this family of synthesizer, the maximum number (N) of elementary pulses is fixed. This limitation has encouraged the emergence of VCO based pulse synthesizer especially to address lower bandwidths which require a large number of elementary pulses, especially in high frequency bands. These synthesizers will be discussed in section III.

II. VCDL BASED PULSE SYNTHESIZER

The first reported work on pulse combining was based on fixed magnitude and width elementary pulse [4]. This preliminary work paves the road to the pulse synthesizing technique.

A. Differential pulse combiner based synthesizer

Based on pulse combining techniques, a pulse synthesizer has been proposed [5]. The synthesizer uses a Digital Delay Line (DDL) to propagate a rising edge. The outputs of the delay line are combined to produce delayed complementary square pulses as shown in Fig. 4. The width of the n^{th} digital pulse can be modified by changing the propagation delay in the n^{th} inverter. The pulses are then combining using current summing in N differential pairs. The outputs of the differential pairs are alternately crossed to achieve positive and negative combination of the elementary pulses. The magnitudes of the elementary pulses are fixed by the DC current in the

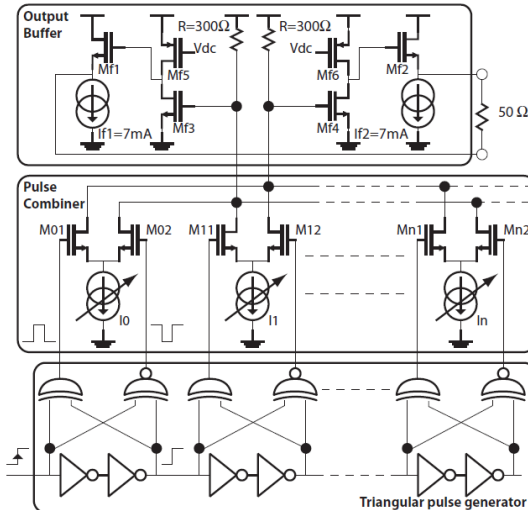


Fig. 4. Principle of differential pulse combiner based synthesizer

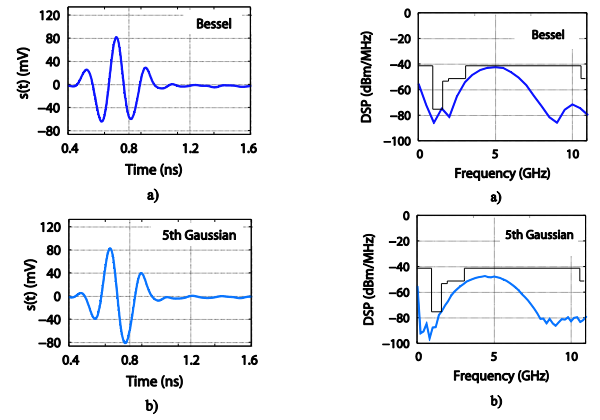


Fig. 2. Synthesized pulse shape with the differential pulse combiner based synthesizer

differential pair. The pulses are then amplified and matched to the antenna with a common source amplifier.

A seven stages synthesizer has been implemented in 130nm CMOS technology. The circuit is represented in Fig. 10.a). The active area is only $0,06\text{mm}^2$, it consumes $87.6\text{mW}@800\text{MHz}$ and it can achieve several pulse shapes as shown in Fig. 2. This first work demonstrates the possibility of synthesizing different pulse shape but suffer from many drawbacks. The DC power consumption is quite heavy due to the use of differential pair. The performances of the output amplifier highly limit the overall performances. Its limited bandwidth produces distortion and affects the pulse shape. This can be compensated with predistortion methods but the tuning of the synthesizer is not straightforward.

B. H-Bridge pulse combiner based synthesizer

To overcome the limitation of the differential pulse combiner, an H-Bridge is proposed to combine the elementary pulses [6]. The principle is presented in Fig. 5. The n^{th} elementary pulse (EP $_n$) is used to control the n^{th} branch of the bridge. The sign of the current flowing into the charge determines the polarity of the n^{th} elementary pulse and the voltage applied to the n^{th} branch set the magnitude. The same pulse digital generator is used.

An eight stages synthesizer has been implemented in 130nm CMOS technology. The circuit is represented in Fig. 10.b). The core size is $700\text{um}*400\text{um}$. Thanks to the H-Bridge

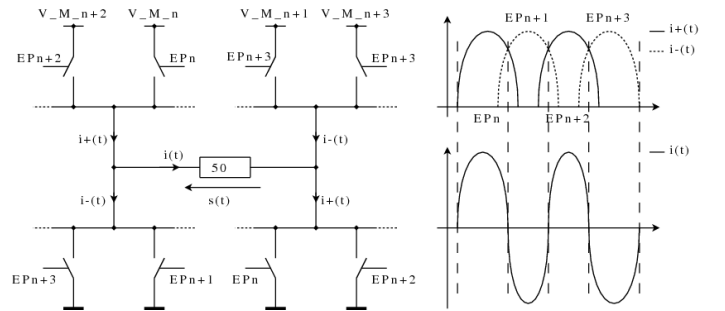


Fig. 5. Principle of H-bridge based synthesizer

architecture it consumes only 250uW@1MHz and 100uW@0Hz. It can achieve several pulse shapes as shown in Fig. 10 and several frequency bands can be addressed by varying the propagation delay in the VCDL. The maximum output magnitude is 1.8V (resp. 0.9V) when pulses centered on 2.5GHz (resp. 5GHz) are generated.

However, this structure is limited by the size of interconnection line required by the H-Bridge output because its length grows with the number of stages which is set by the number of elementary pulses to generate. For the high frequency band, the number of elementary pulses needed to generate a 500MHz pulse can be greater than 60 which makes this architecture unsuitable for the high band of the IEEE 802.15.4a and 802.15.6 standards.

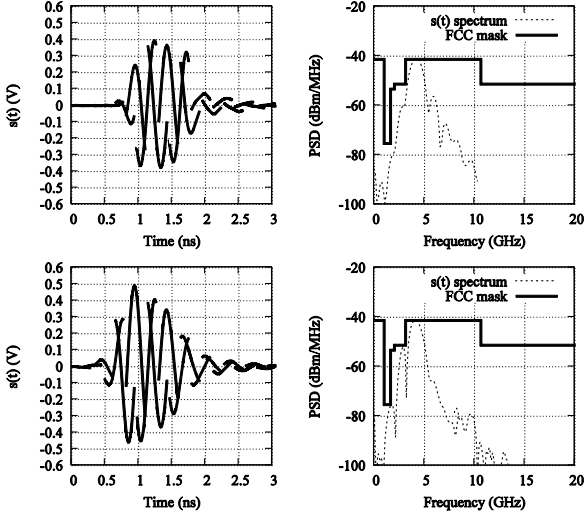


Fig. 6. Synthesized pulse shape with H-Bridge based synthesizer

III. VCO BASED PULSE SYNTHESIZER

To overcome the limitations of the VCDL based architectures when a high number of elementary pulses is needed, the implementation of a VCO based pulse synthesizer is necessary since it relaxes constraints on the size of the delay line and on the number of the required branches inside the output combining stage. However, this requires at first sight a magnitude control of each elementary pulse. Fortunately, based on an analytical analysis of UWB pulses in time and in frequency domains, it is demonstrated that a discrete symmetrical Gaussian envelope with only 5 samples ($N=5$) is enough to respect all IEEE frequency masks of 500MHz channels if a margin around 2dB is considered for ACPR [12]. Moreover, as the pulse bandwidth is independent on the central frequency of the targeted channel, it is only necessary to synchronise the sampled envelope generator and the VCO with a programmable frequency divider where the division factor is set according to the targeted channels.

An implementation of this circuit is proposed on Fig. 7. A VCO generates a sinusoidal waveform whose the frequency is equal to the central frequency of the targeted channel. A sampled envelope is synchronously generated according to this channel, each sample has also a length multiple of the sinus

half-period. Finally, an H-bridge is used to mix the sinusoidal waveform with the envelope.

To be able to address each channel of IEEE standards, the proposed architecture requires also a VCO which is able to cover all the 3.1GHz-10.6GHz band. Due to the width of the frequency band to address, it is usual to implement two oscillators, one for low band channels and another one for high band channels. However, we demonstrate in [13] that only one VCO designed with a standard 65nm CMOS technology can cover all channels. It is based on a three stages ring oscillator architecture where Current Mode Logic (CML) gates are used instead of usual CMOS gates. The oscillations frequency is also controlled by adjusting the gate source voltages of their active loads and can be started and stopped quasi instantaneously which allow OOK modulation to be obtained. Moreover, it can be put in a low power mode when oscillations are stopped, and is able to directly act as a BPSK modulator.

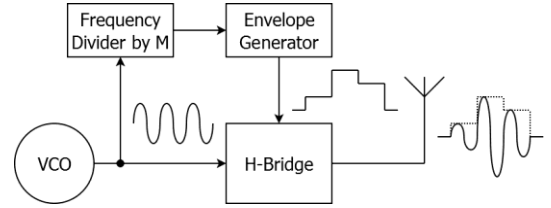


Fig. 7. Principle of the proposed VCO based pulse synthesizer

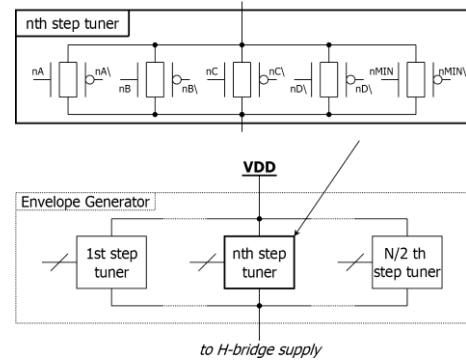


Fig. 8. Principle of the discrete envelope generator

To keep simple the control of UWB pulses shape, a sampled envelope generator, which allows each step to be tuned around their nominal values, is proposed here. To set these values, an analytical model of UWB pulses as the Gaussian up-converted pulse introduced in [14] pulse can be used after considering the required bandwidth. However, a degree of freedom on these values must be kept in order to ensure the respect of the targeted frequency masks in case of process, voltage or temperature variations. The proposed implementation is shown in Fig. 8 and used CMOS transmission gates assembled in step tuners to supply a standard H-bridge. As the Gaussian up-converted pulse is symmetrical, only 3 step tuners are required. However, an additional step tuner, which can be turned-off, has been implemented to have a better envelope control abilities. Digital control signals required by these transmission gates are set by a custom serial interface and enable by the frequency

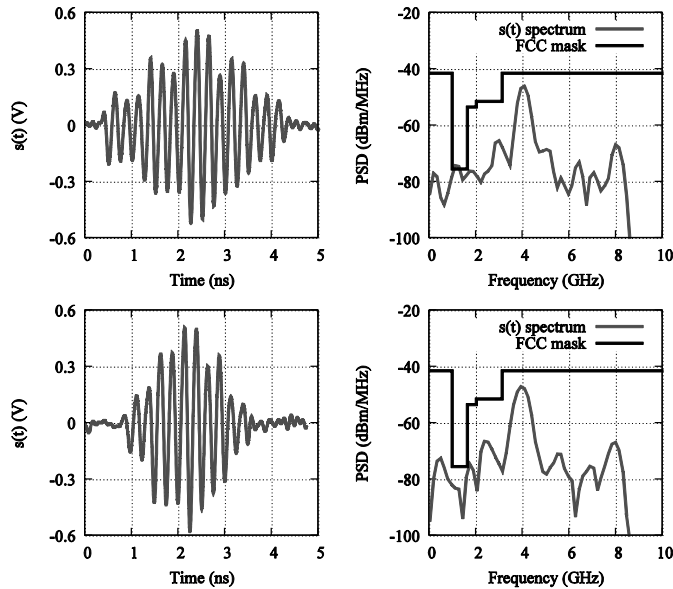


Fig. 9. Synthesized pulse shapes with VCO-based synthesizer

divider. Finally, particular values for step magnitude are fixed by adjusting the size of the transistors of the step tuner.

A prototype of the architecture has been implemented in 65nm CMOS technology from STMicroelectronics. The circuit is represented in Fig. 10.c). Its core area is $220\mu\text{m} \times 250\mu\text{m}$ and its supply voltage is 1.2V. The VCO based pulse synthesizer has been measured and it shows a peak to peak voltage of 1.1V for low band IEEE channels in the worst case. In this case, its power consumption is between $600\mu\text{W}$ and $700\mu\text{W}$ @ 1MHz, depending on the configured envelope, when a power gating cycle (turns-on, generates the pulse, and turns-off) of 10ns. Finally, two different pulses for channels 2 and 4 of IEEE 802.15.4 standard are shown in Fig. 9.

IV. CONCLUSION

Three pulse synthesizers for IR applications have been presented. The first one uses VCDL and differential pair based combiner. The combiner limits the output dynamic of this structure and the H-Bridge based synthesizer has been proposed. The H-Bridge allows high voltage pulses up to 1,9V to be synthesized but the VCDL avoid the generation of pulses having 500MHz bandwidth. A H-bridge pulse synthesizer using a VCO instead of the VCDL has been proposed to overcome this limitation.

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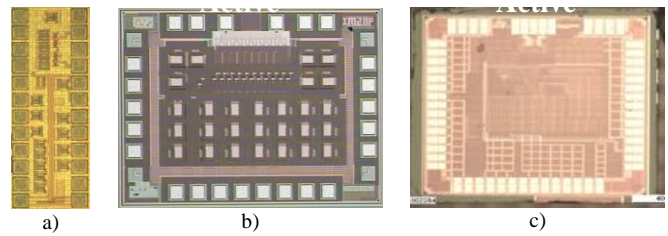


Fig. 10. Fabricated Pulse Synthesizer: a) differential pair based, b) VCDL and H-bridge Based, c) VCO and H-bridge based.

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