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Optimisation of an Integrated Bidirectional Interleaved Single-Phase Power Factor Corrector

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Abstract

This paper presents a design methodology for a full-bridge interleaved bidirectional Power Factor Corrector (PFC) converter. It applies to converters with off-the-shelf components and/or PCB-integrated passive and active components. The procedure is implemented after selection of the topology and the modulation principle. The procedure includes a selection of semiconductor based on losses calculation, EMI filter design including the impact of cell shading and inductor design. The lowest volume is found with Zero Voltage Switching (ZVS) along a complete grid period in Continuous Current Mode (CCM) at fixed switching frequency. This is usually obtained with variable switching frequency such as Discontinuous Current Mode (DCM) or Triangular Current Mode (TCM). Moreover, the paper shows that interleaving enhances efficiency and power density by sharing losses and reducing EMI filter size. A pareto front in the efficiency (η) vs power density (ρ) domain is derived to define the final result.

1. Introduction

The main requirements of next generation converters are high efficiency, high power density, high reliability and low-cost [1]. The development of wide-band gap (WBG) components such as Silicon Carbide (SiC) or Gallium Nitride (GaN) allows the switching frequency to be increased leading to denser converters [2]. To fully take advantage of

Tab. 1: Specifications of the considered Converter

$V_{IN_{RMS}}$ (AC)	230 V
$I_{IN_{RMS}}$ (AC)	15 A
$V_{OUT_{max}}$ (DC)	400 V
$I_{OUT_{max}}$ (DC)	12 A
P_{OUT}	3.3 kW
Temp. °C	-40 to 60 °C
E.M.C	EN55011 Class B conducted EMI

WBG devices and increase the power density the PCB integration of dies and/or passives is seen as a promising and low-cost approach [3][4]. Integration allows parasitic elements to be reduced leading to smaller EMI filter [5]. The paper addresses these two. This paper focuses on the optimisation procedure. This research topic is challenging because power converter design is driven by multiple objectives which require trade-offs. Optimisation procedure improves the converter performances [6][7]. As an example to the presented methodology, the paper proposes the optimisation of a highly integrated 3.3 kW bidirectional AC/DC converter with the main specifications listed in Tab.1.

Power Factor Corrector are commonly used in grid connected applications such as solar inverter or electrical vehicle on-board battery charger. PFCs ensure the compliance with harmonic standards by shaping the grid current according to the grid voltage.

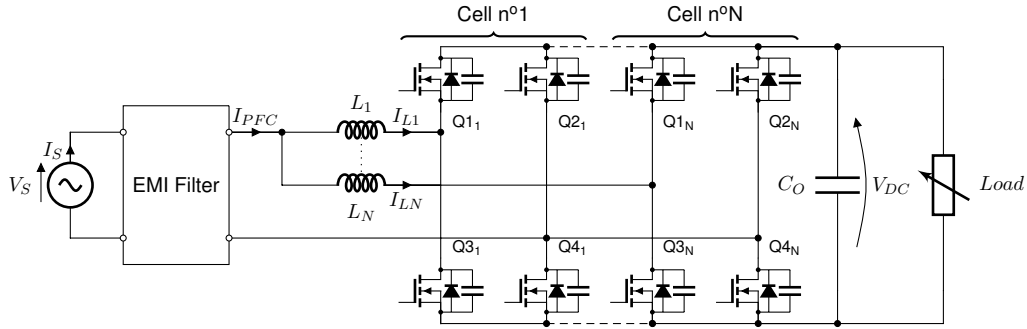


Fig. 1: Topology of the interleaved PFC composed of N High Frequency (HF) legs (odd numbers) and N Low Frequency (LF) legs (even numbers) . The combination of one LF and one HF leg with the associated inductor represents an elementary cell in the global converter.

The selected topology (full-bridge interleaved converter) is presented in Fig.1. The proposed cell association principle permits a modular converter design. The converter is controlled by an unipolar PWM modulation which means one leg is controlled at high frequency while the second one is controlled at the grid frequency. This type of modulation has several advantages such as the reduction of switching losses and the reduction of the input inductor requirements, compared to bipolar PWM [8]. The converter also operates in Continuous Current Mode (CCM). The modular approach is particularly interesting for light load operations, indeed the cell shading improves the efficiency at low power by deactivating one or more cells, as it will be highlighted below with Fig 7.b. The proposed design procedure allows high efficiency/high power density converter to be designed. In this case, advantages of variable frequency control are obtained with fixed frequency control, simplifying the implementation.

This paper is composed of three main parts, the first one deals with the optimisation procedure, which is composed of three main sections. The second part presents the optimisation results. Then, the last part provides a conclusion of this work and presents some perspectives.

2. Optimisation Methodology

Hereafter, the optimisation procedure is introduced and illustrated with Fig.2. As it is indicated in

the flowchart, three main optimisation variables are used: the switching frequency ($f_{SW} = [140 \text{ kHz}; 260 \text{ kHz}]$), the current ripple ($\Delta I = [2 \text{ A}; 12 \text{ A}]$), the number of EMI filter stages ($N_f = [2; 4]$) and the number of interleaved cells ($N = [2; 5]$). Three main parts compose the procedure, the semiconductor selection, the EMI filter design and the inductor design used for the input inductor and the EMI filter part. First of all, waveforms are analytically calculated for a set of variables. These waveforms, e.g. input current, inductor current and switch current, are used to select the semiconductor, design the inductors and the EMI filter. The selection of the semiconductor is done based on a database including SiC bare dies, the estimated volume of the gate driver (Bootstrap type) is also added. The EMI filter design considers multi-stage filters which is congruent with the integration objective, as multiple stage filters allows high attenuation capabilities with low volume [9]. Losses from each parts are used to determine the volume of thermal management. Natural convection is selected for low-cost and high reliability reasons. The thermal coefficient of $5 \text{ cm}^3/\text{W}$ is determined after analytical and FEM calculation to match the specifications. The maximal ambient temperature is 60°C and the maximal device temperature is defined as 125°C . The selection of the final converter is done including the thermal management as it generally represents an important part of the overall volume.

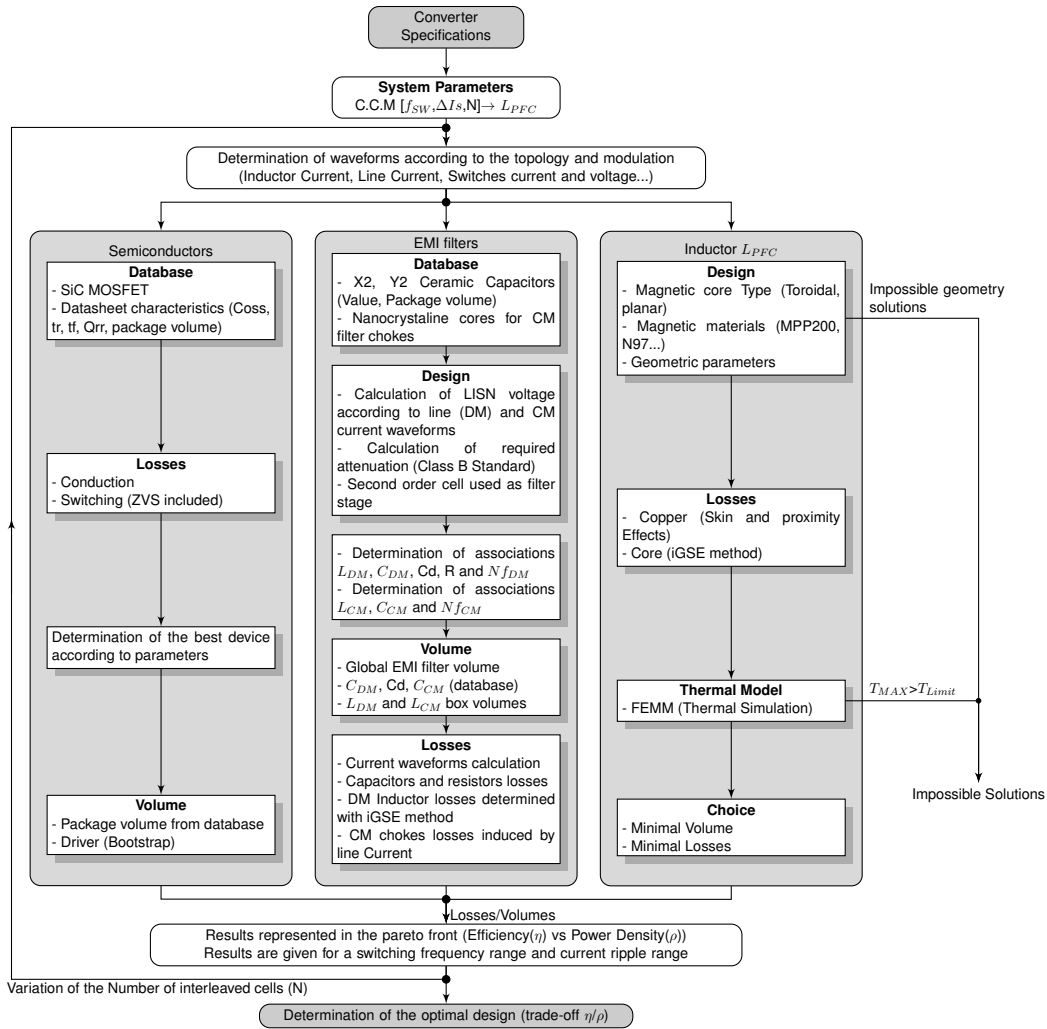


Fig. 2: Design Flow Chart representing the optimisation procedure which involves several inner optimisations for inductor, semiconductors and EMI filters for the worst operation case.

2.1. Semiconductors

PCB dies embedding was assumed to simulate a high level of integration. The main drawback of this is the limited choice of references. Hence, only SiC bare dies from Wolfspeed are considered. The database is composed of 900V and 1200V SiC MOSFETs. All parameters required to calculate losses are picked from datasheets. Losses is the main criteria for this part as the volume of the dies can be neglected compared to the heat sink volume induced by losses, even if the gate driver volume is added. Conduction losses are basically

determined with the RMS value of switch current and the on-state resistance at 150°C, as this value is more representative for high density naturally cooled power converter. Even with WBG devices switching losses may represent a large part of losses at high switching frequency. A simple and fast model using datasheet parameters has been developed to quickly compare the different devices to each other. This model includes : commutation times (rise time t_r , fall time t_f) output capacitor (C_{oss}) and the body diode's reverse recovery charge (Q_{rr}). It is important to note that reverse recovery charge can generate

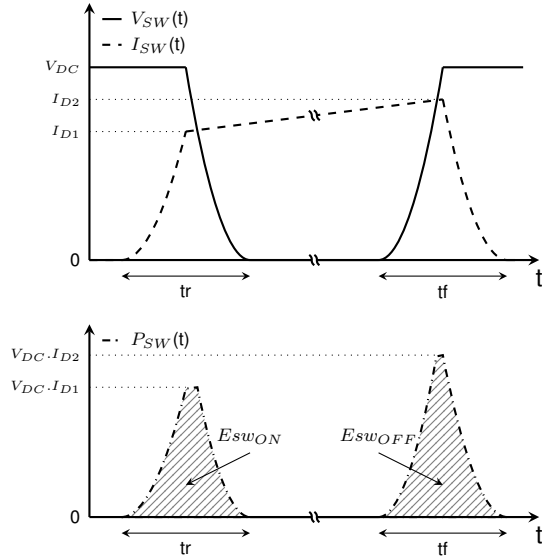


Fig. 3: Simplified commutation waveforms. I_{Dx} corresponds to the switched current which depends on the switching instant on the grid period. V_{DC} corresponds to the DC bus voltage value.

high losses, in particular if SiC Schottky diodes are not used in parallel of MOSFETs. Hence, synchronous rectification is assumed to limit the impact of the body diode [10]. Switching energies are calculated with equations (1) and (2) which are derived from the Fig.3, representing simplified commutation waveforms.

$$E_{sw_{ONx}} = \frac{1}{2} \cdot V_{DC} \cdot I_{Dx} \cdot t_r + \frac{1}{2} \cdot C_{oss} \cdot V_{DC}^2 + Q_{rr} \cdot V_{DC} \quad (1)$$

$$E_{sw_{OFFx}} = \frac{1}{2} \cdot V_{DC} \cdot I_{Dx} \cdot t_f \quad (2)$$

The selected topology allows soft switching to be achieved for at least one of the switch in the HF legs, while switching losses are neglected in the LF leg. Details about ZVS and necessary conditions for the selected topology are presented in [11].

2.2. Inductors

Two types of inductor are investigated, planar inductors are used for discrete converter design and PCB embedded inductors for integrated converter.

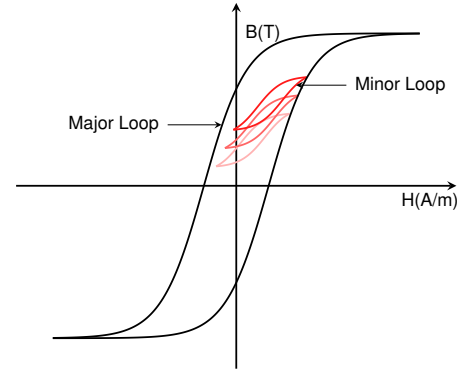


Fig. 4: Typical Hysteresis loop in PFC's inductors. The global hysteresis loop is composed of major and minor loops.

Typical current waveforms in PFC and/or inverter applications are composed of two different frequency components. The low frequency and the high frequency components correspond to the grid frequency and the switching frequency, respectively. Both components impact copper and core losses. Copper losses can be separated, on one side there is DC losses mainly induced by the current at the grid frequency (50 Hz), and on the other side the HF losses caused by the HF component (f_{sw}). The equivalent resistor depends on skin effect and proximity effect. The equivalent high frequency resistor value is determined with 3D FEM simulation. Core losses are also impacted by these two components. The low frequency induction generates one part of losses and the high frequency induction the second one. Each parts correspond to the major loop and the minor loop, respectively. Minor loops are moving along the main low frequency induction, hence additional losses are generated. Fig.4 presents major and minor loops and illustrates the phenomenon. More details about this method which uses the improved Generalised Steinmetz Equation (iGSE) and its implementation are presented in [4]. The design methodology is used for the input inductor (L_{PFC}) and for differential mode (DM) filter inductors.

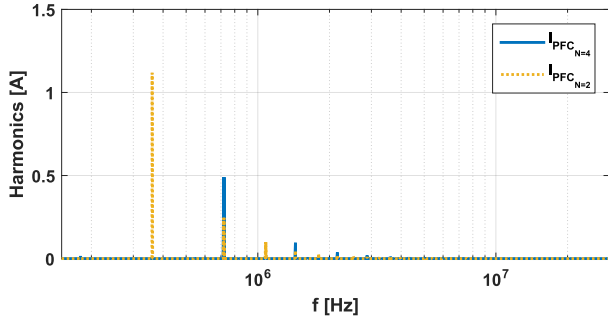


Fig. 5: Impact of cell shading on the input current spectrum for high frequency components

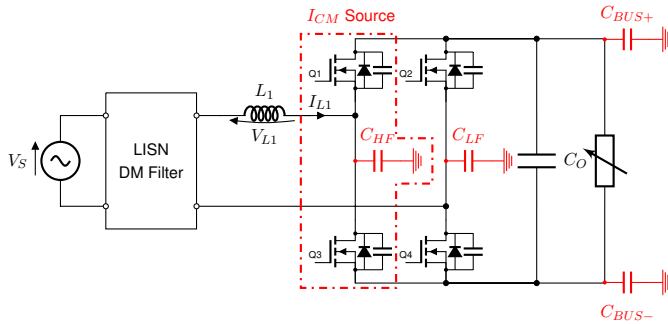


Fig. 6: Representation of parasitic capacitors used in the CM perturbation model. The red dashed box represents the CM current source, the voltage variation across C_{HF} due to the HF leg commutations is the main cause of CM EMI. Other parasitic capacitors (C_{LF} & C_{BUS}) contribute to the filtering. For the first design iteration the parasitic capacitor values are determined from knowledge feedback. C_{HF} and C_{LF} are selected to equal to 1 nF and $C_{BUS} = 10$ nF.

2.3. EMI filter

The trade-off efficiency vs power density is realised for nominal power operation, but the converter has to be compliant with the EN55011 standard for the complete range of power (330W to 3.3kW). Contrary to quasi constant efficiency (Fig.7.b) the cell shading impacts in the wrong way the design of the EMI filter. The worst case concerning EMI perturbations is considered for the EMI filter design. The most constraining case corresponds to an operation mode using the minimal number of interleaved cells, selected equal to two, because $N = 1$ does not lead to a significant increase of the

efficiency at low power. For a converter operating at fixed switching frequency, the lower the number of interleaved cells the higher the current ripple and the lower the apparent frequency, thus the bigger the EMI filter (Fig.5). Details about the DM filter design methodology are presented in [11].

Common mode (CM) perturbations are also impacted by the cell shading, therefore the CM filter is designed for the worst case too. From Fig.6 CM model is derived and used to determine the CM filter in a similar way as DM filter. Firstly the maximal capacitor (Y2 Type Ceramic) value is determined according to maximal earth current (3.5 mA). The global capacitor is then shared according to the number of CM filter stages. Note that the capacitor close to the converter is higher than the capacitor at the grid side to favour a short pass for CM current (equations (3) and (4)).

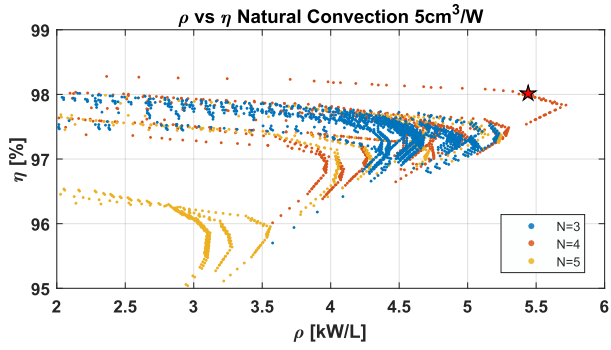
$$C_{CMtot} \leq \frac{3.5 \cdot 10^{-3}}{260 \cdot 2\pi \cdot 50} = 43 \text{ nF} \quad (3)$$

$$K = \frac{1}{2} \cdot Nf \cdot (Nf + 1) \rightarrow C_{CMmin} = \frac{C_{CMtot}}{K} \quad (4)$$

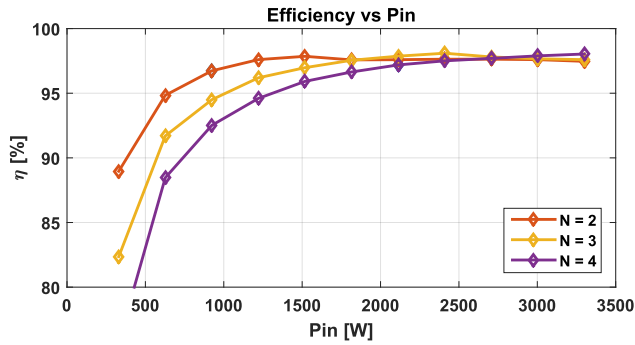
Knowing the required attenuation, the dimensioning frequency and the different capacitor values it is possible to determine the value of the CM choke, which is the same for each filter stage, as it is presented with (5).

$$L_{CM} = \frac{1}{2} \cdot Nf \sqrt{\frac{Att_{req}}{(2\pi \cdot f_D)^{2Nf} \cdot \prod C_{CMi}}} \quad (5)$$

With the required inductance, several solutions are tested depending of core and copper section. Nanocrystalline core are selected because of their high permeability, it is thus possible to reach high inductance with a reduced number of turns, which makes this technology very suitable for CM chokes. Losses generated by the CM chokes are calculated with the current flowing through windings. Natural convection is considered for CM chokes (no contact with the heat sink). The maximal temperature increase for chokes is limited to 40°C, every solution with higher temperature increase are eliminated. Finally, the procedure of EMI filter returns



(a)



(b)

Fig. 7: Results of the optimisation procedure. a) Pareto front obtained at the end of the procedure, the figure presents the impacts of the number of interleaved cells b) Calculated efficiency curves of the selected converter according to the number of operational cells, the selected converter achieves 98 % (at 3.3kW) efficiency and 5.4 kW/L.

several combinations of DM and CM filter with their respective volumes and losses.

In our case the impact of the cell shading induces an EMI filter 2.75 times higher than the EMI filter designed at nominal load using all the cells.

3. Results

The selected converter corresponds to the highest power density with a minimum efficiency of 98% at nominal power. Fig.7a) presents the results of the procedure and highlights the impact of the number of interleaved cells. The selected converter corresponds to four interleaved cells (N=4) achieving 98% efficiency and 5.4 kW/L power density with a

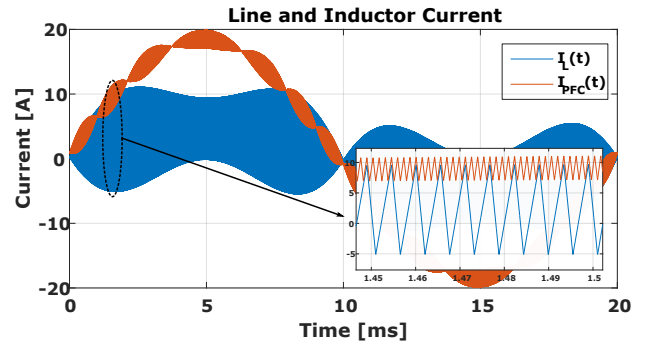


Fig. 8: PFC and inductor current waveforms for the selected converter, represented at the grid frequency with a zoom to see waveforms at the switching frequency. Note that the inductor current ripple is large, this ensures that the inductor current change its sign during each switching period. Hence, both HF switches achieve ZVS along the complete grid period.

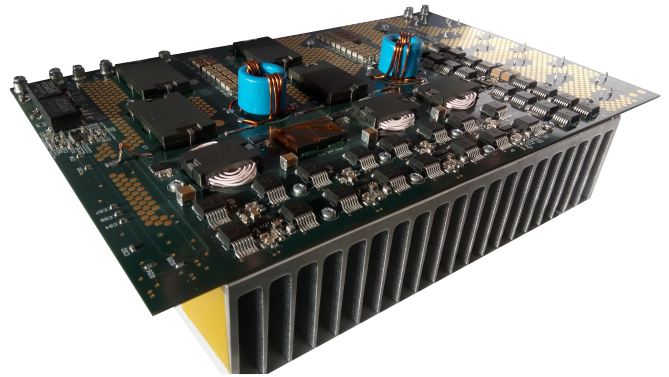


Fig. 9: Discrete converter prototype composed of four switching cells and input EMI filter. Dimensions are 33.6cm x 20.5cm. Heat sink is oversized

natural convection thermal management. Fig.7b) presents the calculated efficiency of the selected converter according to the number of active cells. Thus it is possible to determine the optimal number of active cells according to the power range. Current waveforms for the selected converter are presented in Fig.8. At first sight it seems to be counter-intuitive to tolerate such high current ripple in converter (16A in this case). Commonly, high current ripple means high losses and substantial effort on EMI management. Nevertheless, the result highlights that high current allows semiconductor losses to be reduced because of ZVS is achieved for each HF switch along the complete grid period. Usually, to

Tab. 2: Details about the selected converter. Note that the volume and losses presented for L_{PFC} correspond to the four inductors.

Design for C.C.M @3.3kW		
	η	98.01 %
	ρ	5.41 kW/dm ³
	N	4
	f_{sw}	180 kHz
	ΔI	4 A
General	L_{PFC}	34.72 μ H
	Dies	CPM3-0900-0065B
	Nb EMI filter stages	$N_{f_{DM}}=4, N_{f_{CM}}=3$
	L_{DM}	7.95 μ H
	C_{DM}	[0.33 μ F, 0.28 μ F, 0.19 μ F, 0.094 μ F]
	L_{CM}	0.544 mH
	C_{CM}	[19.2 nF, 12.7 nF, 6.5 nF]
	Total	609.52 cm ³
Volume	L_{PFC}	59.52 cm ³
	DM filter	151.36 cm ³
	CM filter	61.61 cm ³
	Switches+Driver	8.04 cm ³
	Heat sink	329 cm ³
Losses	Total	65.8 W
	L_{PFC}	32.99 W
	Switches	17.04 W
	EMI filter	15.77 W

reach this performance, Discontinuous Current Mode (DCM) or Triangular Current Mode (TCM) are used. however the control of these types of modulation is more complicated due to the variable switching frequency. Moreover the DCM does not achieve ZVS for all commutations [12]. Interleaving technique allows conduction losses to be shared between the four cells. EMI perturbation can also be managed quite easily with interleaving [13], even if the EMI filter is design for the worst case as explained in section 2.3. The efficiency and power density can be widely improved by the proposed configuration obtained with the procedure. Details about the selected converter are presented in Tab.2. The integrated prototype will be used to get a feedback for the design procedure,

such as volumes, losses and parasitic elements especially common mode capacitors.

In parallel to the manufacturing of the integrated converter, a first prototype using off-the-shelf components (7L D2PAK 900V/35A SiC MOSFET) and planar inductors was designed to validate control schemes. This discrete prototype is built with only one board to simplify debugging and measurements. The estimated power density is 1.37 kW/L including input filter, switching cells, measurement circuit and thermal management. An important point which can be noticed with off-the-shelf components is the additional volume induced by interconnection. For example, the volume of power semiconductor with the associated gate driver is twice higher than the sum of discrete volumes. This prototype is used to develop the control. Low voltage and low power tests were performed and validated the interleaving implementation. Further investigations are in progress. Efficiency measurements and EMI compliance will be tested.

4. Conclusion

This paper presents a design methodology for a 3.3kW highly integrated AC/DC converter. This work highlights the fact that high efficiency and high power density can be achieved with the well-known CCM modulation. This main result is based on a particular association of interleaving technique and high current ripple. This association allows ZVS to be achieved along the complete grid period. Hence, the selected converter reaches an estimated efficiency of 98% and a power density of 5.4kW/L even with natural convection thermal management. The selected topology associated to the optimisation procedure permits to propose an uncommon converter configuration with a particular operation mode. A discrete version of the converter was built for upstream design and validation. The integrated version of the converter is in the manufacturing chain. Experimental results will then be compared to the predicted results and to the discrete version. The feedback will permits to improve the optimisation procedure.

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