



HAL
open science

Application of the PCB-Embedding Technology in Power Electronics – State of the Art and Proposed Development

Cyril Buttay, Christian Martin, Florent Morel, Rémy Caillaud, Johan Le Leslé, Roberto Mrad, Nicolas Degrenne, Stefan Mollov

► **To cite this version:**

Cyril Buttay, Christian Martin, Florent Morel, Rémy Caillaud, Johan Le Leslé, et al.. Application of the PCB-Embedding Technology in Power Electronics – State of the Art and Proposed Development. 3D-PEIM, Jun 2018, College Park, Maryland, United States. 10.1109/3DPEIM.2018.8525236 . hal-01844981

HAL Id: hal-01844981

<https://hal.science/hal-01844981>

Submitted on 19 Jul 2018

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Application of the PCB-Embedding Technology in Power Electronics – State of the Art and Proposed Development

Cyril BUTTAY, Christian MARTIN and Florent MOREL
Université de Lyon,
INSA-Lyon, Université Claude Bernard Lyon 1,
École Centrale de Lyon, CNRS
Ampère, F-69621 Villeurbanne, France
cyril.buttay@insa-lyon.fr

Rémy CAILLAUD, Johan LE LESLÉ, Roberto MRAD,
Nicolas DEGRENNE and Stefan MOLLOV
Mitsubishi Electric Research Centre Europe
1 Allée de Beaulieu
Rennes, France F-35708

Abstract—The embedding of components in Printed Circuit Board (PCB) material is an attractive solution to improve the performance of power converters in the 1 W–100 kW range by increasing the power density (exploitation of unused volume in the PCB), reducing circuit parasitics (strip-line approach to current distribution, shorter interconnects), and improving manufacturability (rationalization of the manufacturing process, automation). This paper presents a review of the embedding technologies, with a special focus on power components (passive, active) and thermal management. The second part of the article is dedicated to the design process, and proposes a new design approach, inspired from microelectronics. The ambition is to simplify the design process by using “design toolkits”. These toolkits would provide the designer with elements such as design rules, libraries or models. The objective is to enable automatic design validation, and to ensure the design can be produced directly.

I. INTRODUCTION

For more than 100 years, evolution in power electronics has mainly been driven by improvements in the switching components [1]: valves, silicon transistors and thyristors, MOSFETs, IGBTs. Silicon-based components are still progressing, with the introduction of the superjunction MOSFETs or the trench IGBTs [2]. Since 2001, wide band-gap materials have been commercially introduced: Silicon Carbide (SiC) and Gallium Nitride (GaN).

From a circuit point of view, many topologies were introduced over the years [3], and a sound theory has been built [4]. It seems to be a consensus nowadays that there is not much improvement to be expected from a new power circuit topology [1], [5], [6]. A large part of the current research activity regarding circuit design focuses on the “multi-cellular” approach [7], where elementary switching cells or elementary converters are associated to form a larger converter. This has the advantage of modularity, reduced electro-magnetic interference – EMI – (with proper control, the elementary blocks produce interference which partially cancel each other) and inherent fault-tolerance, at the cost of increased complexity.

The next driver for progress is considered to be integration and packaging [1], [5]–[8]. Future packaging technologies

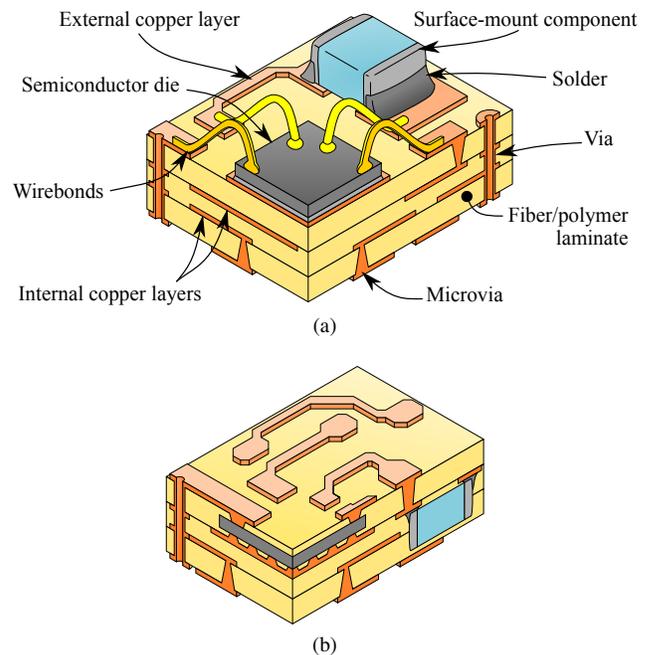


Fig. 1: (a) Standard PCB with devices mounted on its surface; (b) the same devices embedded in the PCB.

should offer better electrical and thermal performances, low cost, and should be able to manage the complexity of the multi-cellular approaches.

Among the possible integration technologies, printed circuit board (Fig. 1a) is particularly attractive: because it is a mature technology, many advanced design tools are available, as well as a full manufacturing supply chain. It allows a high density of interconnects, and is relatively inexpensive. Many manufacturing steps of a PCB rely on batch processes, i.e processes which are performed simultaneously to all parts of a PCB panel, independently of its size and of the number of features it contains. This is a fundamental aspect, also found in microelectronics (wafer-level processing): for a given

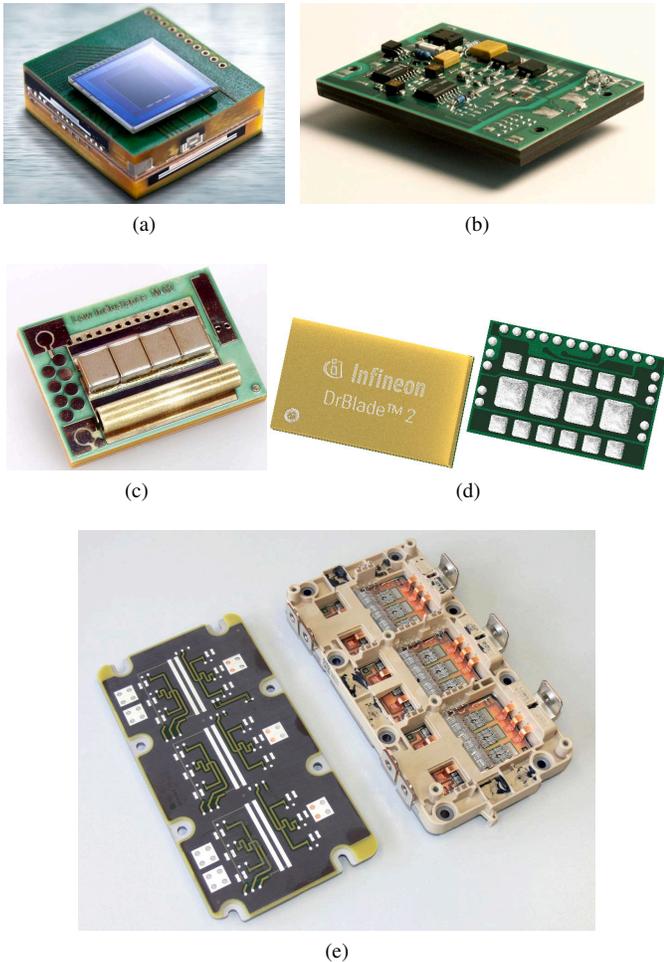


Fig. 2: Some examples of PCB integration: (a) a (cross-sectioned) camera module which includes data processing and power management in the PCB (total size $16 \times 16 \text{ mm}^2$) [9]; (b) a 60 W, credit-card-size converter with magnetic and capacitive components embedded in the PCB [10]; (c) 4 SiC dies embedded in a PCB, with decoupling capacitors [11]; (d) a commercial application: “Dr Blade”, which includes MOSFET and gate driver in the same PCB package (source: Infineon); (e) comparison between a 50 kW power module with embedded dies (left) and standard technology (right), approximate size $15 \times 8 \text{ cm}^2$ [9].

manufacturing configuration (equipment used, layer count in the PCB. . .) cost and turnaround time are independent of the circuit design.

With the ever increasing need for more compact electronic systems, integration technologies have been developed to take advantage of the inter-layer space in multi-layer PCBs (Fig. 1b). *Component embedding* was first introduced in the 80’s for ceramic circuits, and implemented with organic PCBs in the 90’s [12]. This topic has been particularly active in Europe, with research institutes such as Fraunhofer IZM [9], or companies such as Hofmann Leiterplatten [13] or Imberra

Electronics [14]. Since 2010, this technology has attracted a lot of interest, with relatively complex circuits being produced, such as the camera in Fig. 2a. These circuits include several semiconductor dies, passive components (resistors, inductors, capacitors), etc.

If we focus on power electronics, examples of PCB integration are given in Figs. 2b to 2e. In Fig. 2b, layers of magnetic and dielectric materials are stacked with copper and polymer-impregnated fibre sheets (“pre-pregs”) and laminated to form a solid substrate with embedded passives [15]. In Fig. 2c, SiC dies are embedded in a PCB, with decoupling capacitors mounted on the surface directly above. The authors demonstrate that this configuration generates a parasitic inductance of less than 1 nH [16], [17], 10 times lower than the best commercial power modules currently available. A larger-scale demonstrator, developed during the German project “Hi-Level”, is presented in Fig. 2e, with a side-by-side comparison of two “modules”: each of them includes 18 IGBTs and 18 diodes to form an inverter with a 50 kW rating, but the one based on PCB embedding is much thinner than the other (millimetres compared to centimetres). Finally, an actual industrial application of PCB embedding is presented in Fig. 2d. This circuit integrates two power transistors and the corresponding half-bridge gate driver IC. It is produced at a large scale (production capability is 3.3 million per month [18]).

It is worth noting that component embedding is not the only way to take advantage of PCB technology: in [19], a flex-rigid PCB is folded in an intricate way to form the windings of a magnetic component and wrapped around large capacitors to encapsulate the converter. In [20], a multi-layer PCB is laminated on a ceramic substrate to host the gate driver circuit, but wirebonds are still used to connect the power semiconductor dies. These wirebonds are replaced by a flex PCB substrate in [21]–[23] to form low-inductance interconnects. In [24], a comparable approach is chosen with rigid, multi-layer PCB instead of flex. In [25], standard PCBs are populated with surface-mount components that have a uniform thickness, to allow for dense PCB stacking. However, none of these techniques offer the same level of integration and manufacturing process rationalisation as PCB embedding.

A comprehensive article recently presented the state of the art of PCB embedding for power electronics [26], and [9] gives an history of the technology, with a strong focus on embedding power semiconductor devices. As embedding develops (this is particularly true for signal electronics), standards have appeared such as JPCA-EB01, CEI 62878 and IPC 7092 [13], [27]. For power electronics, however, many issues still have to be addressed, and are discussed in the next section. The design process in itself has to be reinvented; propositions are made in section III.

II. TECHNOLOGY REVIEW

Some signal electronic systems were produced with almost all components embedded in PCB (see Fig. 2a for example). However, this is not the case for power electronics: so far, the research has focused on embedding only a subset of a

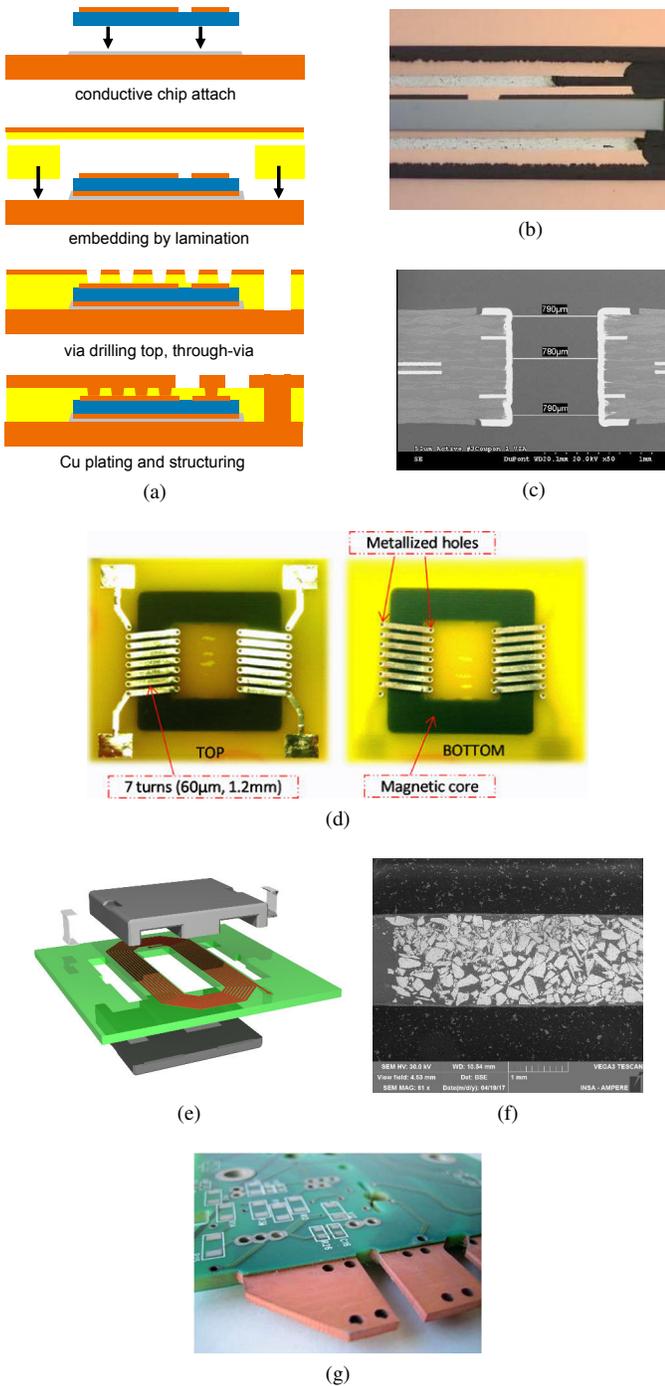


Fig. 3: Embedding of some components: (a): manufacturing process to embed a power semiconductor die in a PCB [9] and (b) a cross section of such die (dark grey) embedded in a laminated PCB with sintered-silver (light grey) interconnects; (c): cross section of a PCB with an embedded capacitive layer (visible in the middle of the board) [28]; (d) embedding of a ferrite core (30 mm on a side) to form a common-mode filter [29]; (e): concept of the “planar” magnetic component, with a magnetic core clamped around PCB windings; (f) direct embedding of ferrite powder to form a large-size inductor (50 mm diameter) [30]; (g) a thick copper conductor for handling large currents (hundreds of amperes) (source: <https://www.isoltronic.ch/>).

converter (in many cases the active devices, but embedding of passives has also been investigated). This is why the review below is proposed on a component-per-component basis.

A. Embedding of Active Devices

Most of the research and development on component embedding is actually focused on active devices. It was first developed for microelectronic devices, with thin dies and a high number of interconnects [9], [31], mounted flip-chip prior to embedding in a PCB. For power semiconductor devices, the embedding technique is different, because most of them require contacts to be taken on both sides of the die. Several solutions were investigated to form these contacts: in [17], the dies are populated with gold “stud bump” prior to embedding; after lamination, windows are machined in the PCB to retrieve the gold bumps. In [32], a thick copper buffer is mounted on the dies prior to embedding; mechanical drilling is performed later, followed by copper electroplating. In [33], a piece of metal foam is stacked on top of the die to provide electrical connection with the copper layers in the PCB.

In most cases, however, a laser is used to ablate the PCB material and get access to the dies after embedding: either a low power CO₂ laser [34], which offers a good selectivity (it ablates organic materials but not metals), or a UV laser, which is more accurate, but has no selectivity [14], [35], [36] (Figs 3a and b). This laser-drilling technique offers the advantage of using tools that are standard in the PCB industry. However, it requires the dies to have copper pads, which is not standard (most power dies have aluminium on top, for wire-bonding, and silver on bottom, for soldering). Copper is indeed required for the electroplating step which follows drilling [37]. Although producing semiconductor dies with a copper finish does not constitute a major scientific challenge, such dies are currently difficult to procure. Some alternative deposition methods were investigated such as cold spray [38] or sputtering [39].

Finally, another approach is the embedding of packaged devices (*inserted devices*, see section II-C, below) rather than of bare dies, as depicted in Fig. 2a. This is a simple solution for integrated circuits such as gate drivers, but is not so attractive for power semiconductors as the packaging constitutes an additional thermal barrier. It may, however, constitute a workaround for the lack of copper die finish discussed above.

B. Embedding of Formed Components

Capacitive films [40] can be used in the PCB stack-up (Fig. 3c), to form capacitors which are distributed over the entire board. These are basically a single-layer plane capacitor ($C = \epsilon S/t$, with C the capacitance, ϵ the permittivity of the dielectric material, t its thickness and S the surface of the capacitor). While this is particularly efficient for microelectronics, where low capacitance values (pF to nF), low voltage (3 to 5 V) and very high frequency capacitors are required, it is not so suited to power electronics: the capacitance required is often more than one micro-farad, and voltages can reach thousands of volts. Most available films have a capacitance

value of around 1 nF cm^{-2} , with voltages ratings lower than 100 V peak [40]. High permittivity materials such as BaTiO_3 ($1,000 < \epsilon_r < 10,000$) are used, but they are mixed with organic binders, to form large films which can be handled for fabrication, resulting in an equivalent $\epsilon_r < 100$, hence the low resulting capacitance.

Magnetic components are especially attractive candidates for embedding, because they are custom components which occupy a large share of a typical converter (13 % of the volume in [41]), and the manufacturing of their copper winding is not very efficient (they are individually wound, with possibly many turns). Planar components (Fig. 3e) partially address these issues, but full PCB embedding goes further as depicted in Fig. 3d. However, so far the research has mainly focused on the low-power (1–100 W) range [42], [43], which is especially suited to the “Point Of Load” (POL) converters used, for example, in the power management of computers.

Road-maps for POL converters [44] and more general power embedding [26] show that little improvements are to be expected from the magnetic materials in the foreseeable future. Most of the gain should come from a better use of the existing materials. This includes techniques such as the embedding of solid cores, as depicted in Fig. 3d [29], [42], [45], which may be difficult to extend to higher power levels (i.e. larger cores), because solid cores (ferrite, iron powder, etc.) are brittle, and yet must endure the high laminating pressure (2 MPa) experienced during PCB manufacturing. More compliant materials were also investigated, such as organic pastes with a ferrite load [46], direct embedding of ferrite powder [30] (Fig. 3f), use of Low Temperature Co-fired Ceramic materials [47], [48], or use of thin-layers (tens of microns) of permalloys or amorphous materials [49]. Their performances tend to be lower than those of solid cores, but they may be more attractive for manufacturing. Even for solid cores, copper losses were found to increase much faster with frequency for embedded inductors than for standard, wire-wound inductors [50].

C. Embedding of Inserted Components

For power electronics, multi-layers capacitors are usually required. While it is possible to stack many dielectric layers during PCB fabrication, this is unpractical as it requires patterning (etching) of as many copper layers to form the electrodes of the capacitors. At the moment, the most practical solution is to embed surface-mount components [51], as depicted in Fig 1b. Such components must sustain the lamination temperature (in the order of $200 \text{ }^\circ\text{C}$ over 1 h) and usually integrate many layers of ceramic dielectrics with high permittivity (such as BaTiO_3 , this time without any organic binder), so they offer capacitance densities of more than $10 \mu\text{F cm}^{-2}$. They are, however, quite sensitive to mechanical stresses. This was investigated during the FP7 project Hermes [35], but only for very small capacitors ($1 \times 0.5 \text{ mm}^2$) [52], which are much smaller than required for most power converters.

To embed multilayer capacitors (as well as for any other surface-mount component such as IC, resistor, etc.), they are



Fig. 4: Dual-phase passive cooling systems using PCB technology: (a) a heatpipe formed by a cavity in a PCB [53]; (b) a 2 mm diameter tubular heatpipe inserted in a PCB (cross section view) [54]; (c) a thermal ground plane (vapor chamber) which can be inserted in a PCB stack-up.

assembled to a patterned board (using, gluing, soldering, or any standard attachment method), and cavities are machined in the prepreg sheets which are to be stacked on top [13]. This allows for a reduction in the pressure experienced by the embedded components during lamination, but requires a careful evaluation of the cavity size and of the amount of resin to provide for proper filling. As standard attachment methods are used, virtually any component can be embedded.

D. Thermal management of Embedded components

Standard PCB materials have poor thermal conductivity (around $1 \text{ W m}^{-1} \text{ K}^{-1}$ [55]). Alumina-loaded materials can achieve up to $5 \text{ W m}^{-1} \text{ K}^{-1}$ [55], but they are sensitive to the growth of conductive anode filaments, which may cause short circuits [39]. Thicker copper conductors can provide better heat spreading [56] and increase the current carrying capability of the PCB (Fig. 3g). The thermal inertia very close to the die is very important for short-circuit robustness [57]; PCB-

embedding potentially allows adding a comparatively high mass of copper on both sides of the die.

While copper vias can be used to achieve a thermal conductivity in the z-axis which is comparable to that of bulk copper [36], [58], this is not so true in the x- and y-directions. Anisotropic materials such as pyrolytic graphite sheets can be used to increase this in-plane conductivity to values as high as $1700 \text{ W m}^{-1} \text{ K}^{-1}$ [59]. A more radical approach to thermal management is to embed dual-phase cooling systems such as heatpipes [53] (Fig. 4a), [54], [60] (Fig. 4b) or vapour chambers (also known as thermal ground planes, Fig. 4c) [61]. Both are closed systems which rely on the phase change of a fluid to overcome the intrinsic limits of heat conduction through solids. They also may be more mechanically compliant than a solid lump of metal.

Finally, the thermal interface material (TIM), which thermally couples the PCB to a heat-sink, is typically the weakest link in the thermal path. Some electrical insulation is typically required in power electronics applications, and most electrical insulators are poor thermal conductors. PCB-specific solutions include the use of FR4 prepreg or transfer adhesive to attach an aluminum plate to the PCB [62]. Another alternative to standard soft TIM is to use a gel TIM located in a cavity of the PCB [63].

E. Reliability tests

As the embedding of power devices is still in its infancy, the focus is still more on technology development than on reliability testing. For smaller components (as used in microelectronics), the technology is more advanced, and research groups have already implemented design rules based on reliability data [52], [64].

As power devices tend to be used at higher temperatures ($T_j = 175^\circ\text{C}$ or more, either because of harsh environmental conditions, or because of their power density), the temperature capability of the PCB material itself must be investigated. Several studies demonstrated that some materials (such as hydrocarbon-ceramic materials) can survive more than 10 000 h at 250°C , providing they are properly protected from oxidation [65]. Although they do not offer the best temperature capability, even the standard epoxy-based materials (FR4) can sustain 190°C over more than 1000 h [66], providing they are protected from oxygen.

Thermal cycling is also a matter of concern, as standard PCB materials tend to have a high Coefficient of Thermal Expansion – CTE – (more than 40 ppm/K in the z-direction [67], and even 240 ppm/K above the glass-transition temperature). Fibers (glass, aramid. . .) are added to form composites with a much more limited CTE in the x and y axes (13–15, [67]), but it remains higher than the CTE of Si or SiC dies (3–4 ppm/K) or ceramic capacitors (10–15 ppm/K [68]). However, for dies embedded in available low-CTE materials, it has been demonstrated [39], [55] that it is possible to achieve a reliability on par with that of standard power modules. With the same sort of low-CTE materials [69] showed that an embedded magnetic core could sustain more than 1000 -50/+200 °C cycles while an

identical core embedded in standard FR-4 material was broken after 150 cycles. The robustness of more complex structures to thermal cycling is still to be assessed, as large elements can be embedded in the PCB of a power converter (copper layers of several millimeter in thickness, larger magnetic cores, etc.)

F. Conclusions on the Technology Review

PCB embedding is a rapidly developing technology. Solutions have been proposed for the embedding of dies, passives, thermal management systems, with very good performances. At this stage, there are no obvious “showstopper” which could prevent further progress. There are, however, many challenges still to be addressed, such as (in no particular order):

- Development of devices for embedding: dies with suitable finish, specific packages for ICs, compatible passives. . .
- Management of many components with multiple form factors or shapes: there is a risk we might end-up replacing air with PCB material instead of producing more compact converters.
- Rational use of embedding: an optimal circuit probably uses both the volume (embedding) and the surfaces of the PCB. At the moment, there is no clear definition of which components should be embedded and which should remain on the surface.
- Use of the overall form factor: PCB embedding tends to produce flat circuits (a few millimeters thick, and several centimeters wide), which are not always practical. Stacking of several PCBs or producing thicker PCBs are possible workarounds, but they come with their own drawbacks (complexity of the interconnects, thermal management, complex manufacturing process. . .).

Many of these issues must be addressed at the design level, which is the subject of the next section.

III. TOWARDS AN INTEGRATED DESIGN ENVIRONMENT

A 2015 contest, organised by Google and the IEEE (the “Little Box Challenge”, with a 1 M\$ prize) demonstrated that advanced converters could achieve at the same time a very high efficiency (>95% in a 2 kW photo-voltaic application) and a very high power density (up to 12 kW L^{-1} , 10 times that of commercial units) [41]. A detailed analysis of this contest [70] highlighted two main scientific challenges: advanced integration technologies for active and passive devices, and efficient, computer-based design techniques. As discussed above, PCB embedding is an attractive candidate regarding the advanced integration technology. This is, however, not so clear for the computer-based design techniques. This section proposes a new design approach which relies on PCB embedding.

A. Current Design Methods in Power Electronics

Power electronics is intrinsically a complex topic (see Fig. 5): the design of a converter involves several physical domains (electrical, thermal, mechanical), and is based on heterogeneous materials and hardware [71] (as opposed to the monolithic silicon integration encountered in microelectronics). This is a real challenge, as most computer-based

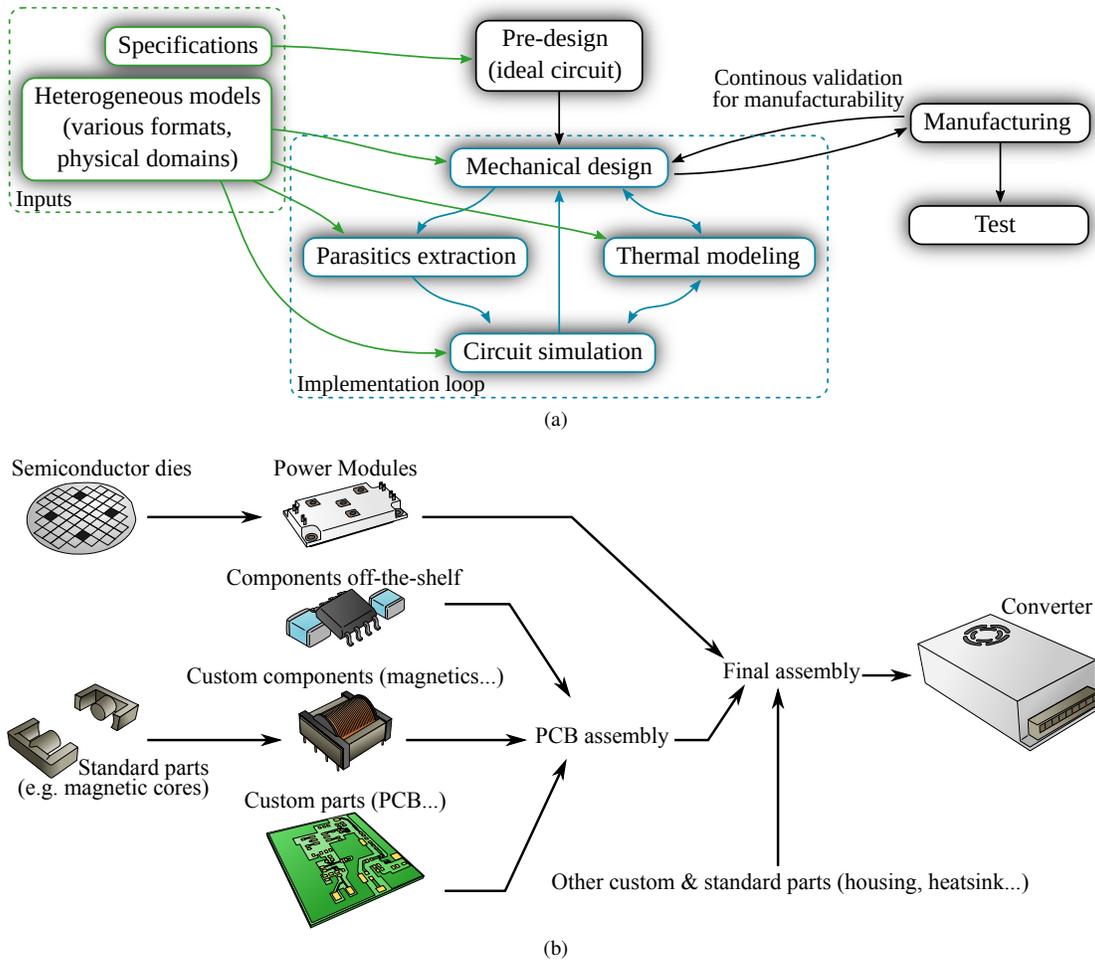


Fig. 5: (a) Overview of the design workflow of a power electronic converter: a pre-design (circuit topology, selection of the main components) is derived from the specifications of the converter. Then, using the available component models, more accurate simulations are run, including the effect of the parasitic elements or thermal analyses. This process is iterated several times until the converter offers satisfying performance (“implementation loop”), with frequent validation with the manufacturers to ensure all the parts of the converter can actually be produced. Eventually, the design is sent to manufacturing, and tested. (b) example of an assembly process (kilowatt-range): a custom PCB is manufactured, and populated with COTS (Components-Off-The-Shelf) as well as custom components (typically the power inductors or transformers); the power semiconductors are usually pre-packaged in power modules (although they could be supplied as discrete components); PCB(s) and power module(s) are then assembled and secured to a heatsink and a custom housing to form the final converter, in a largely manual process.

modelling tools only address one physical domain, or one technology.

In recent years, several research groups have proposed “design workflows”, where various pieces of software are linked together to simulate the behaviour of a “virtual prototype”. Some use a mix of Finite-Element Modelling (FEM) software and circuit simulators, to analyse the electrical and thermal behaviour of a structure [72], and even to integrate the thermo-mechanical stresses arising from thermal cycling [73]. As FEM is computationally intensive, other groups developed model reduction techniques to produce lighter models [74], [75]. These models can then be used in an automated process to design a converter with optimised performance (efficiency, power density...) [76]–[78].

A common issue with computer simulation is the lack of suitable models [79]: the description languages for circuit models are incompatible with each other (SPICE, MAST, VHDL-AMS...). Even implementations of the same description language differ largely from one simulator to another. Regarding FEM models, they require many parameters [80] which are either not available (e.g. internal layout or composition of a power module), or very specific: in [81], we showed that mechanical simulations not only required the information regarding the shape and composition of a layer, but also about its manufacturing process (in this case the properties of the layer were affected by annealing).

Overall, because of the lack of integrated design tools, and because power electronic systems rely on many differ-

ent manufacturing processes (for the various components, the interconnections, the thermal management, etc.), most design processes include many iterations (several hardware prototypes), for which computer simulation is used more for analysis than for design [82]. This is very different from the microelectronics world, where the design flow relies on software suites which integrate the manufacturing constraints and all the required models through “Design Toolkits”. This “Design For Manufacturing” approach ensures that the designed circuit can be manufactured, and that the manufactured circuit behaves as expected.

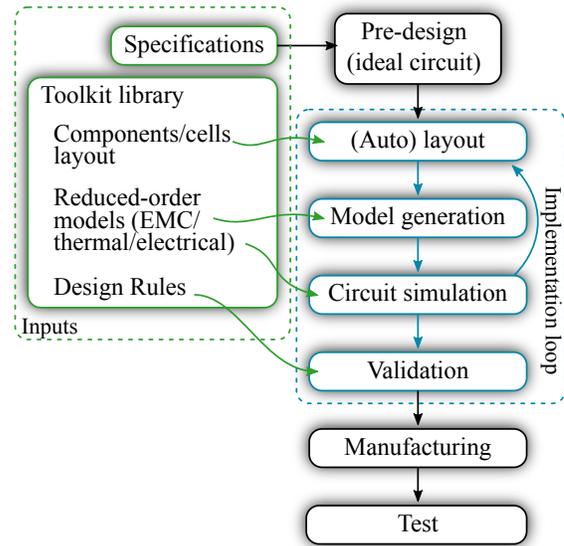
B. Proposed Design Approach

In microelectronics, designers use an Electronic Design Automation (EDA) software suite, which allows them to design their circuit, simulate it, implement it (“generate the masks”) and perform all sorts of validations and checks during the process. The manufacturing technology (whether it is 14 nm CMOS from foundry X or 0.35 μm BCD from foundry Y) is considered from the beginning of the design process, by using design toolkits, which contain libraries of elementary cells (simple gate or more advanced functions), with all the data to simulate or route them. Libraries also implement design rules related to the technology, to enable design validation. Advanced simulation tools allow not only to simulate the circuit, but also to extract the parasitic elements (capacitances, crosstalk, etc.) or to perform a thermal analysis.

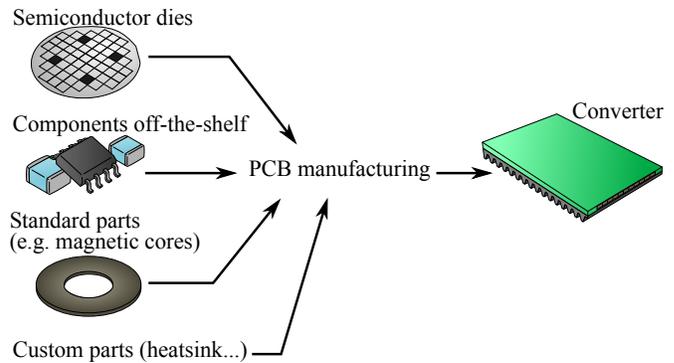
Basically, a single person can design a new integrated circuit entirely on a single computer, and generate manufacturing files which are directly used at the foundry. This “design toolkit” approach is not new: in 1980, Mead and Conway [83] introduced a set of design rules for the design of Integrated Circuits (ICs). In particular, they proposed to express all dimensions of a transistor as a multiple of a single value (which would become the “node size”, the main metric in the Moore law). Compared to the manual design used at this time, this simple approach removed a lot of flexibility. But it made it possible to use computer in the design phase, to manage the increasing complexity of IC design, triggering what is known as the “VLSI revolution” (Very-Large-Scale Integration).

An approach inspired by the EDA processes was initiated, with the “Power Electronics Design Automation” (PEDA) [71]. It is based on standard PCB technology (i.e. without embedding). A library of circuits (actually low-power, isolated DC-DC converters) is used to design converters with larger power/voltage/current ratings by combining those in the library in series and parallel. Many tasks are automated (such as code generation for the controller, or routing of the layout).

PCB embedding is a consistent manufacturing solution, with batch processes which are much like the wafer-level manufacturing encountered in microelectronics; the geometry of the layout is perfectly controlled (all components are mounted on a single rigid board), so they can be modelled and analyzed; powerful PCB design tools, with some simulation and validation capabilities are available. PCB embedding is therefore a particularly attractive candidate to extend the



(a)



(b)

Fig. 6: (a) Proposed design workflow based on PCB embedding: compared to Fig. 5a, a library with consistent models is supplied upfront (made possible by the use of a single, well controlled manufacturing technology). This allows for automatic model generation (extraction of parasitics, generation of compact thermal models..., as well as automatic validation against the design rules. As it is largely automated and autonomous, the implementation loop can be run rapidly, resulting in an optimized design, which can directly be sent to manufacturing, without additional validation step.

(b) corresponding assembly process, also simplified, as all the customization now takes place during the manufacturing of the PCB (which, in this ideal case, also provides the housing). Several levels of intermediate packaging are thus removed (power modules, bobbin for the magnetic components, etc.

microelectronics EDA approach to power electronics, in what we call the *Power Electronics Embedding Design Automation* (PEEDA).

The expected benefits of PEEDA are many: there is, of course, the ambition to move to full “virtual prototyping”, to reduce design time and cost. But other outcomes might be of comparable if not greater interest: the “fabless” approach, where many companies can focus on design with little investment upfront, while manufacturers focus on technology optimization; the shared runs (similar to the multi-project wafers), where many designs which use the same technology are assembled on a single PCB panel to share the tooling costs; the simplification of qualification tests (as the same technology is reused many times, not all the qualification tests have to be repeated for every product). Finally, the scalability of the PCB process allows an identical product to be made as a few units or as millions.

C. Getting There

While there are clear benefits to using PEEDA, and although it is based on the tremendous PCB ecosystem, it still requires a lot of development work.

- Definition of the design flow: many software tools are available, including PCB design, parasitic extraction, thermal analysis, etc. But their inter-operation is still limited, involving a lot of manual work to move back and forth. Device models are often incompatible, and many simulators cannot handle the complexity of a power electronic converter circuit (with time constants ranging from sub-nanosecond to seconds or minutes, complex inductive and capacitive coupling, etc.). Simplified models are a possible solution to address this complexity, but in any case, they must be generated automatically.
- Definition of the design rules: this includes some rules aimed at manufacturability or reliability, which must be validated experimentally (this is especially true for large embedded passive devices, for which little is known regarding reliability). Again, these design rules must be in a form which allows automatic validation. These design rules could also include the definition of the technology itself (for example the definition of standard PCB stack-ups, e.g. a given number of layers) to enable the “multi-project” panels presented above.
- Development of embedded power devices: many power components are not available yet in embedded form (larger passive components, sensors, etc.). Even the power semiconductors, which focus most of the work on embedded devices, are still very difficult to procure with suitable finish. There is still considerable work to be undertaken to develop the embedding technology.

Another aspect should not be underestimated: the impact of devices embedding on the existing PCB supply chain. Indeed, embedding requires handling components (including bare dies) in PCB factories, something which is not common nowadays. Device embedding also has a very strong impact on the “value” chain: as known good devices are embedded in a PCB, and

rework is not possible, any process failure is much more expensive. Production yields of 99 % [64] or even 99.7% [51] are required for such technology to be of any interest.

IV. CONCLUSION

PCB embedding is a very active topic, especially on the technological front, with many research teams involved. Very good performances have been demonstrated regarding size reduction, improved switching performance, thermal performance, or even reliability.

While the development of the technology is still ongoing, and there is still much to be made, we think some effort should now be focused on the design process. Indeed, PCB embedding has the potential to enable the “VLSI revolution” of power electronics, providing suitable design tools are available. Much like with the integrated circuits, this will require trading some flexibility for manufacturing process optimization and design automation.

A “design toolkit” approach is proposed, inspired by microelectronics. This toolkit fully describes the manufacturing technology to guide the designer and enable automatic validation. This “design for manufacturing” approach should ensure seamless transfer from design files to a manufactured product.

The expected outcomes of such approach include shorter development cycles, flexible design (“bespoke converters”), shorter qualification procedures, and lower initial investment (“fabless” approach).

ACKNOWLEDGMENT

The authors would like to thank Mr. Jean-Christophe CRÉBIER and Yves LEMBEYE, from G2ELab for their fruitful discussions.

REFERENCES

- [1] J. D. van Wyk and F. C. Lee, “On a future for power electronics,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59–72, 2013. [Online]. Available: <http://ieeexplore.ieee.org/abstract/document/6548072/>
- [2] G. Majumdar, T. Oi, T. Terashima, S. Idaka, D. Nakajima, and Y. Goto, “Review of integration trends in power electronics systems and devices,” in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, March 2016, pp. 1–10.
- [3] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. IEEE COMPUTER SOC PR, 2002. [Online]. Available: http://www.ebook.de/de/product/3799992/ ned_mohan_tore_m_undeland_william_p_robbins_power_electronics_converters_applications_and_design.html
- [4] R. D. Middlebrook and S. Cuk, “A general unified approach to modelling switching-converter power stages,” in *1976 IEEE Power Electronics Specialists Conference*, June 1976, pp. 18–34.
- [5] E. Prem, “Electronics enabling efficient energy usage – results from the E4U project,” E4U, FP7 project, Project Report, 2009. [Online]. Available: www.e4efficiency.eu
- [6] S. C. Ó Mathúna, P. Byrne, G. Duffy, W. Chen, M. Ludwig, T. O’Donnell, P. McCloskey, and M. Duffy, “Packaging and integration technologies for future high-frequency power supplies,” *IEEE transactions on industrial Electronics*, vol. 51, no. 6, pp. 1305 – 1312, 2004.
- [7] J. W. Kolar, “What are the big challenges in power electronics?” in *Proceedings of CIPS*, Nüremberg, 2014.
- [8] S. Seal and H. A. Mantooth, “High performance silicon carbide power packaging—past trends, present practices, and future directions,” *Energies*, vol. 10, no. 3, 2017. [Online]. Available: <http://www.mdpi.com/1996-1073/10/3/341/htm>

- [9] A. Ostmann, "Evolution and future of embedding technology," in *IMAPS/NMI workshop "disappearing die – embed your chips"*, 2016.
- [10] E. Waffenschmidt, "Design and application of thin, planar magnetic components for embedded passives integrated circuits," in *Proceedings of the 35th Power Electronic Specialists Conference (PESC'04)*, 2004, pp. 4546–4552.
- [11] E. Hoene, A. Ostmann, B. T. Lai, C. Markczok, A. Müsing, and J. W. Kolar, "Ultra-Low-Inductance Power Module for Fast Switching Semiconductors," in *Proc. PCIM Europe*, 2013, pp. 1–8.
- [12] L. Luke, Ed., *The PCB Magazine*, vol. 4, no. 7, jul 2014. [Online]. Available: thepcbmagazine.com
- [13] T. Hofmann, "Practical experience manufacturing PCBs with embedded active and passive devices," *The PCB Magazine*, 2011.
- [14] P. Palm, J. Moisala, A. Kivikero, R. Tuominen, and A. Iihola, "Embedding active components inside printed circuit board (PCB) - a solution for miniaturization of electronics," in *Proceedings. International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces, 2005.*, March 2005, pp. 1–4.
- [15] E. Waffenschmidt, B. Ackermann, and J. A. Ferreira, "Design Method and Material Technologies for Passives in Printed Circuit Board Embedded Circuits," *IEEE Transactions on Power Electronics*, vol. 20, no. 3, pp. 576–584, May 2005.
- [16] K. Klein, E. Hoene, and K.-D. Lang, "Packages for Fast Switching HV GaN Power Devices," in *Proceedings of the PCIM 2014 conference*, 2014.
- [17] E. Hoene, "Ultra Low Inductance Package for SiC," in *ECPE workshop on power boards*. ECPE, 2012.
- [18] K. Essig, "Enhancing power modules efficiency by chip embedding," in *IMAPS/NMI workshop "disappearing die – embed your chips"*, 2016.
- [19] E. de Jong, B. Ferreira, and P. Bauer, "Toward the Next Level of PCB Usage in Power Electronic Converters," *Power Electronics, IEEE Transactions on*, vol. 23, no. 6, pp. 3151–3163, 2008.
- [20] A. B. Lostetter, F. Barlow, and A. Elshabini, "An overview to integrated power module design for high power electronics packaging," *Microelectronics reliability*, vol. 40, pp. 365–379, 2000. [Online]. Available: www.elsevier.com/locate/microrel
- [21] S. Dieckerhoff, T. Kirfe, T. Wernicke, C. Kallmayer, A. Ostmann, E. Jung, B. Wunderle, and H. Reichl, "Electric Characteristics of Planar Interconnect Technologies for Power MOSFETs," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, Jun. 2007, pp. 1036–1042.
- [22] M. Zurnaci, "MiniSKiiP IPM - Intelligent Power Modules Family - Technical Explanations," Semikron, Tech. Rep., Aug. 2012. [Online]. Available: http://www.semikron.com/skcompub/en/MiniSKiiP_IPM.pdf
- [23] P. Beckedahl, S. Bütow, A. Maul, M. Roebnitz, and M. Spang, "400A, 1200V SiC power module with 1nH commutation inductance," in *Proceedings of the Conference on Integrated Power Systems (CIPS)*, nuremberg, mar 2016.
- [24] J.-L. Marchesini, P.-O. Jeannin, Y. Avenas, J. Delaine, C. Buttay, and R. Riva, "Implementation and Switching Behavior of a PCB-DBC IGBT Module Based on the Power Chip-on-Chip 3D Concept," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 362–370, Aug. 2017. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-01373011>
- [25] B. Ferreira, "PCB Integration Technology Overview," in *ECPE Seminar "Power PCBs and Busbars"*, Delft, 2008.
- [26] A. Alderman, L. Burgyan, B. Narveson, and E. Parker, "3-D Embedded Packaging Technology," *IEEE Power Electronics Magazine*, pp. 30–39, dec 2015.
- [27] M. Morianz and H. Stahr, "Embedded power electronics on the way to be launched," in *Proceedings of the European Microelectronics Packaging Conference (EMPC)*. Friedrichshafen, Germany: IMAPS, 2015. [Online]. Available: <http://ieeexplore.ieee.org/document/7390738/>
- [28] Dupont., "Dupont intera embedded passives materials – intera HK04 planar capacitor laminate," Dupont, Tech. Rep., 2007.
- [29] M. Ali, E. Labouré, F. Costa, and B. Revol, "Design of a hybrid integrated EMC filter for a DC–DC power converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4380–4390, 2012.
- [30] R. Caillaud, C. Buttay, J. Le Lesle, F. Morel, R. Mrad, N. Degrenne, S. Mollov, and C. Combettes, "High power PCB-embedded inductors based on ferrite powder," in *5th Micro/Nano-Electronics, packaging and assembling, design and manufacturing forum MiNaPAD 2017*. Grenoble, France: IMAPS, May 2017. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-01535727>
- [31] A. Kugler, M. Koyuncu, A. Zimmermann, and J. Kostelnik, "Chip Embedding in Laminates," in *Ultra-thin Chip Technology and Applications*, J. Burghartz, Ed. Springer New York, 2011, pp. 159–165.
- [32] A. B. Sharma, D. Paul, M. Kreck, Y. Rahmoun, P. Anders, M. Gruber, and T. Huesgen, "PCB embedded power package with reinforced top-side chip contacts," in *2016 6th Electronic System-Integration Technology Conference (ESTC)*, Sept 2016, pp. 1–5.
- [33] Y. Pascal, A. Amar, D. Labrousse, M. Petit, S. Lefebvre, and F. Costa, "Using Laminated Metal Foam as the Top-Side Contact of a PCB-Embedded Power Die," *IEEE Electron Device Letters*, 2017. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-01582268>
- [34] C. Yu, C. Buttay, E. Labouré, V. Bley, C. Combettes, and G. Brillat, "Comparison of topside contact layouts for power dies embedded in PCB," in *Electronics System Technology Integration Conference*. Grenoble, France: IMAPS, Sep. 2016. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-01373042>
- [35] A. Ostmann, L. Boettcher, D. Manassis, S. Karaszkievicz, and K.-D. Lang, "Power modules with embedded components," in *Microelectronics Packaging Conference (EMPC) , 2013 European*, Sep. 2013, pp. 1–4.
- [36] G. Regnat, P.-O. Jeannin, G. Lefevre, J. Ewanchuk, D. Frey, S. Mollov, and J.-P. Ferrieux, "Silicon carbide power chip on chip module based on embedded die technology with paralleled dies," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*. IEEE, 2015, pp. 4913–4919.
- [37] C. Yu, C. Buttay, E. Labouré, V. Bley, and C. Combettes, "Highly integrated power electronic converters using active devices embedded in printed-circuit board," in *4th Micro/Nano-Electronics, packaging and assembling, design and manufacturing forum MiNaPAD 2015*. Grenoble, France: IMAPS, Apr. 2015. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-01197043>
- [38] M. Mueller and J. Franke, "Highly efficient and flexible plasma based copper coating process for the manufacture of direct metallized mechatronic devices," in *2016 IEEE 18th Electronics Packaging Technology Conference (EPTC)*, Nov 2016, pp. 365–369.
- [39] R. Randoll, W. Wondrak, and A. Schletz, "Lifetime and manufacturability of integrated power electronics," *Microelectronics Reliability*, vol. 64, pp. 513 – 518, 2016, proceedings of the 27th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S0026271416301767>
- [40] J. Andreasakis, "Embedded Capacitors," Oak-Mitsui Technologies, presentation, Nov. 2005. [Online]. Available: http://www.laocsmta.org/archive/Embedded_Capacitance_Presentation.pdf
- [41] D. Bortis, D. Neumayr, and J. W. Kolar, " $\eta\rho$ -Pareto Optimization and Comparative Evaluation of Inverter Concepts considered for the GOOGLE Little Box Challenge," in *Proceedings of the 17th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2016)*, 2016, p. 11 p.
- [42] Q. Chen, Z. Gong, X. Yang, Z. Wang, and L. Zhang, "Design considerations for passive substrate with ferrite materials embedded in printed circuit board (PCB)," in *2007 IEEE Power Electronics Specialists Conference*, June 2007, pp. 1043–1047.
- [43] Y. Kondo, Y. Yazaki, M. Sonehara, T. Sato, T. Watanabe, Y. Seino, N. Matsushita, T. Fujii, K. Kobayashi, H. Shimizu *et al.*, "Embedded planar power inductor technology for package-level DC power grid," in *Electronics Packaging and iMAPS All Asia Conference (ICEP-IACC), 2015 International Conference on*. IEEE, 2015, pp. 814–817.
- [44] Q. Li, M. Lim, J. Sun, A. Ball, Y. Ying, F. C. Lee, and K. D. T. Ngo, "Technology roadmap for high frequency integrated DC-DC converter," in *2009 IEEE 6th International Power Electronics and Motion Control Conference*, May 2009, pp. 1–8.
- [45] B. Sun, R. Burgos, D. Boroyevich, R. Perrin, C. Buttay, B. Allard, N. Quentin, and M. Ali, "Two Comparison-Alternative High Temperature PCB-Embedded Transformer Designs for a 2 W Gate Driver Power Supply," in *IEEE Energy Conversion Congress and Expo (ECCE 2016)*. Milwaukee, WI, United States: IEEE, Sep. 2016. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-01373036>
- [46] D. H. Bang and J. Y. Park, "Ni-Zn ferrite screen printed power inductors for compact dc-dc power converter applications," *IEEE Transactions on Magnetics*, vol. 45, no. 6, pp. 2762–2765, June 2009.
- [47] S. Ji, D. Reusch, and F. C. Lee, "High-Frequency High Power Density 3-D Integrated Gallium-Nitride-Based Point of Load Module Design," *transactions on power electronics*, vol. 28, no. 9, pp. 4216–4226, 2013.

- [48] W. Zhang, Y. Su, M. Mu, D. J. Gilham, Q. Li, and F. C. Lee, "High-density integration of high-frequency high-current point-of-load (POL) modules with planar inductors," *IEEE transactions on Power Electronics*, vol. 30, no. 3, pp. 1421–1431, Mar. 2015.
- [49] C. Marxgut, J. Muhlethaler, F. Krismer, and J. W. Kolar, "Multiobjective optimization of ultraflat magnetic components with PCB-integrated core," *IEEE Transactions on Power Electronics*, vol. 28, no. 7, pp. 3591–3602, 2013.
- [50] R. Caillaud, C. Buttay, R. Mrad, J. Le Lesle, F. Morel, N. Degrenne, S. Mollov, and C. Martin, "Design, manufacturing and characterization of printed circuit board embedded inductors for power applications," in *19th International Conference on Industrial Technology (ICIT 2018)*, 2018.
- [51] P. Goldman, Ed., *The PCB Magazine*, vol. 7, no. 6, jun 2017. [Online]. Available: <http://pcb.icconnect007.com/mags/pdf.php?id=104670>
- [52] M. Brizoux, A. Grivon, W. Maia Filho, E. Monier-Vinard, J. Stahr, and M. Morianz, "Industrial PCB development using embedded passive & active discrete chips focused on process and DfR1," *PLUS. Produktion von Leiterplatten und Systemen*, vol. 12, no. 11, p. 2670, 2010.
- [53] W. W. Wits, "Flat miniature heat pipes in printed circuit boards," in *ECPE Workshop on Advanced Cooling*. Delft: ECPE, 11 2008.
- [54] J. S. de Sousa, P. Fulmek, M. Unger, P. Haumer, J. Nicolics, M. A. Ras, and D. May, "Enhanced in-plane heat transport in embedded mini heat pipes PCB," *International Symposium on Microelectronics*, vol. 2017, no. 1, pp. 000130–000134, 2017. [Online]. Available: https://doi.org/10.4071/isom-2017-TP51_001
- [55] R. Randoll, M. Asef, W. Wondrak, L. Böttcher, and A. Schletz, "Characteristics and aging of PCB embedded power electronics," *Microelectronics Reliability*, vol. 55, no. 9, pp. 1634 – 1639, 2015, proceedings of the 26th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S002627141500164X>
- [56] H. Stahr, M. Unger, J. Nicolics, M. Morianz, S. Gross, and L. Böttcher, "Thermal benchmark of a classic and novel embedded high-power 3-phase inverter bridge," in *2016 6th Electronic System-Integration Technology Conference (ESTC)*, Sept 2016, pp. 1–6.
- [57] L. Tinschert, M. Hernes, and J. Lutz, "Improving the short circuit ruggedness of IGBTs," *Microelectronics Reliability*, vol. 64, no. Supplement C, pp. 519 – 523, 2016, proceedings of the 27th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S0026271416302840>
- [58] G. Lefevre, N. Degrenne, and S. Mollov, "Thermal management of a low-cost 2kW solar inverter," in *2014 16th European Conference on Power Electronics and Applications*, Aug 2014, pp. 1–10.
- [59] C. Zweben, "Thermal Materials Solve Power Electronics Challenges," *Power Electronics Technology*, pp. 40–47, Feb. 2006. [Online]. Available: <http://powerelectronics.com/thermal-management/thermal-materials-solve-power-electronics-challenges>
- [60] J. S. de Sousa, P. Fulmek, M. Unger, P. Haumer, and J. Nicolics, "Enhanced heat transport in printed circuit boards via passive components embedding," in *2017 IMAPS Nordic Conference on Microelectronics Packaging (NordPac)*, June 2017, pp. 84–89.
- [61] L.-A. Liew, C.-Y. Lin, R. Lewis, S. Song, Q. Li, R. Yang, and Y. Lee, "Flexible thermal ground planes fabricated with printed circuit board technology," *Journal of Electronic Packaging*, vol. 139, no. 1, pp. 011003–011003–10, 2017.
- [62] B. Heinz, "Heat management of circuit boards," *Wurth Elektronik*, Tech. Rep., mar 2011. [Online]. Available: www.we-online.com
- [63] N. Degrenne and S. Mollov, "A low-cost and high-performance thermal interface assembly between printed circuit board and heat-sink," in *Proceedings of the European European Conference on Power Electronics and Applications (EPE-ECCE 2017)*, Warsaw, Poland, sep 2017.
- [64] M. Brizoux, A. Grivon, W. Maia Filho *et al.*, "Development of a Design & Manufacturing Environment for Reliable and Cost-Effective PCB Embedding Technology," in *IPC Apex Expo conference*. IPC, 2011. [Online]. Available: <https://www.smtnet.com/library/files/upload/embedded-chips.pdf>
- [65] D. Shaddock and L. Yin, "Reliability of high temperature laminates," in *International Conference and Exhibition on High Temperature Electronics Network (HiTEN)*. International Microelectronics Assembly and Packaging Society, 2015.
- [66] O. Avino-Salvado, W. Sabbah, C. Buttay, H. Morel, and P. Bevilacqua, "Evaluation of printed-circuit boards materials for high temperature operation," in *International Conference and Exhibition on High Temperature Electronics Network (HiTEN 2017)*, ser. Proceedings of the High Temperature Electronics Network (HiTEN 2017). Cambridge, United Kingdom: IMAPS, Jul. 2017. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-01565131>
- [67] Panasonic, "R-1755v laminage specification sheet," Panasonic Electric Works Electronic Materials Europe GmbH, Tech. Rep., 2007.
- [68] J. Franklin, J. Bultitude, J. McConnell, R. Phillips, M. Laps, P. John, and T. Ashburn, "High capacitance stacked multi-layer ceramic capacitors for power supplies," in *CARTS 2010 Conference Proceedings*, New Orleans, USA, apr 2010.
- [69] R. Perrin, B. Allard, C. Buttay, N. Quentin, W. Zhang, R. Burgos, D. Boroyevich, P. Preciat, and D. Martineau, "2 MHz high-density integrated power supply for gate driver in high-temperature applications," in *Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, United States, Mar. 2016. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-01372141>
- [70] J. W. Kolar and *et al.*, "Approaches to overcome the Google/IEEE Little Box Challenges," *ETH Zurich*, Tech. Rep., 2015.
- [71] L. Kerachev, A. Andreta, Y. Lembeye, and J.-C. Créber, "A new step towards the power electronics design automation," in *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. Nuremberg: VDE Verlag, May 2017, pp. 1232–1239.
- [72] D. Boroyevich, F. C. Lee, J. D. v. Wyk, G. Q. Lu, E. P. Scott, M. Xu, R. Burgos, F. Wang, T. M. Jahns, T. A. Lipo, R. D. Lorenz, and T. P. Chow, "IPEM-based power electronics system integration," in *5th International Conference on Integrated Power Electronics Systems*, March 2008, pp. 1–10. [Online]. Available: <http://ieeexplore.ieee.org/abstract/document/5755711/>
- [73] P. Solomalala, J. Saiz, A. Lafosse, M. Mermet-Guyennet, A. Castellazzi, X. Chauffeur, and J.-P. Fredin, "Multi-domain simulation platform for virtual prototyping of integrated power systems," in *Power Electronics and Applications, 2007 European Conference on*, Sep. 2007, pp. 1–10.
- [74] J. Biela, J. Kolar, A. Stupar, U. Drofenik, and A. Muesing, "Towards Virtual Prototyping and Comprehensive Multi-Objective Optimisation in Power Electronics," in *Power Conversion and Intelligent Motion Conference (PCIM 2010)*, Nuremberg, Germany, May 2010, p. 23.
- [75] P. L. Evans, A. Castellazzi, and C. M. Johnson, "Automated fast extraction of compact thermal models for power electronic modules," *IEEE transactions on power electronics*, vol. 28, no. 10, pp. 4791–4802, 10 2013.
- [76] J. W. Kolar, J. Biela, T. Friedli, and U. Badstuebner, "Performance trends and limitations of power electronic systems," in *Proceedings of the Conference on Integrated Power Systems (CIPS)*, 2010.
- [77] K. Raggl, T. Nussbaumer, G. Doerig, J. Biela, and J. W. Kolar, "Comprehensive Design and Optimization of a High-Power-Density Single-Phase Boost PFC," *IEEE transactions on industrial Electronics*, vol. 56, no. 7, pp. 2574–2587, Jul. 2009.
- [78] R. Caillaud, C. Buttay, R. Mrad, J. Le Lesle, F. Morel, N. Degrenne, and S. Mollov, "Comparison of planar and toroidal PCB integrated inductors for a multi-cellular 3.3 kW PFC," in *Integrated Power Packaging (IWIPP), 2017 IEEE International Workshop On*. Delft, Netherlands: IEEE, Apr. 2017, pp. 1–5. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-01535721>
- [79] D. Cottet, "Industry perspective on multi domain simulation and virtual prototyping," in *Proceedings of Control and Modeling for Power Electronics (2008), COMPEL 2008, 11th Workshop on*. IEEE, 2008.
- [80] S. Pietranico, S. Pommier, S. Lefebvre, and S. Patoatto, "Thermal fatigue and failure of electronic power device substrates," *International Journal of Fatigue*, vol. 31, no. 11, pp. 1911–1920, 2009.
- [81] A. Ben Kabaar, C. Buttay, O. Dezellus, R. Estevez, A. Gravouil, and L. Gremillard, "Characterization of materials and their interfaces in a direct bonded copper substrate for power electronics applications," *Microelectronics Reliability*, 2017. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-01541230>
- [82] T. Ericson, N. Hingorani, and Y. Khersonsky, "PEBB - power electronics building blocks from concept to reality," in *2006 Record of Conference Papers - IEEE Industry Applications Society 53rd Annual Petroleum and Chemical Industry Conference*, Sept 2006, pp. 1–7.
- [83] C. Mead and L. Conway, *Introduction to VLSI systems*. Addison-Wesley Reading, MA, 1980, vol. 1080.