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To cite this version:

Oriol Aviño Salvado, C. Cheng, Cyril Buttay, Hervé Morel, D Labrousse, et al.. SiC MOSFETs robustness for diode-less applications. EPE Journal - European Power Electronics and Drives, 2018, pp.1 - 8. 10.1080/09398368.2018.1456836 . hal-01844980

HAL Id: hal-01844980

https://hal.science/hal-01844980v1

Submitted on 19 Jul 2018

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SiC MOSFETs Robustness for Diode-less Applications

O. Avino-Salvado[a], C. Cheng[b], C. Buttay[a], H. Morel[a], D. Labrousse[b], S. Lefebvre[b], M. Ali[a]

[a]Univ Lyon, INSA-Lyon, CNRS, Laboratoire Ampère UMR 5005, F-69621, Lyon, France
[b]CNRS, SATIE UMR 8029, F-94235 Cachan, France

ARTICLE HISTORY
Compiled March 12, 2018

Abstract
Silicon-Carbide (SiC) technology presents several advantages over silicon for power electronics applications, such as lower losses. However, SiC technology is not totally mature, and some reliability problems remain. This paper studies the robustness of SiC MOSFETs in the case of diode-less applications and the associated phenomena, such as gate oxide degradation. Several devices were stressed under conditions of inductive switching and inverse current conduction. These devices were periodically characterised. As a result, a threshold voltage shift was observed in the MOSFET, with a dependence on the duty cycle of the transistor. On the contrary, no significant degradation of the internal P-N junction of the transistor was observed.

KEYWORDS
MOSFET, Silicon Carbide (SiC), reliability, robustness, threshold voltage, intrinsic diode, diode-less, oxide traps.

1. Introduction

Despite the fact that SiC has been known since the end of the nineteen century [1], its use as a semiconductor is relatively recent [2, 3]. The firsts SiC diodes were commercialized in 2001 [4] and it was not before 2007 and 2011 that the first commercial JFET and MOSFET devices were introduced. Among the advantages of SiC versus Si [5], there are its breakdown electrical field (3-5 MV/cm) which is about ten times higher than that of Silicon and a band gap about three times higher (3.26 eV vs 1.11 eV). Thermal performances are also better: SiC has a thermal conductivity nearly three times higher (4.9 $W/cm.K$ vs 1.5 $W/cm.K$), and an intrinsic resistance much lower than Si (0.3 $m\Omega.cm^2$ vs 400 $m\Omega.cm^2$ for a 1200 V breakdown voltage, at room temperature).

As a result, SiC devices are especially attractive for power applications. They allow important loss reduction, which, associated with better thermal performances, may yield to a reduction of the system dimensions. This may allow to replace the current IGBT devices by SiC MOSFET or JFET devices in high power, volume-constrained applications such as aeronautics or railways.

However attractive the material is, the commercial development of SiC devices faces technological challenges about defect elimination. Among them, dislocation issues [6]

CONTACT H. Morel. Email: herve.morel@insa-lyon.fr

and micropipes [7] have limited for a long time the forward-blocking capacity of SiC devices at high voltages [8], one of SiC most promising applications. Besides, the mobility on the SiC MOSFETs channel is limited by defects induced by traps located near the conduction band [9], as well as trapped charges which reduces coulomb scattering mobility of carriers on the inversion layer [10].

Although manufacturers have considerably minimised these defects for the last commercialised SiC devices, these are not fully controlled yet and some reliability problems remain [11]: robustness under short-circuit conditions [12] as well as gate oxide reliability and gate bias instability [13, 14] remain some of the principal reliability problems on SiC MOSFETs[15]. Finally, the degradation of the internal body diode of SiC MOSFET was reported in [16, 17].

While SiC BJT or JFET have specific driving requirements, which results in particular driving circuits [18], SiC MOSFETs are comparable to the classic Si MOSFETs or IGBTs. This makes SiC MOSFETs especially attractive, as they can be driven with standard driver circuits. SiC MOSFETs simply need a negative gate voltage in the off-state (for dV/dt immunity) and a relatively high gate voltage in the on-state (about 20 V).

In this paper, the robustness of the internal diode of SiC MOSFETs is assessed under realistic operating conditions. This work is oriented towards aeronautical applications (inductive switching and a bus voltage of 540 V, corresponding to the future aircraft HVDC network). An example of such application is an inverter where the transistors are mounted without antiparallel diodes. Diode-less converters require fewer components, hence a more compact and cheaper system.

The objective is to study whether current commercial devices could be used in "diode-less" applications, assessing their reliability. Two parameters are specially interesting. A forward voltage drift on the diode would indicate the presence of stacking faults in the substrate. Also, in comparable conditions, [17] reported a drift in the gate threshold voltage of some MOSFETs. This has consequences on the gate drive circuit design and eventually on the on-state resistance of the transistor.

2. Analysis of SiC MOSFET robustness in Chopper Mode

The SiC MOSFET structure is comparable to that of a Silicon MOSFET. Figure 1 shows a typical MOSFET structure and the current paths I_{CH} when the current flows through the channel and I_{BD} when it flows through the internal diode.

The main robustness issues of SiC MOSFETs in chopper mode [17] are the threshold voltage shift and the degradation of the P-N junction [19] if the internal diode is involved. Recent publication [20] shows a similar test to that presented in this paper, using an inverter and conducting through the internal diode during dead-times. However, it focuses on forward voltage and leakage current. Present work bases its originality on the threshold voltage drift at different stress conditions, ever more constraining than used in [20].

Lelis et al. [21] suggested that the threshold voltage instability is related to the activation of near-interfacial oxide traps, or even to the formation of additional interface charges, which would modify the threshold voltage. Both mechanisms could be related to carrier injection in the oxide. Principal phenomena causing carrier injection [22, 23] are: injection by tunnel effect, Fowler-Nordheim injection and hot carrier injection.

Standard JEDEC tests [24] HTGB (High Temperature Gate Bias) and HTRB (High Temperature Reverse Bias), see table 1, are used to assess device reliability. These tests

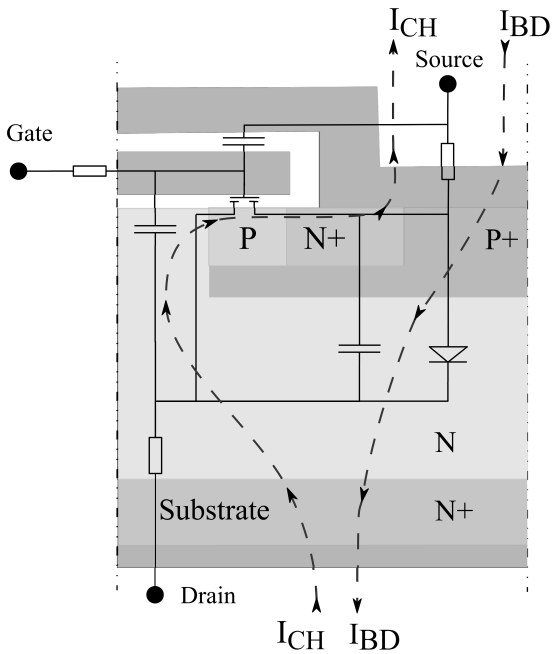

Figure 1.: Internal structure of a SiC MOSFET and current paths I_{CH} and I_{BD}

were defined and adjusted for Silicon devices. An additional test, called "HTGS" (High Temperature Gate Switching), is also used [14, 25]. Although this test reproduces more realistic conditions of use, it is not a JEDEC standard.

Recent publications [14] highlighted an important threshold voltage drift for HTGB tests performed at $V_{GS} = 20\ V$. For "HTGS" tests [14], with pulsed excitation and $V_{GS} = +20/-5\ V$, threshold voltage drift is significantly lower. Therefore, polarity changes on the gate seem to induce different effects than the static conditions used for JEDEC tests.

Regarding the P-N junction, the degradations which may occur when the internal diode is used are attributed to the formation of basal plane dislocations. This issue is associated with the SiC epitaxial growth [26, 27].

A commonly used solution to avoid any P-N junction degradation is to use a Schottky diode in an antiparallel configuration. This solution also offers advantages such as faster recovery time and lower losses. However, it has the downside of requiring more components. An intermediate solution is a structure integrating a Shottky diode in the MOSFET die [19].

Acronym	Test full name	Test Conditions	Standard ref.	Performed here?
HTGB	High Temperature Gate Bias	$T = T_{max}$ $V_{GS} = +V_{GSmax}/-V_{GSmin}$ V_{GS} cst $V_{DS} = 0\ V$	JESD22-A108D	No
HTRB	High Temperature Reverse Bias	$T = T_{max}$ $V_{GSmin} < V_{GS} < 0\ V$ $V_{DS} = V_{BR}$ or near	JESD22-A108D	Yes see Fig.3
HTGS	High Temperature Gate Switch-ing	$T_{amb} = T_{max}$ $V_{GS} = +V_{GSmax}/-V_{GSmin}$ or near Pulsed excitation Frequence and Duty Cycle no explicitly defined $V_{DS} = 0\ V$	No standard test	No
CMB	Chopper Mode Bias	$T = T_{max}$ $V_{GS} = -8\ V$ $V_{DS} = 540\ V$ $f = 20\ kHz$ $D = 0.5$	No standard Test	Yes, see Fig.2

Table 1.: Tests used on gate bias and threshold voltage instability

3. Experimental Methodology

The aim of this experiment is to study the degradation of the P-N junction, as well as the drift in threshold voltage for SiC MOSFETs. Devices under test (DUT) are required to conduct in reverse mode and under inductive switching conditions. A specific chopper-mode bias (CMB see table1) test setup has been designed and built.

This CMB test setup is based on a back-to-back structure composed by a Buck converter followed by a boost converter. The current in the boost converter is controlled and set at 10 A. This imposes the same current to the buck inductor, and therefore to the DUT when it is involved. The input voltage is $V_{DD} = 540\ V$. Figure 2 shows a schematic of the Buck converter, with the boost converter represented as a current source.

The devices under tests are Wolfspeed C2M008012D SiC MOSFETs, 1200 V, 80 $m\Omega$, in a TO-247 package. It is worth noting that new devices are used for each test. Devices are attached to a temperature-regulated hot plate to operate near their maximum junction temperature of 150 °C [28]. The experimental protocols, including the methodology used to estimate the junction temperature are presented in the following sections. The test results are presented in section 4.

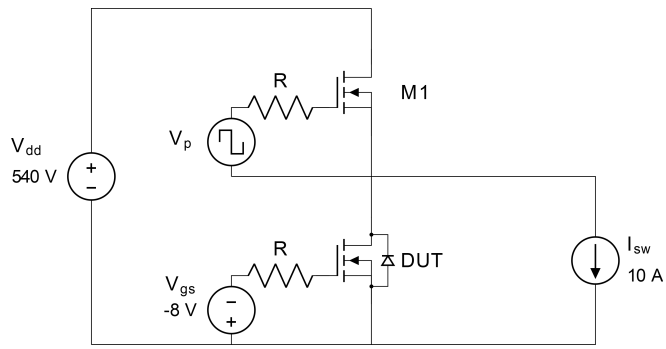

Figure 2.: CMB test schematic

3.1. *Junction temperature estimation*

Estimation of junction temperature using thermosensible parameters has been a largely discussed subject in the literature [29, 30]. As a fine estimation of junction temperature is important in order to test the devices without exceeding their maximal junction temperature, a method for junction temperature estimation is presented.

Junction temperature estimation is performed in steady state using equation 1 and the saturation current I_{SAT} as a thermosensible parameter [30]. T_J and T_S are respectively the junction and heat-sink temperature, P_D is the power dissipated by the device under test, and R_{JC} and R_{CS} are respectively the junction-case and case-sink thermal resistances.

$$T_S = T_J - P_D(R_{JC} + R_{CS}) \tag{1}$$

T_S is regulated at a constant value, and $R_{JC} = 0.65$ °C·W [28].

To determine R_{CS}, the current I_{SAT} was characterized (using an Agilent B1505B curve tracer in pulsed mode and a Thermonics T-2500E/300 thermal conditioner) over a temperature range of 60 °C and 150 °C (ΔT=10 °C). The resulting I_{SAT} characteristic can be fitted using a second order polynomial by equation 2 for an operating point located in the saturation region ($V_{GS} = 6\ V,\ V_{DS} = 8\ V$):

$$I_{SAT}\Big|_{\substack{V_{GS}=6\ V \\ V_{DS}=8\ V}} = 6.10^{-5}\ T^2 + 6.6.10^{-3}\ T + 0.5536 \tag{2}$$

Once the MOSFET was characterized, it was assembled on the hot plate together with a Thermal Interface Material (TIM) layer (SIL-K10 from Bergquist). The device was excited at the same operating point used for the characterization ($V_{GS} = 6\ V,\ V_{DS} = 8\ V$). Using eq. (2), it was then possible to calculate the junction temperature from the measured I_{SAT} value at equilibrium ($I_{SAT} = 2.11\ A$, corresponding to a junction temperature $T_J = 117$ °C). As dissipated power is the product of I_{SAT} and V_{DS}, $T_S = 80$ °C, and $R_{JC} = 0.65$ °C, R_{CS} was calculated using the equation 3.

$$R_{CS} = \frac{T_J - T_S}{V_{DS} \cdot I_{SAT}} - R_{JC} = \frac{117 - 80}{16.88} - 0.65 = 1.55\ °C/W \tag{3}$$

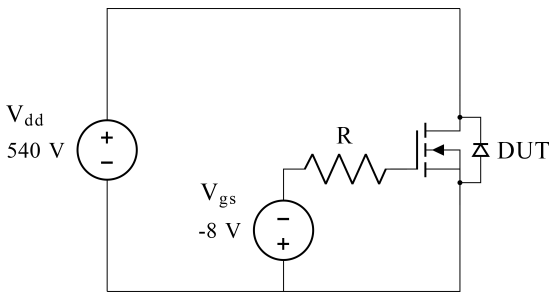

Figure 3.: HTRB test schematic

Switching losses on the DUT could be neglected if the MOSFET channel remains always blocked (see Fig.2), as these are not important for the internal diode of a SiC MOSFET [31]. The forward voltage drop of the diode at the CMB operating point (T_J=150 °C, $V_{GS} = -8\ V$,I_{BD}=10 A) was measured as V_F=3.84 V. As the chosen inductance L=80 mH results in a low current ripple, the diode current is assumed to have a square waveform. Then, the power dissipated by the DUT can be calculated using equation 4. Finally, using equation 1 and the values calculated above, one can estimate that a junction temperature T_J = 150 °C is achieved for a heat-sink temperature of T_S=108 °C (eq. 5).

$$P_D = V_{Frms}.I_{rms} = \frac{3.84\ V \cdot 10\ A}{2} = 19.2\ W \tag{4}$$

$$T_S = 150 - 19.2(0.65 + 1.55) = 108°C \tag{5}$$

Because of the thermal resistance of the TIM layer SIL-K10 presents some incertitudes, as it depends on the temperature and applied pressure, an uncertainty of ±6 °C is assumed for T_J. This ±6 °C uncertainty is considered to set the heatsink at a temperature of T_S=102 °C which garantees T_J < 150 °C. This error has been determined after a set of tests at different power levels and temperature.

3.2. *HTRB Test*

In the literature, several studies based on JEDEC tests (static conditions of operation) report a threshold voltage drift [13].

For the sake of comparison, a standard test (HTRB, see fig. 3) is performed on 10 devices. Test conditions are the same as for the CMB test bench ($V_{DD} = 540\ V$, $V_{GS} = -8\ V, T_J = 150$ °C). The test was run for 400 hours.

Devices are initially characterized and placed in a forced-convection oven (no power is dissipated by the devices during the HTRB test, so no heatsink is necessary). They were characterized every 100 hours (and after the first 10 hours). Characterizations are realized at room temperature, using an Agilent B1505B curve tracer. A long dwell time of 1 hour is used to ensure stability of the temperature.

Obtained results are compared in section 4.1 to the results presented in the literature for similar tests. Also, they are compared to the threshold voltage drift observed for the CMB test bench.

$D_{M1}(\%)$	$D_{DUT}(\%)$	Conduction time of DUT intrinsic diode(%)	Conduction time of DUT channel(%)
50 (%)	0 (%)	50 (%)	0 (%)
45 (%)	5 (%)	50 (%)	5 (%)
35 (%)	15 (%)	50 (%)	15 (%)
13.4 (%)	85 (%)	1.6 (%)	85 (%)

Table 2.: Configurations used for the CMB test with partial channel conduction.

3.3. *CMB Test — Channel Always Blocked*

The aim of this test is to assess an eventual degradation of the P-N junction. The test is done at $T_J = 150$ °C. The gate voltage is fixed at a constant voltage $V_{GS} = -8\ V$, forcing the MOSFET in the off-state, and only allowing the forward current to flow through the intrinsic diode. It is worth noting that the datasheets [28, 32] mentions an absolute minimal $V_{GS} = -10\ V$. However, the latest datasheet [32] version recommends a $V_{GS} = -5\ V$ for applications involving the internal diode. Nevertheless, this is not mandatory and the absolute minimal V_{GS} level remains -10 V.

A complete characterization at room temperature of the devices under test was realized every 20 hours after a cooling down time of 1 hour. Devices were also characterized after the first 10 hours. Total test duration was 100 hours. As a threshold voltage drift was observed, the test was prolonged up to 400 hours for four components.

3.4. *CMB Test — Partial Channel Conduction*

In the section above, the MOSFET is always in the blocking state, using only the intrinsic diode. This is not representative of most application cases, where the diode is using during the dead-time, before the MOSFET channel is turned on. Another test is therefore proposed in order to study the impact of the diode duty cycle on the DUT degradation, particularly on the threshold voltage drift. The voltage applied to the gate is $V_{GS} = +20/-8\ V$.

In order to submit the internal diode to the same stress as in the test presented in section 3.3, the duty cycle of device M1 – see fig. 2 – is varied. Table 2 shows the duty cycle (D) for devices M1 and DUT. The DUT conduction time is divided between intrinsic diode and channel conduction durations and expressed as a percentage. Obviously, there is one case where is not possible to have the current flowing though the intrinsic diode for 50% of the switching period (when D=0.85 %). In this case the internal diode is only solicited during the dead-time.

4. Experimental Results

In this section, the results obtained using the test setup described above are presented.

4.1. *HTRB Test*

The HTRB test – see fig. 3 – was performed on 10 devices at 150 °C. Fig. 4 presents the normalised mean value of the threshold voltage of tested devices. It is observed

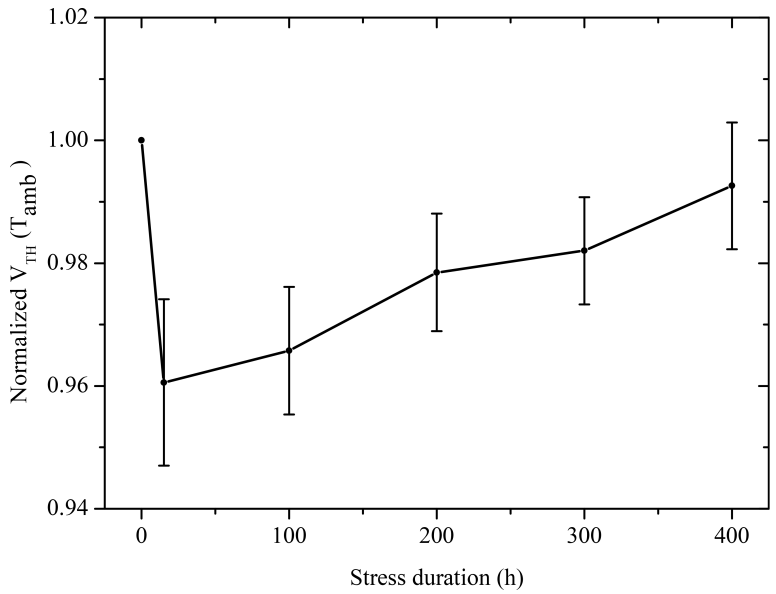

Figure 4.: HTRB test results on 10 devices. Characterized at ambient temperature, $I_{DS} = 100\ \mu A$, $V_{DS} = 1\ V$). Indicated value is the average of normalized threshold voltage.

a drop in the threshold voltage after the first 10 hours of operation, followed by a slow recovery to the initial value. However, the initial V_{TH} drop is small (< 5 %). These results are reassuring, as previous articles [13, 17] reported much larger V_{TH} drifts. Nevertheless, devices used on these publications could be of older generations. Particularly, in [13], the V_{TH} drift is larger than 20 % compared to the initial value for an HTGB test performed at $V_{GS} = -5\ V$. In the case where $V_{GS} = -10\ V$, V_{TH} drops dramatically according to [17]. It is also worth noting that, contrary to our configuration, in these experiments the drain and source terminals of the DUT are connected together ($V_{DS} = 0$) and it might have an effect on the threshold drift.

4.2. *CMB Test — Channel Always Blocked*

This CMB test was performed on 10 devices. Unfortunately, for one of these devices an important threshold voltage drop was detected after 10 hours of operation ($V_{TH} = 0.47\ V$). The gate leakage current of this device was acceptable (Igs=500 pA at $V_{GS} = 22\ V$), but it is necessary to notice that its threshold voltage was in the lower range allowed by the manufacturer [28] ($V_{TH} = 1.97\ V$ at $V_{DS} = 1\ V$, $I_{DS} = 100\ \mu A$) when it was characterised initially at room temperature. Therefore, this device was removed from the test, and the final group under study is composed of nine samples only.

Fig. 5 shows the evolution of the normalized value of V_{TH}, $R_{DS_{on}}$, and V_F. There is a noticeable drop in V_{TH} (about 20 % after 100 hours of operation). However, the degradation rate decreases over time. It is therefore necessary to continue the tests over a longer period of time in order to assess if there is some stabilization.

In the same figure, one can observe that the forward voltage drop of the intrinsic diode remains constant. This suggests that there is no noticeable degradation of the P-N junction, contrary to previously reported in the literature [17, 19]. On-state resistance of the MOSFET also remains stable, even if a larger experimental scattering is observed on this parameter among the samples.

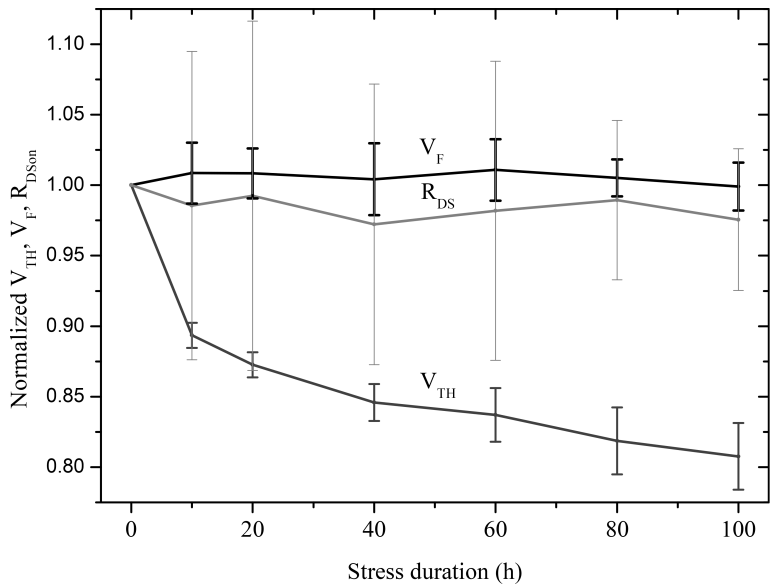

Figure 5.: CMB tests results on 9 devices. Normalized average of V_{TH}, V_F, $R_{DS_{on}}$ characterized at ambient temperature. $V_F(V_{GS} = -8\ V, I_{SD} = 10\ A)$, $R_{DS_{on}}(V_{GS} = 20\ V, I_{DS} = 10\ A)$, $V_{TH}(I_{DS} = 100\ \mu A,\ V_{DS} = 1\ V)$.

Fig. 6 shows the V_{TH} degradation extrapolated to 10,000 hours of operation. Curve fitting was performed using the least squares method (and including some data points acquired for up to 400 h CMB testing). After 10,000 hours of operation, one can predict a 35 % drop in V_{TH}.

4.3. *CMB Test — Partial Channel Conduction*

In this case, switching pattern is more complex (and more realistic): during the switching cycle, the current flows either through the internal diode or through the channel of the DUT (see table 2 and Fig. 7). The test has been done on only one sample for each test condition, but it clearly shows a different V_{TH} drift for different duty cycles. Further studies may be realised for more accurate results.

Fig. 8 shows the influence of the duty cycle "D" on the threshold voltage degradation. The cases where D=0 (which corresponds to the tests presented in the previous section), D=0.05 and D=0.15 are fully comparable with each other, as the conduction time through the intrinsic diode remains at 50% of the switching cycle (20 kHz). It is observed that for low duty cycle (5–15 %), the threshold voltage shows a weak negative drift, lower than 8%, and seems to stabilize rapidly.

For larger duty cycle (D=85 %), the threshold voltage presents a positive drift of about 8 %. Further investigation is necessary in order to assess whether this augmentation could result in a higher internal resistance of the device, and therefore higher conduction losses. Indeed, on the tested device, a $R_{DS_{on}}$ increase of 2.6 % was measured. Also, further analysis is required in order to determine influence of several parameters as frequency, applied V_{GS}, dV/dt.

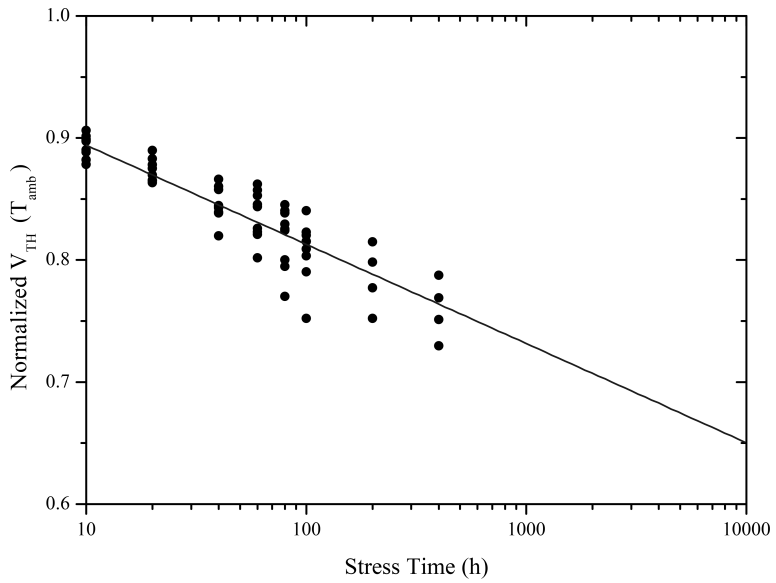

Figure 6.: Evolution and extrapolation of normalized V_{TH} over CMB test stress. Characterization at ambient temperature, $I_{DS} = 100\ \mu A$, $V_{DS} = 1\ V$.

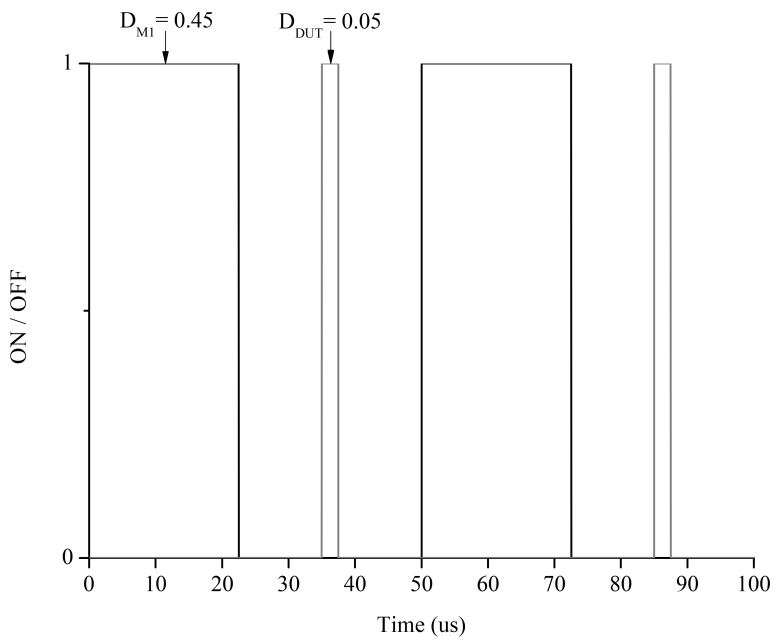

Figure 7.: Logic state of switches M1 and DUT for D_{DUT}=5%

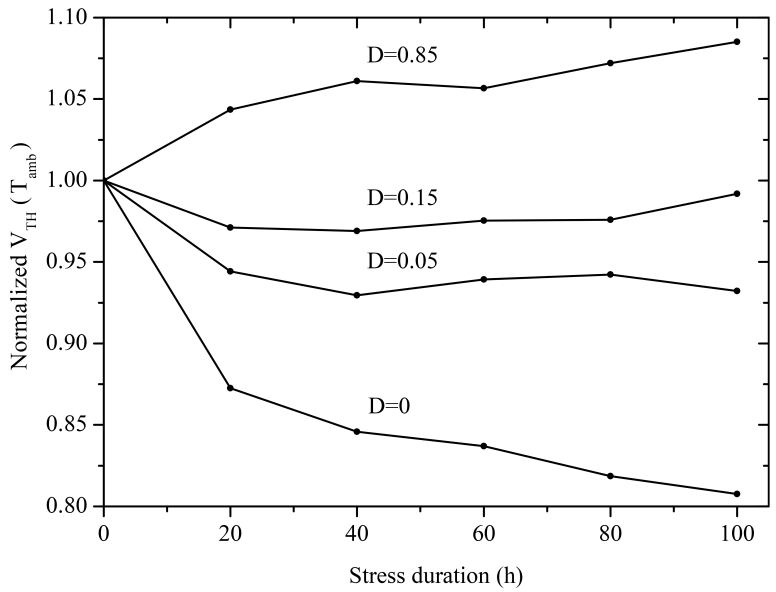

Figure 8.: Normalized V_{TH} evolution under CMB stress for different duty cycle D_{DUT} – see table 2 –. Characterization at ambient temperature, $I_{DS} = 100\ \mu A$, $V_{DS} = 1\ V$.

5. Conclusions

While Silicon MOSFET robustness is proved within a estimated lifetime higher than several tens of thousands hours, this paper shows that current SiC MOSFETs are not so stable in their characteristics. The intrinsic diode does not show a significant degradation when it is used. This differs from previous reports in the literature, and may indicate an improvement in the SiC substrate quality reducing its defect density as reported in recent years [33, 34]. Among these defects there are the basal plane dislocations or stacking faults, which would cause degradation on the PN junction.

The threshold voltage drift of the MOSFET is, *a priori*, due to the carrier injection and trapping at the SiO_2/SiC interface, or in the oxide. This injection depends on the polarity of the voltage applied at the gate, as well as on the application time (i.e. of the duty cycle).

The experiments presented here show that the standard JEDEC test used on silicon IGBT and MOSFET are not fully adapted to SiC devices. The degradation observed of the gate oxide in chopper mode is indeed higher than in static mode (HTRB). This degradation suggests that carrier injection phenomenon occurs during the switching phases, although further investigation is necessary.

The tests realized with the MOSFET channel always in the off-state show a large decrease of the threshold voltage. However, the drift seems to follow a logarithmic relationship with time, so it becomes significantly slower after the first hours of operation. Using this logarithmic approximation, a 35 % drop in threshold voltage after 10,000 hours of operation is estimated. In a real application case, the diode is only used during a small fraction of the overall switching cycle (during dead-times). Therefore, it is possible to use the internal diode instead of adding an external diode ("diode-less" applications).

Regarding the driver, and to avoid short-circuit problems as a result of a reduction in threshold voltage, the use of a negative voltage to block the device is recommended. The reduction of the MOSFET threshold voltage may reduce the immunity to EMC phenomena, which has to be studied into future.

Future work will include a larger number of samples to obtain more reliable results, a study of V_{TH} drift on devices from other manufacturers and the influence of several parameters such as dV/dt, V_{GS} levels and frequency.

Acknowledgements

This work was funded as part of the GENOME-PREMICES initiative, in the scope of the Investment for the future.

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