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► **To cite this version:**

Fabrice Caignet, Rémi Bèges, Patrice Besse, Jean-Philippe Lainé, Nicolas Nolhier, et al.. Hierarchical Modeling Approach for System Level ESD Analysis: From Hard to Functional Failure. Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC) , May 2015, TAIPEI, Taiwan. 4p., 10.1109/APEMC.2015.7175399 . hal-01843414

HAL Id: hal-01843414

<https://hal.science/hal-01843414>

Submitted on 2 Aug 2018

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Hierarchical modeling approach for system level ESD analysis: from hard to functional failure

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Abstract— With the increased number of embedded systems into our surrounding area, the electronic devices are exposed to more severe environments and have to survive ElectroStatic Discharges (ESD). Both hard and functional failures have to be guaranteed. In this paper, we will present the methodology we started to develop eight years ago to predict the impact of (ESD). Through two main examples, we will show that a behavioral modeling of the device can give good simulation results. The next step will be the implementation of failure criteria to predict both hard and functional robustness. This paper is a summary of the various results obtained.

I. INTRODUCTION

Electronic products are implemented into all systems that drive our days. Multimedia, automotive and aeronautic applications take on board more and more electronic functions, providing higher performances. As these systems are exposed to severe environments the failure requirements are growing in importance. The analysis and understanding of malfunction is usually very difficult. Indeed, the stress is propagated through harness cables, a part being absorbed by protections such as diode but a residual stress may still reach Integrated Circuits (IC). In this case, the IC does not operate as expected and can be even damaged. It is particularly important for applications that require very high level of safety such as Aeronautic and Automotive applications. As a result, the demand for robustness against system-level HBM, defined by IEC61000-4-2 standard [1], is reliability shifted to the IC component itself. Performing ESD rehabilitation prediction at system level remains a very challenging topic for many reasons. The first one is the lack of freely available information of the on-chip protection devices. Another reason that seriously complicates such task is the difficulty to model accurately and efficiently an entire system. These issues are clearly identified by the Industry Council [2].

This paper presents a complete methodology to perform transient system level simulations that help in predicting the impact of ESD. Two types of failures can be distinguished. One causing permanent damages, such as the destruction of the electronic system, called “Hard failure”. This one leads to costly manufacturing because part of the system has to be replaced. The second called “Soft or Functional failure” leads

to temporally lose of function. Even if the system can restart its activity, it could be critical during real-time execution of safety functions.

We will detail the method used to model the IC core that allows predicting both hard and functional robustness. Starting at the IC level, and using a classic hierarchical modeling technique, a complete system and environment model is assembled. At the IC level, a characterization and modeling technique will be introduced, that requires no proprietary information on the chip.

At the system level, these studies show specifically that the electrical environment of the IC (passives, transmission lines, pulse generator, etc.) impacts on the propagation of the stress just as much as the IC itself does. Emphasis will be put on where to direct the modeling effort, which elements can be neglected that is key to build a non-overkill system model. Some examples coming from previous studies will be synthesized to demonstrate what are the proper criteria that allow ESD impacts prediction.

II. MODELING METHODOLOGY

The modeling of the system is based on previously work [3, 4, 5] and VHDL-AMS [6] is used as description language. The simulation is set up with the assembly of “LEGO-like” blocs following the topology of the system composed of multiple elements: ICs, PCB lines, passive components and the test bench environment.

The complexity of embedded products leads to a complex protection strategy at the IC level. However, models of ICs should be simple and user-friendly to allow global simulation of the application board including external protections. Of course, it should be accurate to give a good estimation of the robustness level with appropriated failure criteria to be able to predict both hard and functional failures. Moreover, the hierarchical modeling methodology applied must take into account the functionalities of the circuit under operating conditions. To perform System Efficiency, ESD Design (SEED) [2] according to the requirements presented below, models have to be easily extracted and implemented into the design flow. Figure 1 shows the basic principle of simulation flow to achieve system level ESD simulation. It clearly shows that the circuits are only part of the full system simulation.

Stress generator, passives, connections and cable models are as important as the return path of the current. In our approach, the circuit behavioral model elaboration is implemented into two parts. The first one is the behavior of the ESD protection strategy of the chip to reproduce the current paths. The next step is the introduction of failures criteria depending on the adequate study such as the time to failure obtained with Wunsch & Bell [7] for hard failure. Soft failure criteria will depend on the operating conditions, and have to be associated with a proper core model.

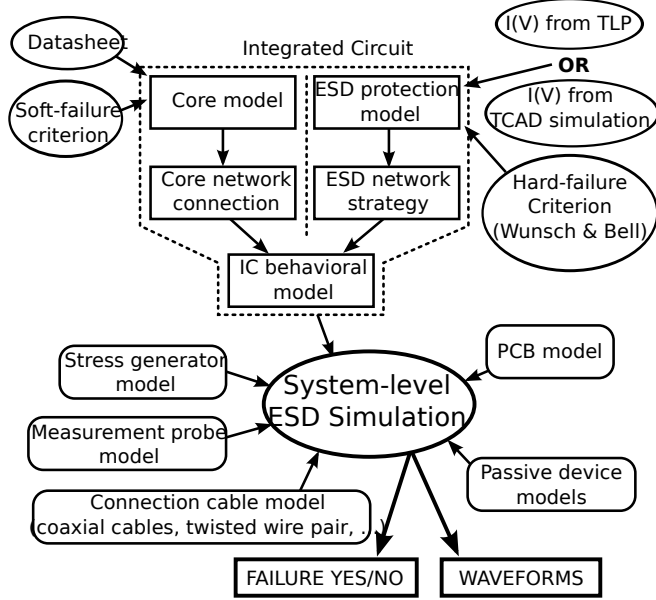


Fig. 1 Design flow for System Efficiency ESD Design (SEED) – Details of the models needed

A. IC Modeling

The IC is obviously treated as a black box, however the core and the ESD protections are still considered individually in the modeling work. By using a TLP bench, $I(V)$ curves for each pair of pins are extracted on a powered off device. Therefore, these $I(V)$ curves correspond mainly to ESD protections. Most of the time, this extraction technique provides good simulation results as reported in [3, 4, 5, 8, 9]. But in some cases, the behavioral of the protection on biased condition is strongly different as detailed in paper [10], where the hard failure dramatically changes depending on the value of the power supply. In such a case, it is possible to get a behavioral $I(V)$ curve while the system is powered.

Each characteristic is approximated by a piecewise linear curve as reported in figure 2. The set of points describing the different segments form a behavioral pin-to-pin model, stored in a text file, similarly to IBIS files concept [11]. By combining all these information in a text file, a portable, platform independent model is obtained, leaving implementation details and the choice of the simulation tool to the original equipment manufacturer.

Figure 3(a) describes an example of protection with a strong snapback (SCR). Few parameters, voltage, V_x , current, I_x , are necessary to build the state machine diagram

represented Figure 3(b). V_x and I_x define the inflection points of the Silicon Controlled Rectifier (SCR) and the equations for the states 0, 1, 2 and 3.

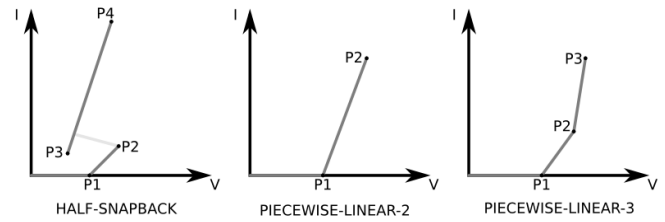


Fig. 2 Piecewise linear description of $I(V)$ curves obtained using TLP measurements.

There is no timing information in the implementation of this ESD $I(V)$ curve description. The voltage across the component can change instantly, leading to unrealistic behavior and raising convergence issues when performing a simulation of the structure. To solve this problem, a small capacitor is connected in parallel of each module. Physically, such capacitor is meaningful because a real ESD protection always shows an equivalent parallel capacitor, defining the rate at which the voltage can change across its terminals.

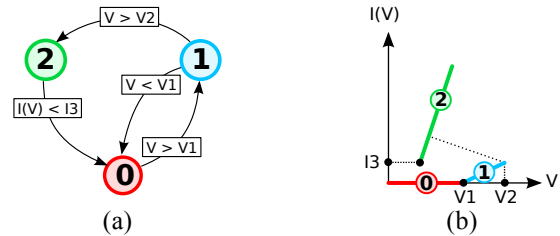


Fig. 3 Piecewise linear description of $I(V)$ curves obtained using TLP measurement.

B. Environment modeling

ESD signals have high di/dt and so, the parasitic elements of IBIS are important to estimate the dynamic of the current that flow into the chip and to the IC protections. In previous works [3, 4, 5], we have demonstrated that during normal operating conditions the parasitic elements of IBIS and the passive components of the board can create complex events like delayed-triggered or snapback protections, and forces the current path leading to the destruction of the ICs. In paper [12] the artifacts created by the environment (including ESD generators, PCB lines and measurement setup) are detailed.

By combining the IC model and the external elements of the system, SEED can be conducted. Once the system simulation is achieved the next step is to define failure criteria. Wunsch & Bell characterizations using TLP are used to provide electrical limits before failure.

III. HARD FAILURE INVESTIGATION

A. Power to failure extraction

According to [7], the power to energy failure level of a semiconductor, due to thermal effect, is strongly dependent of pulse current widths. The analytical model developed by Wunsch & Bell, focuses on the time scale where thermal

diffusion is in the time range of the pulse. It results in a relation depending on $1t$ (t =Pulse width duration).

Equations of Wunsch & Bell and Tasca will be introduced into our model. The equations are simplified. It results in the following analytical formula, which includes three main parameters:

$$Pf(t) = \frac{A}{t} + \frac{B}{\sqrt{t}} + C \quad (1)$$

Pf is the power to failure, A , B and C are constant values extracted from measurements. Wunsch & Bell curve (figure 4) referring to a real case [5] is proposed. The equivalent behavior of the IC is described by a strong snapback as presented figure 3a.

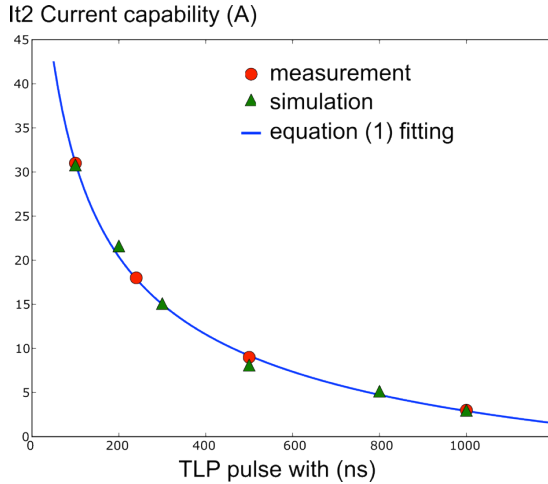


Fig. 4 Wunsch & Bell curve of the IC1 device.

To predict the robustness by simulation, the energy dissipated into the structure is computed from the following equation:

$$E = \int i(t) \times v(t) dt \quad (2)$$

The energy is computed during the simulation and when the value is higher than the time to failure curve, a flag points out the hard failure of the protection. This is directly computed for all the ESD protections involved into the current path. It is then possible to extract the level of failure, the time when the failure occurs and the involved protection. To validate this approach, the simulation is performed with TLP waveforms, and the maximum current value before damage is reported on the graph with green triangles (Fig 4). We can observe a good correlation of failure levels between measurements and simulations.

B. HMM robustness prediction

Two test vehicles will be used in real system configurations. The first one deals with an integrated circuit using a strong snapback ESD protection (IC1). The second one deals with a circuit dedicated to high voltage application (80V) requiring a low-snapback ESD protection (IC2). The two devices are submitted to Human Body Model (HMM) stress and the robustness failure level is compared to simulation.

For IC1 device, the current paths depending on the system implementation have been studied in [5]. Parasitic R, L, C elements of the package have been extracted from S-parameters measurements. Two cases are evaluated: direct zapping on the pin and stress with a 220pF external capacitor in parallel to the pin of the device. Table I compares the robustness of IC1 and the failure levels predicted by simulation.

TABLE I: HMM ROBUSTNESS OBTAINED BY SIMULATION AND BY MEASUREMENT WITH AND WITHOUT EXTERNAL CAPACITOR ON IC1

HMM 150pF/330Ω	Measurements results	Simulation results
220pF in parallel	Pass: 15.2kV Failed: 15.4 kV	Pass: 15.8kV Failed: 16kV
no external Cap	Pass: 15.2kV Failed: 15.4 kV	Pass: 15.8kV Failed: 16kV

The second case, IC2, deals with an analog circuit dedicated to 80V applications. In this case, the equivalent behavioral model of global pins is closed to a reverse biased diode model. The triggering voltage value V_{T1} and the snapback voltage value are very closed and higher than 80V. The same prediction will be achieved with external capacitors (10nF and 100nF) placed in parallel (table II).

TABLE II: HMM ROBUSTNESS OBTAINED BY SIMULATION AND BY MEASUREMENTS WITH AND WITHOUT EXTERNAL CAP ON IC2

HMM 150pF/330Ω	Measurement results	Simulation results
no external Capacitor	Pass 5kV Fail 5.5kV	Pass 5.7kV Fail : 5.8kV
10nF in //	Pass 10kV Fail 12kV	Pass 11kV Fail 11.5kV
100nF in //	>25kV	>>25kV

Simulation results provide good accuracy with measurements. We can observe the benefits of external capacitors on IC2. The value can be selected to fulfill the ESD specification requirements. Of course the capacitance value can impact the signal integrity during normal operations.

IV. FUNCTIONAL FAILURE INVESTIGATION

The next step to achieve system safety is the prediction of soft failures. The study we present is based on the publication [12] where the functionality of a voltage regulator is investigated. Using a classic hierarchical modeling technique, a system-level model is assembled with the IC, passives and printed circuit board models. TLP and IEC 61000-4-2 stresses are then applied. A behavioral model of the ESD strategy IC has been developed following the proposed methodology of this paper. For functional purpose, a simple level 1 MOS transistor and a Proportional-Integral control are used to model the voltage regulation. Because the voltage regulation is slow in comparison to an ESD event, this rough model of the function with approximate parameters is sufficient to achieve accurate results at the ESD timescale, as will be demonstrated later. The RESET function provided by the

regulator model is a simple range comparator as specified in the IC datasheet.

TLP and IEC 61000-4-2 stresses are injected on the system under test, on the unregulated input voltage pin. The IC is powered on. The stress generator and the voltage supply are isolated using an injection capacitor and a decoupling inductor, similarly to the Direct Power Injection (DPI) technique.

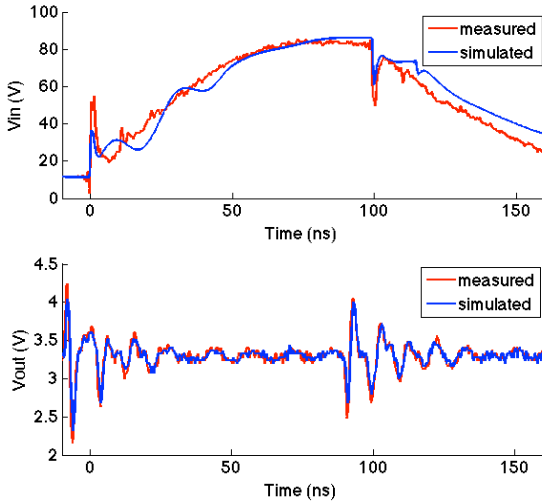


Fig. 5 Comparison between measurement and simulation at the input and output for 600V TLP injection (1ns rise time -100ns duration).

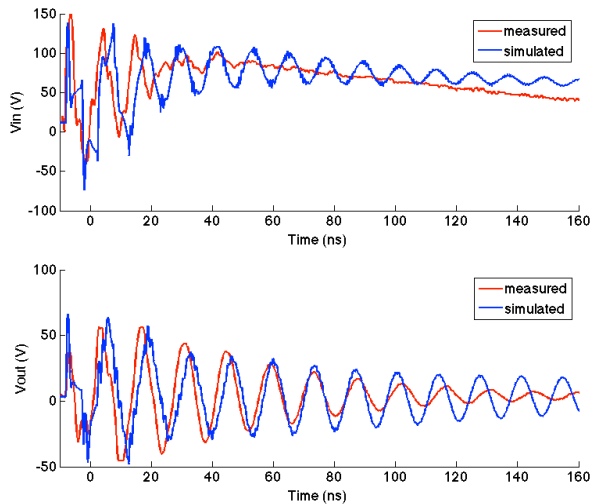


Fig. 6 Comparison between measurement and simulation at the input and output for 8KV IEC61000-4-2 injection.

Results demonstrate that the model performs right with a powered on device stressed by a TLP impulse sufficiently important to trigger ESD protections (Fig. 5). When and IEC 61000-4-2 stress is injected into the system (Fig. 6), there is an good correlation between simulation and measurement, which confirms that the model behaves as expected. The regulation function can be predicted with sufficient accuracy.

To achieve such results, a very thorough test setup modeling is required, and is as important as the IC modeling itself. The main three elements to pay attention to are

connection cables, oscilloscope's probes and non-ideal decoupling capacitor model.

V. CONCLUSION

This paper described a method to predict the robustness of integrated circuits submitted to ESD system level stress with and without external devices. It has been successfully used to evaluate the ruggedness of different products using different ESD protection strategies. This prediction method is based on behavioral models of ICs and on the models of external elements that can be easily extracted. Behavioral models and failure criteria are generated from TLP measurements using different pulse widths. Both hard and soft failures are predicted using full behavioral criteria. This method is useful to select the best protection solutions at the PCB level to prevent ICs against damages and could be implemented in the system design flow. It closes the gap between IC manufacturers and equipment manufacturers providing a tool to predict the ESD stress propagation at the system level.

ACKNOWLEDGMENT

The authors would like to thank the people who worked on this topic since 8 years, and all the people involved into ANR project E-SAFE ended in 2012 which has supported this work. This work is also supported by the ESDA for modeling purpose.

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