Practical Transient System-level ESD Modeling - Environment Contribution

Marise Bafleur, Rémi Bèges, Fabrice Caignet, André Durier, Christian Marot, Nicolas Nolhier

Practical Transient System-level ESD Modeling - Environment Contribution

Rémi Bèges[1,2], Fabrice Caignet[1,5], André Durier[3], Christian Marot[4], Marise Bafleur[1,5], Nicolas Nolhier[1,5]

(1) CNRS, LAAS, 7 avenue du Colonel Roche, F-31400 TOULOUSE, FRANCE
tel.: +33561337840 , e-mail: rbeges@laas.fr

(2) Freescale Semiconductor, 134 avenue Eisenhower, 31023 TOULOUSE cedex 1, BP 72329, FRANCE

(3) Continental Automotive France SA, 1 Avenue Paul Ourliac, 31100 TOULOUSE, FRANCE

(4) Airbus Group Innovations, 18 rue Marius Terce, 31300 TOULOUSE, FRANCE

(5) Univ. de Toulouse, UPS, LAAS, F-31400, Toulouse, France

Abstract – A methodology for building a transient model of an analog system is detailed. It does not require proprietary knowledge for integrated circuits (IC). At IC level, it combines a protection structure characterization and behavioral modeling with a core description. A specific test board is developed with a smart voltage regulator to validate the methodology. A system model is assembled to perform powered-on transient ESD simulations. A soft-failure criterion is chosen and the prediction of trends in soft-failure generation is carried out. The strong influence of the electrical environment is demonstrated through this case study.

I. Introduction

Performing system level reliability prediction against an Electro-Static Discharge (ESD) stress remains a very challenging topic. Being able to do so could bring further improvements to existing protection approaches [1], while reducing costs. In the case of analog devices, the lack of freely available transient IC models makes the task difficult. For digital circuits, IBIS files [2], meant for signal integrity simulations, could form the beginning of an answer but are not entirely suitable [3].

Several studies were performed in the past about IC modeling and system level ESD simulations [3][5][8][13]. This preliminary work laid the basis for behavioral modeling based on TLP extraction of IC parameters. Validations were performed using simple injection scenarios (TLP and IEC 61000-4-2) [13] and soft failures were studied on digital chips. Other investigations [14][15] were conducted in the past about hard failures of non-powered systems. The propagation of a stress from the input connector of a board to the input pin of an IC was studied and improved design rules (System Efficient ESD Design – SEED) were defined.

In the continuity of this work, this paper addresses a new case of a system designed around a mixed-signal IC (a smart voltage regulator) that contains digital, analog and power functions. The final goal is the prediction of soft-failure robustness of the device. In order to study soft-failures, it is required that the device is powered-on and placed in regular operating conditions. The integrated circuit model must be able to work under such novel condition. For that matter, the IC modeling technique is extended in order to perform powered-on simulations. Before doing soft-failure prediction, the ESD propagation through the system is simulated. This intermediate step aims at reproducing in simulation the voltage variations on the IC output when an input is exposed to an ESD.

The complete test setup is modelled using a modular approach. Each element of the setup is well characterized and modelled separately. This approach is quite flexible and enables mixing different types of models (structural, behavioral, physical, etc.) with different implementation techniques (SPICE, VHDL-AMS, Verilog-AMS, etc.). All these blocks are then assembled following a classical hierarchical modeling technique.

In order to validate this technique, a specific test board has been developed around a smart voltage

regulator (see part II). The IC is placed on a board with all the passive devices recommended by the IC manufacturer to ensure proper functioning, as it would be in a real application. This chip is a smart regulator supplying a reset-out signal that indicates the loss of the regulation function. The raise of this flag is considered here as the soft-failure criterion.

An important aspect highlighted throughout this document is the tremendous impact of the environment when trying to achieve accurate system-level simulations. The impact of the main elements of the board and the test setup will be detailed in parts V and VI.

Different ESD stresses are applied to validate this approach in part VII. First, a TLP is used as a stress generator in order to test the model in a "simple" injection scenario, to perform a first evaluation of the modeling work. Two more tests are then conducted, using a standard IEC 61000-4-2 ESD gun[4] and pulse 3B from the ISO 7637-2 automotive standard [16].

Ultimately, it is demonstrated in section VIII that some trends on soft-failure robustness can be predicted.

II. Test Board

The test board is build around an automotive low dropout (LDO) smart voltage regulator IC. For an input voltage between 4.4 and 45V, it supplies a regulated 3.3V output voltage with a maximum current of 400mA. The regulator also provides a digital open collector output that triggers low when the regulated voltage is outside the +/- 3% range around 3.3V. The raise of this flag is considered to signal a soft-failure. The test setup (see schematic Fig. 1) is a printed circuit board with all the passive devices (decoupling capacitors, pull-up resistors, etc.) needed for the IC to properly operate.

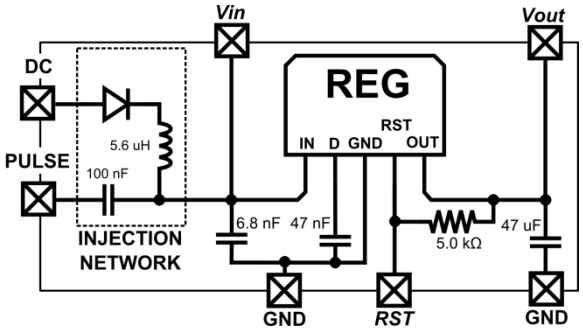

Figure 1: Test PCB schematic

An injection network (Fig. 1) is used to superimpose the impulse on the DC supply voltage. This is based on the Direct Power Injection (DPI) standard injection setup [18]. A 5.6 uH inductor in series with a Schottky diode ensures that no transient current will be injected inside the DC supply. The 100 nF capacitor isolates the stress generator from the DC supply. The capacitor value is chosen high enough to not filter the stress pulse and provide correct isolation from the DC supply. The system is implemented on an FR4 double-sided PCB. Bottom face is a ground plane and all traces are 110 Ω matched.

The board is then connected to a test setup (Fig. 2), for stress injection and measurements. All cables are 50 Ω matched, and the ground connection is provided by the stress generator. 1MΩ oscilloscope inputs are used for measurements.

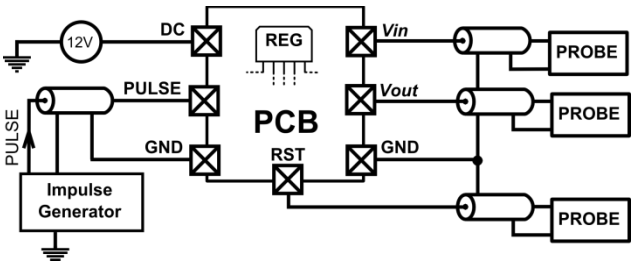

Figure 2: Test setup schematic

III. Simulation flow for system-level ESD

In this part, the global approach for achieving system level ESD simulation and robustness prediction is presented. The simulation flow employed is introduced in Fig. 3. This is a modular approach where each module can be described separately using any language (SPICE, VHDL, VHDL-AMS, Verilog, etc.).

The principle is to have a library of well defined models, and to assemble them together according to the board and setup configuration.

For a practical in-lab testing, where the test setup is fixed and each element is well characterized, this flow is particularly suitable, as only the IC model and board schematic needs to be changed when testing a new product. The application of this simulation flow to a real-world application, where the electrical environment of the board is not mastered, is not considered in this work. This is relying on the fact that test standards define testing conditions that should be representative of the real-world electrical environment of the device under test.

The IC model is divided in multiple blocks as detailed in IV. Package, ESD protections and core functions are modelled separately then connected together. A characterization and modeling technique for protection structures is presented, that requires no

proprietary information on the chip. The method used to model the IC core and package parasitic will be detailed. The integrated circuit model is the most complex to implement, but that does not mean it has the biggest influence on the simulation.

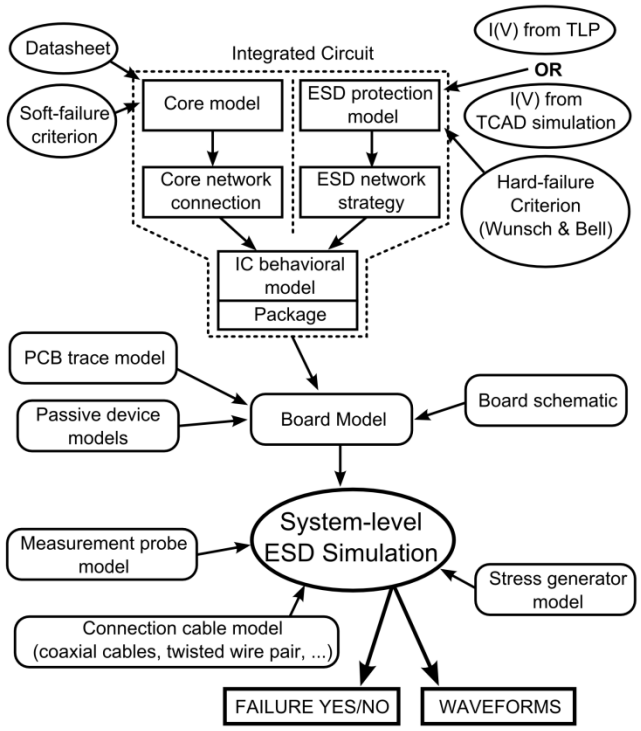

Figure 3: Proposed simulation flow

The printed circuit board is in the second level in the hierarchy. The schematic, the chip model and off-the-shelf models for PCB traces and passive devices are combined together. Several interactions between those elements are detailed in V.

Finally, at the test setup level (section VI), this study presents the work done for electrical environment modeling (transmission lines, pulse generator, oscilloscope inputs).

The influence of most elements of the setup and root causes for simulation errors and measurement artefacts are detailed through sections IV, V & VI.

IV. The IC Model

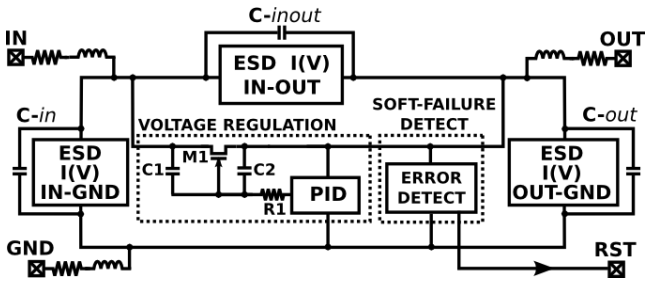

Figure 4: The complete IC model

The complete IC model is presented Fig. 4. To account for ESD protections and power structures, a pin-to-pin model is used, representing the quasistatic I(V) characteristic between two pins.

It is applied to input, output and ground pins, by pairs of two pins. Voltage regulation and reset functions are modeled as well, as described in IV.b.

a. Pin-to-pin model (ESD protections)

A pin-to-pin I(V) model is developed for ESD protections. It is a behavioral black-box model, meaning that no design knowledge of the structure existing between the two pins is needed. An ESD structure, a power structure (power transistor, power clamp, etc.) or a parasitic structure are treated the same way.

First, a classical 100 ns (300 ps risetime) TLP characterization is performed (Fig. 5). An I(V) curve for each pair of pins is extracted on a unpowered device. Using TLP-extracted I(V) curves to describe ESD protection structures and pin-to-pin responses has been previously introduced in several papers [5][6][7] and is considered a valid approach.

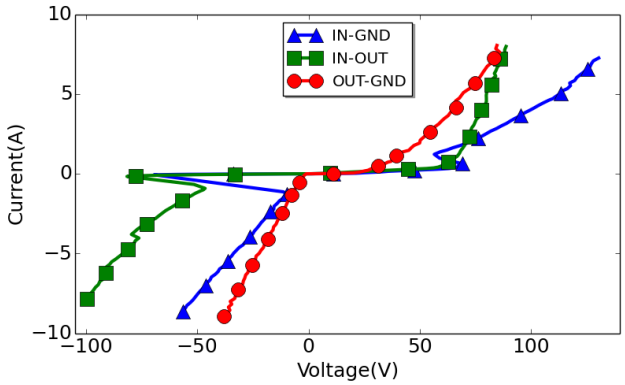

Figure 5: TLP pin-to-pin measurements of the IC

Each characteristic is then approximated by a piecewise linear curve, forming a behavioral pin-to-pin model. For simulation purposes, a two-terminal VHDL-AMS component has been developed to translate the I(V) characteristic. The code handles snapbacks and uses a numerical state-machine (see figure 6) as described by N. Monnereau [3][8].

There is no timing information in the implementation of the ESD I(V) module, the voltage across the component can change instantly, leading to unrealistic behavior and raising convergence issues when performing a simulation of the structure.

To solve this problem, a small capacitor is connected in parallel of each module. Physically, such capacitor is meaningful because a real ESD protection always shows an equivalent parallel capacitor, defining the rate at which the voltage can change across its terminals. It slows down the voltage changes across the protection structure, allowing the simulation to converge during snapbacks.

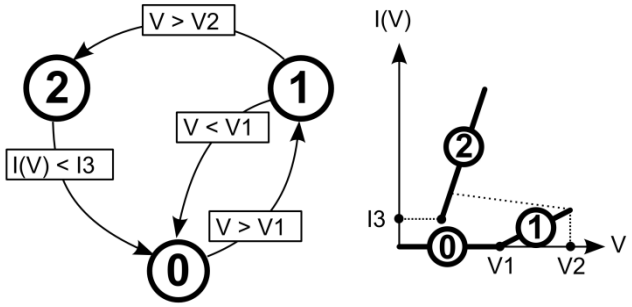

Figure 6: State machine overview for 1 pin/ 1 polarity

The only issue with that approach is to not account for the overvoltage that can be generated during the triggering of the ESD protection (Fig. 7). In this work, this did not showed up as an issue. This point can be fixed in VHDL-AMS by adding a delay between the moment the state machine goes into snapback and the moment the current starts flowing.

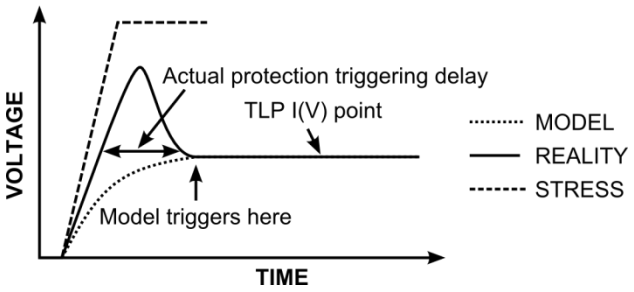

Figure 7: ESD Protection induced overvoltage

In simulation, the capacitor slows down voltage variations. When the voltage is high enough, the ESD protection switches on and absorbs current with no delay.

In reality, ESD protections do not immediately conduct current before a conduction delay. During that delay, the voltage keeps increasing, causing an overvoltage. When the current through the protection becomes high enough, voltage falls down to the TLP-extracted quasistatic bias point.

b. Core modeling

A behavioral model was developed from scratch with information extracted from the datasheet. This is a far from ideal approach, but it requires once again no proprietary knowledge of the chip. The voltage regulation is implemented by the combination of a simple SPICE level 1 MOS transistor (M1) and a Proportional Integral Derivative (PID) controller [17] (see Fig. 8).

Basically, the PID module computes the error between the desired and actual output voltage, and acts on the grid-source voltage in order to reduce that error. It is essential to limit the grid-source voltage supplied by the PID module in order to limit the maximum output current to the value given in the datasheet. This is done in the PID module implemented in VHDL-AMS.

The maximum output current I_{max}, in conjunction with the output capacitor of value C_{out}, gives the maximum rate of increase of the output voltage $\Delta Vout/\Delta t = I_{max}/C_{out}$ (in V/s).

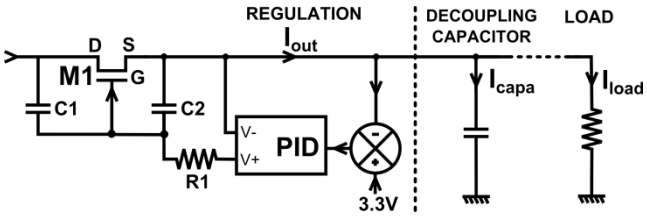

Figure 8: Behavioral voltage regulation model

In this model, the maximum rate of decrease of the output voltage does not depend on the regulator itself, but on the output load. Indeed, when the output voltage is too high, Vgs is clamped to 0 V and the current through the MOS is null. The output capacitor being charged up too high, the only way to lower the output voltage is to discharge the capacitor through a load. This is an assumption made on the actual unknown behavior, but because the voltage regulation is slow compared to an ESD it does not seem to have a great impact on simulation accuracy.

Finally, the values for the three parameters P, I and D will determine how the current varies between those two boundaries [0 mA ; 400 mA] (values from the datasheet), and most importantly, will provide stability to the control loop if correctly tuned.

A first order low-pass filter constituted by [R1;C2] (Fig. 8) was added to limit the rate of change of V_{GS}. The C1 capacitor accounts for the gate-coupling effect during ESD. Because the voltage regulation is slow in comparison to an ESD event, this rough model of the function is enough to achieve accurate results at the ESD timescale.

The RESET function is a simple range comparator without any timing. The chosen voltage range for the model is the nominal output specified in

the IC datasheet (+/-2%). Outside of that range, a numerical flag is raised. This is a very simplistic approach compelled by the lack of knowledge on the actual function. However it is already sufficient to produce acceptable results for soft-failure simulation (section VIII).

c. Package model

An RLC network models the package of the device. The equivalent capacitance (from IBIS[2]) to ground is neglected because supposed of extremely low value. The series inductance is the only element that can have a significant impact on the waveforms. Typical values are considered close to a few nH [9], which is enough to induce a significant voltage spike across its terminals during transient current injection (i.e. TLP)[5].

The combination of all these blocks form the complete IC model introduced previously (Fig. 4). It can be used to simulate the injection of an electrical fast transient (TLP, IEC 61000-4-2, etc.) directly on the bare chip.

V. Board Modeling

a. Passive Devices

For pulses with rise-time close to the nanosecond, High-Frequency (HF) effects of passive elements are not negligible. The use of perfect models for capacitors and inductors lead to unrealistic simulations as presented in Fig. 9.

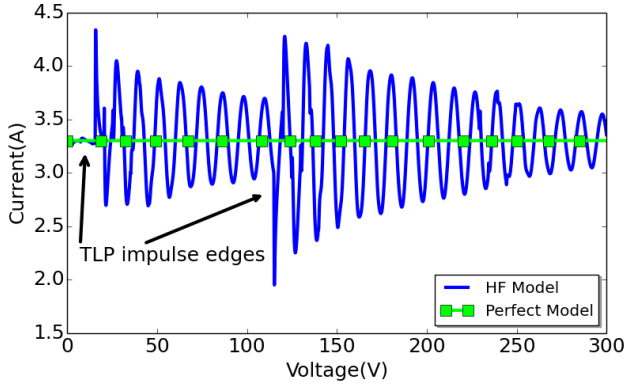

Figure 9: Simulated response of perfect vs. real 47uF capacitor during TLP injection on the test board

However, it is unnecessary to use an HF model for every single passive element of the circuit. In the simulations presented in this document, only decoupling capacitors were modelled as such, apparently being the only ones to have a significant impact. An impedance analyser allows for easy and accurate extraction of values for the different elements of the HF model.

b. PCB traces

The study was conducted for 110 Ω matched PCB traces, but it can apply to other impedances as well.

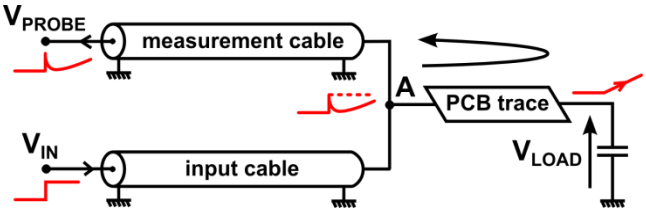

Figure 10: PCB "masking" effect configuration

PCB traces induce a delay proportional to their length (~33 ps/mm for 110 Ω). In the case where a PCB line, on the propagation path of a stress, separates a load from a measurement point A (see Fig. 10 and 11), a residual peak can be generated on the measurement. Even very short lines (< cm) are affected.

Indeed when a stress propagates towards the load (see Fig. 10), it first hits the measurement point A. The potential at point A starts rising. After a time corresponding to the delay of the PCB trace, the pulse reaches the load. The voltage settles to the load bias point, and this voltage change propagates back toward the measurement point A, reaching it after a second PCB delay. During this interval of time, the voltage at the measurement point A was exclusively set by the original pulse, and not dependent on the load.

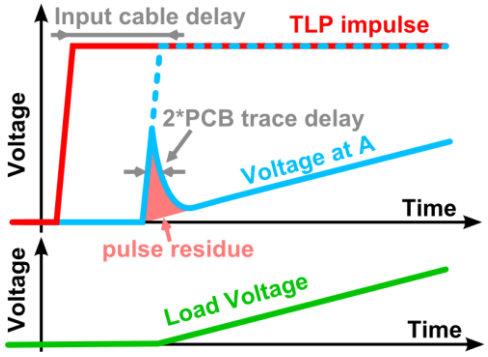

Figure 11: V(t) at node A (blue) original impulse (red) and load voltage (green)– the load is a capacitor

In Fig. 11 and 12 the load (a capacitor) is considered perfect and does not show any HF behavior. The spike is purely due to the PCB trace. In reality this delay-induced peak and HF-effects previously described in V.a. could cumulate.

Taking this effect into account is essential when the delay of the PCB trace is not negligible against the

stress signal risetime. The ratio between both time values will determine the amplitude of the generated spike.

On the other hand, in our setup, other PCB traces not involved in this type of configuration were kept short (< 5 cm) and did not seem to impact the measurements.

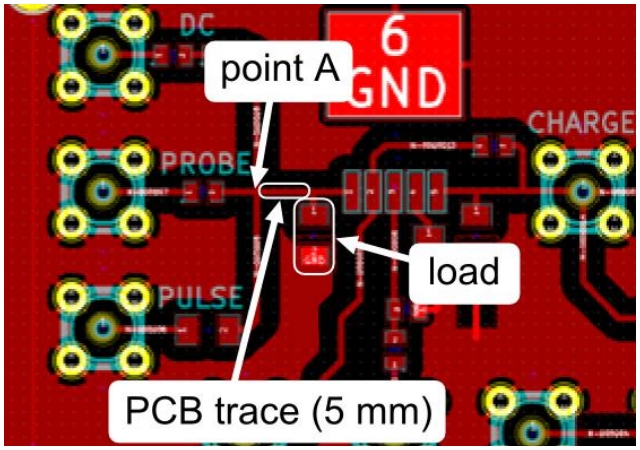

Figure 12: delay masking effect on test board

In simulation only the 5 mm long PCB trace specified in figure 13 was modelled, but not any other longer traces. The same transmission line model was employed for coaxial cables and is described in VI.a.

VI. Environment Modeling

a. Cables

Because ESDs can last a few hundred nanoseconds, propagation delay of coaxial cables (about 5ns/m for a 50 Ω cable) is not negligible in a simulation. Such cables, by introducing a delay between two reactive loads or impedance breaks, can induce important oscillations with a period of about twice the cable delay.

There are several solutions for modeling a lossless coaxial cable or PCB trace. The most popular model is the distributed LC ladder. The issue with this model is the huge amount of elements required for dealing accurately with long transmission lines and short risetimes. In the case of a TLP, there can be several orders of magnitude between line's delay and LC's element delay (that should be much smaller than signal risetime for accuracy), leading to a massive amount of LC elements and very long simulation times.

There is a computationally much more efficient solution when losses are negligible. In [12], Branin details an analytical solution to the transient analysis of a transmission line. It provides a true mathematical solution, rather than the approximation performed with the LC ladder, and is perfectly accurate for uniform lossless transmission lines. As a consequence, this analytical model guarantees that risetimes will not be deteriorated. Last but not least, simulation time is not dependent on the transmission line delay because the delay is simply a parameter in the model's equations.

This is the solution that was chosen for cables and PCB traces, as it enables much more accurate results and shorter simulation times. This model is implemented in VHDL-AMS with an option to preload the line at a user-defined voltage, which is very practical for TLP simulations and reduces computation time.

b. Probes

Building a proper oscilloscope probe model is also very helpful to achieve proper correlation between measurement and simulation. An important characteristic to take into account in the simulation is the actual bandwidth of the probe. In some cases, it can be lower than the sampling frequency of the oscilloscope. Adding a simple 1st order low-pass filter with similar bandwidth in the probe model seems to be sufficient.

For high-speed oscilloscopes, the user often has a choice between a strong impedance (i.e. 1 MΩ) probe and a matched 50 Ω termination. In the case of a 1 MΩ probe, the strong impedance guarantees that only a tiny fraction of the transient current will be injected inside the oscilloscope. However, when connected to the circuit by the mean of a coaxial cable (50 Ω for example), the resulting impedance break generates unwanted reflections and spikes on the measurements.

Using a matched 50 Ω probe allows overcoming this issue and get a higher bandwidth. However, with such lower impedance, the probe is much less transparent to the rest of the circuit. The impedance offered by the IC input can often be higher than 50 Ω, directing the majority of transient current directly into the probe.

In the measurements (section VII), it was chosen to use a 1 MΩ probe and take the unwanted reflections into account in the simulation, but for future work an on-site pickup resistor (pick-off tee) combined with a 50Ω oscilloscope input will rather be used.

c. Generator model

Finally, when lacking an accurate pulse generator model, an excellent knowledge of the generator's electrical circuit has proven extremely useful. In the

case of TLP generators, several elements such as attenuators or power diodes can significantly impact the signal waveform after the moment the pulse has been injected, because of reflection phenomena.

For ISO 7637-2 generator, none of these options were available. It has been characterized with high quality resistive or capacitive loads, and a model was derived from these measurements (see figure 13).

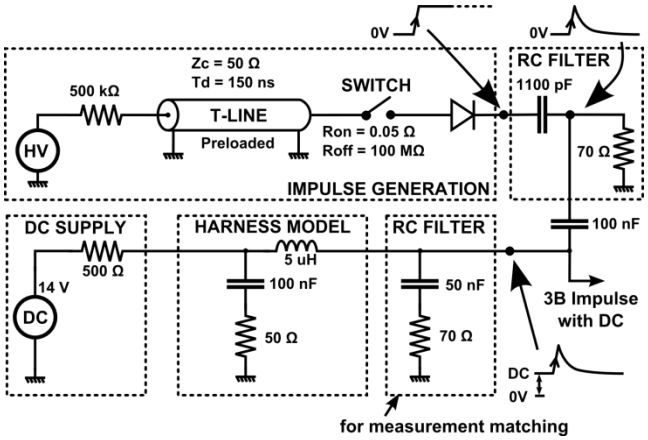

Figure 13: Behavioral ISO 7637-2 3B generator model

VII. Measurements/Simulations

A comparison between simulated and measured signals at the main input and output pins of the system is performed first with a TLP stress (see figure 14). The goal is to predict the signal waveform at the output of the IC when injecting an ESD on the input.

Results demonstrate that the model correlates very well with the measurements when a powered-on device is stressed by a TLP impulse sufficiently important to trigger ESD protections.

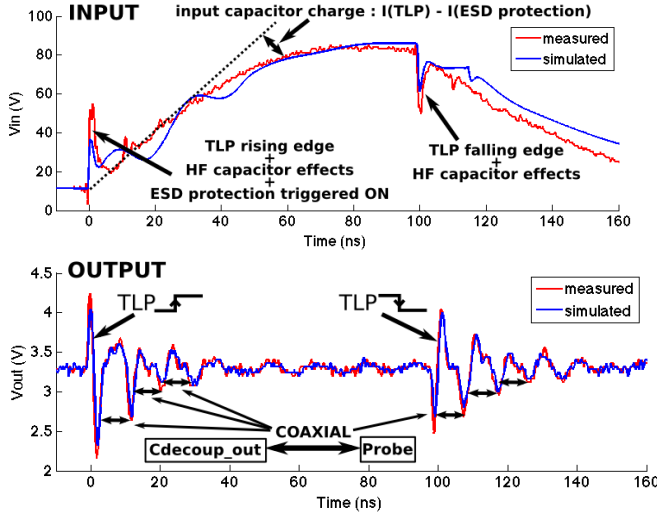

Figure 14: Measured vs Simulated Vin(t) & Vout(t) (600 V TLP impulse)

This modeling technique gives accurate results even if the ESD model of the IC has been extracted in non-powered conditions. On the input (Fig. 14), we see from 20 ns the capacitor charging up at constant current, minus the current deviated into the ESD structure. As the voltage increases, the current flowing through the ESD protection rises as well, slowing down the charge of the decoupling capacitor.

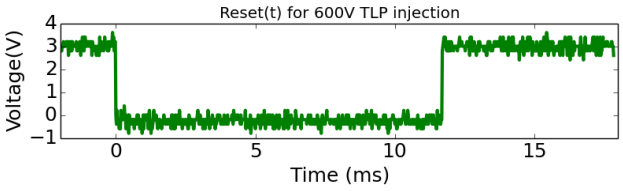

Figure 15: Measured Reset(t) (600V TLP impulse) - Different timescale than figure 14 - Note : there is a 5us delay on x axis compared with figure 14.

On the output (Fig. 14), we can observe two damped oscillations. They are well reproduced in simulation because cable, probe and decoupling capacitor models are accurate.

In that case, the IC does not really impact the period of oscillations as one might first assume, it only has an influence on the amplitude (transmitted power from the input). The RESET flag is raised (triggered low), both in real and simulated conditions. The simulated reset curve is not displayed because it is simply a numerical flag that is also raised for a 600V TLP impulse. On Fig. 15, the reset output triggers low about 5 us after the stress is injected, which is the standard behavior defined in the datasheet.

Basically, the ESD event seems to be detected immediately by the reset comparator, but it takes 5 us to trigger the reset pin down. The flag is then held down during 12 ms, which is consistent with the datasheet.

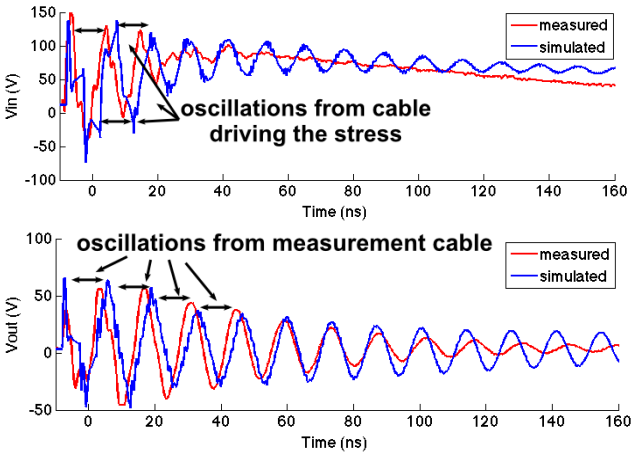

Figure 16: Vin(t) (top), Vout(t) (center) and Reset(t) for 8kV IEC 61000-4-2 injection

TLP turned out to be an excellent tool for adjusting the values of the different elements of the simulation. Its clean, squared pulse and 50 Ω matching ease both signal analysis and model debugging.

A similar test on the identical setup is conducted with an 8kV IEC 61000-4-2 ESD gun. Chiu's model [11] is used to generate the ESD in simulation, with values slightly tuned for our in-lab ESD gun.

On the input, the first peak amplitude matches well with the measurement (figure 16). A strong oscillation is observed between -10 and 30 ns, mainly due to the in-lab gun imperfections and the cable used in the setup to drive the stress to the PCB. The oscillation is damped much quicker in the measurement, apart from that there is a good correlation between simulation and measurement on the input.

On the output (figure 16), the 8 kV gun stress induces an over-voltage of 60V on the 47 µF capacitance, and the observed oscillation is well reproduced by the simulation. As a consequence, the RESET flag is raised. All these results confirm that the model behaves properly when confronted to an IEC 61000-4-2 pulse.

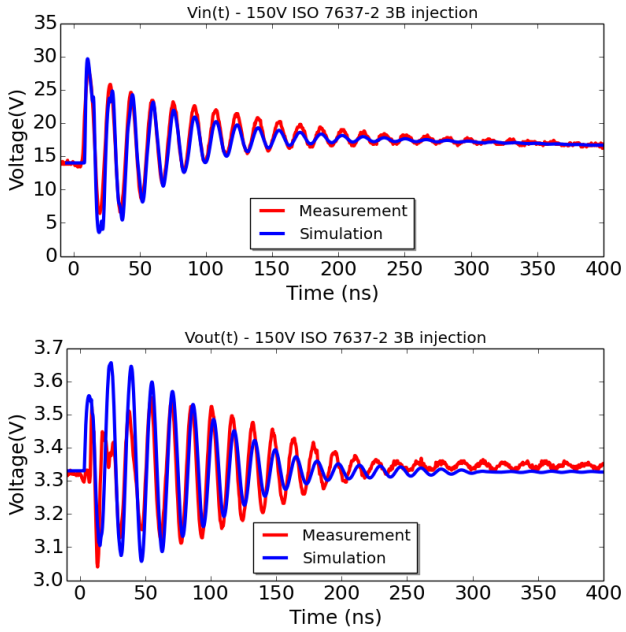

Figure 17: Vin(t) (top) and Vout(t) (bottom) for ISO 7637-2 3B 150V injection

Finally, the test is repeated with an ISO 7637-2 3B impulse (Fig. 17). Once again, oscillations with similar period to those in Fig 14 and 16 are observed, and correspond to measurement cables. In simulation, using the delay defined in the cable datasheet is enough to get the right period for these oscillations. The results are in the same order of magnitude in terms of accuracy. On the output, amplitudes are a bit off and the dampening is slower, which may be explained by the lack of accuracy of the generator's model. The first peak on both input and output correlates well, showing that PCB effect, HF behavior of decoupling capacitors and generator risetime are well modelled.

Globally, the results are acceptable and demonstrate that this modeling work is valid at the ESD timescale in the case of an IC that hosts digital, analog and power functions.

VIII. An example of soft-failure main trend prediction

Once the transient behavior of the models was validated, an attempt to predict the minimal TLP level required to induce soft failures has been carried out. For that matter, the amount of identical 6.8 nF decoupling capacitors in parallel on the input was increased, and for each amount, the minimal TLP stress level triggering a reset was recorded (see top curve Fig. 18). The simulation has an important offset error but the curves are varying in the same manner and the trend fits with the measurement. Simulation and measurement agree on the fact that increasing the amount of decoupling capacitors on the input improves the robustness of the system against soft failures.

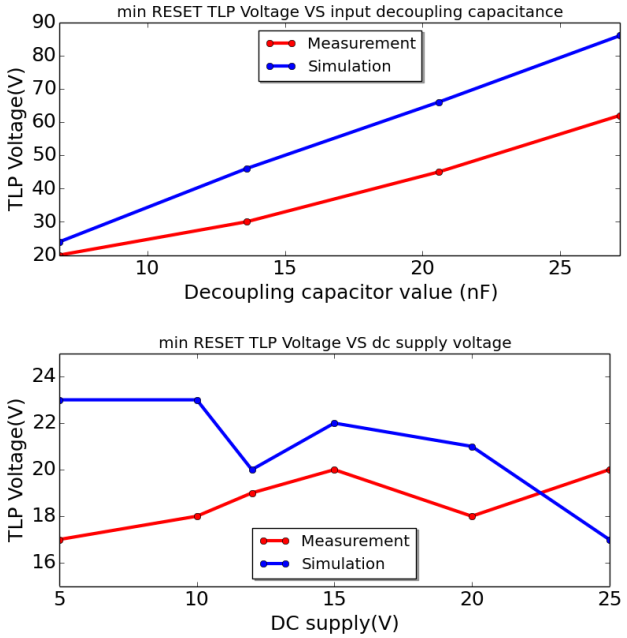

Figure 18: RST TLP voltage versus decoupling capacitance (top) and DC supply voltage (bottom)

The impact of the DC supply voltage on the soft-failure robustness is also studied (see bottom curve Fig. 18). The DC voltage is varied and once again the minimal TLP level inducing a soft-failure is recorded. The curves are globally flat with an important static error. Once again, simulation and measurement agree that in this particular study case, the DC supply voltage has no influence on the soft-failure robustness of the system.

This two curves show the present limit of the model. In this work, it is so far not possible to predict accurately the soft-failure level, only a trend. This result however was achieved with no proprietary knowledge of the chip and in particular of the reset-out function properties (timings, exact triggering levels, etc.).

IX. Conclusion

A working technique for modeling an integrated circuit (ESD protections and core functions) without any knowledge of its design has been presented. It enables transient system-level simulations of a powered-on device stressed by a positive pulse of several hundred nanoseconds.

The model of the system, built on a modular hierarchical approach, has been validated with TLP, IEC 61000-4-2 and ISO 7637-2. The analog output voltage and some trends for the reset are predictable by simulation. It was demonstrated that the environment impacts quite a lot the propagation of the stress, and must be accurately taken into account in the modeling.

For soft-failure prediction, this approach showed some limitations. Ultimately, the knowledge of the internal design could help developing a more accurate behavioral model of the chip that would enable soft-failure prediction without disclosing proprietary information. This concept will be investigated further at the IC level and specifically at modeling core functions at the ESD timescale in order to enable true soft-failure prediction at the system level.

Acknowledgements

The authors would like to thank Leonardo Di Biccari (ST Microelectronics) for his very valuable feedback on this work.

References

[1] Industry Council on ESD Target Levels, White Paper "System Level ESD, Part I: Common Misconceptions and Recommended Basic Approaches"

[2] Input Output Buffer Information Specification, http://www.eda.org/ibis/

[3] Monnereau, Nicolas, et al. "Behavioral-modeling methodology to predict Electrostatic-Discharge susceptibility failures at system level: An IBIS improvement." EMC Europe 2011 York

[4] "Electromagnetic compatibility (EMC), Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test", IEC61000-4-2

[5] Nicolas Monnereau, Fabrice Caignet et al., "Building-up of system level ESD modeling: Impact of a decoupling capacitance on ESD propagation", EOS/ESD Symposium 2010

[6] Li-Moum Ting, Charvaka Duvvury et al., "Integration of TLP analysis for ESD troubleshooting"

[7] Hugh Hyatt, Jay Harris, et al., "TLP Measurements for Verification of ESD Protection Device Response", IEEE transactions on electronics packaging manufacturing, Vol 24, No.2, April 2001

[8] Nicolas Monnereau, Fabrice Caignet et al., "Investigating the probability of susceptibility failure within ESD system level consideration", EOS/ESD Symposium 2011

[9] Mark Pavier, Arthur Woodworth, et al., "Understanding the effect of power mosfet package parasitics on vrm circuit efficiency at frequencies above 1mhz", 2003.

[10] "Electromagnetic Compatibility (EMC), Integrated Circuits, Measurement of Electromagnetic Immunity 150 kHz to 1 GHz - Part 4: Direct RF Power Injection Method", IEC62132-4, 2007.

[11] K.M. Chiu, "Simulation and measurement of ESD test for electronic devices", Phd thesis, 2003.

[12] F.H. Branin Jr, “Transient analysis of lossless transmission lines”, Proceedings of the IEEE, Volume 55, Issue 11, Nov 1967.

[13] P. Besse, F. Lafon et al., “ESD system level characterization and modeling methods applied to a LIN transceiver”, EOS/ESD Symposium 2011

[14] Stéphane Bertonnaud, Charvaka Duvvury et al., “IEC System Level ESD Challenges and Effective Protection Strategy for USB2 Interface”, EOS/ESD Symposium 2012

[15] Tianqi Li, Junji Maeshima et al., “An application of utilizing the system-efficient-ESD-design

(SEED) concept to analyze an LED protection circuit of a cell phone," Electromagnetic Compatibility (EMC), 2012 IEEE International Symposium.

[16] ISO 7637-2 standard, "Road vehicles - Electrical disturbances from conduction and coupling - Part 2: Electrical transient conduction along supply lines only"

[17] Karl J. Åstrom, Tore Hagglund, "PID Controllers: Theory, Design, and Tuning", ISBN-13: 978-1556175169

[18] Electromagnetic Compatibility (EMC), Integrated Circuits, Measurement of Electromagnetic Immunity 150 kHz to 1 GHz - Part 4: Direct RF Power Injection Method, IEC62132-4, 2007