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Synchronous Full-Adder based on Complementary Resistive Switching Memory Cells

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Abstract—Emerging non-volatile memories (NVM) such as STT-MRAM and OxRRAM are under intense investigation by both academia and industries. They are based on resistive switching mechanisms and promise advantageous performances in terms of access speed, power consumption and endurance (*i.e.* $>10^{12}$), surpassing mainstream flash memories. This paper presents a non-volatile full-adder design based on complementary resistive switching memory cells and validates it through two NVM technologies: STT-MRAM and OxRRAM on 40 nm node. This architecture allows low power consumption. Thanks to the non-volatility and 3D integration of NVM, both standby power during “idle” state and data transfer power can be reduced. Using a low changing frequency can also control the switching power of NVM. The complementary cells and parallel data sensing enable fast computation and high reliability.

I. INTRODUCTION

Modern computing systems suffer from rising static power due to high leakage currents which increase exponentially with the downscaling of Complementary metal–oxide–semiconductor (CMOS) technologies [1]. According to ITRS roadmap in 2012, the static power will play a predominant role in power consumption in the coming years [2]. In order to overcome this power issue, hybrid circuits integrating resistive switching non-volatile memory (NVM) are being investigated by both academia and industries. Due to their advantageous performances, Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM) [3] and Oxide Resistive RAM (OxRRAM) [4] are among the most promising NVM technologies. Indeed, as compared to conventional floating gate technologies, they provide fast write/read operations, low power consumption, CMOS compatibility and high endurance.

While these NVMs are based on different physical mechanisms, several common features exist. For instance, they consist in two terminal nanoscale devices; their resistance may be switched between ‘0’ and ‘1’ states; the memory cell may be integrated into back-end of line (BEOL) [5-8]. Recently, a number of innovative circuits based on hybrid Resistive Switching (RS) memory/CMOS circuits have been proposed. For example, magnetic look-up-table (MLUT) and non-volatile flip-flop (MFF & RS-NVFF) were introduced for reconfigurable logic circuits and normally off electronics [9-10]. A pre-charge sense amplifier (PCSA) [11] was presented and shows remarkable improvement in terms of reliability comparing with other SAs for RS memory cell sensing. In this context, resistive switching non-volatile full-adder (RS-

NVFA) based on hybrid technology could open the way towards ultra-low power and high density ICs [12]. Moreover, RS-NVFA could also overcome the communication bottleneck between separated logic module and memory block.

Magnetic Tunnel Junction (MTJ)-based RS-NVFA were proposed in the last years [13-15] and tested with conventional technology nodes. However they suffer from either high current for magnetic field generation or complex sensing circuit with capacitances. This paper presents a new full-adder design based on RS-NVM cells. Our design is validated by conducting transient simulations with two technologies: STT-MRAM and OxRRAM on 40 nm node. The rest of this paper is organized as follows: in the next section, the two technologies are briefly described and their compact models are introduced. The RS-NVFA architecture is detailed in section III. Section IV is devoted to transient simulations and performance analysis.

II. EMERGING RESISTIVE SWITCHING MEMORIES

Magnetic tunnel junction (MTJ) is the basic cell of MRAM and it consists of a thin insulating barrier (*i.e.* MgO) separating two ferromagnetic (FM) layers (Fig. 1a). Thanks to tunnel magneto-resistance (TMR) effect [16], its resistance, RP or RAP, depends on the relative orientation, Parallel (P) or Anti-Parallel (AP), of magnetizations in the two FM layers. STT is a switching mechanism promising high power efficiency and fast speed [2-3]. This mechanism enables profoundly simplifying CMOS circuitry, as only a bipolar current is required (Fig. 1b). MTJ switches as the passing current exceeds a given critical current noted I_{CO} . Recent progresses demonstrate that perpendicular magnetic anisotropy (PMA) provides a high-energy barrier E to face the thermal instability of in-plane anisotropy. It also presents lower switching energy (<0.1 pJ/bit@32 nm) and faster speed (<1 ns) [17-19].

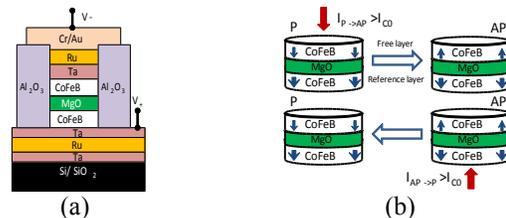


Figure 1. (a) Vertical structure of MTJ composed of CoFeB (1.3)/MgO (0.85)/CoFeB(2) thin films. (b) STT switching mechanism: the MTJ state changes either from P to AP as the electrons flow from the top ($I_{p \rightarrow ap} > I_{CO}$), or from AP to P as the electrons are injected from the bottom ($I_{ap \rightarrow p} > I_{CO}$).

TABLE I

PARAMETERS AND VARIABLES PRESENT IN THE FITTING FUNCTIONS		
Parameter	Description	Default Value
$Area$	MTJ surface	40 nm x 40 nm
$TMR(0)$	TMR ratio with 0 V_{bias}	120%
V	Volume of free layer	surface x 1.3 nm
$R \cdot A$	Resistance-area product	10 $\Omega\mu\text{m}^2$
V_{write}	Writing voltage	1.5 V
V_{read}	Reading voltage	1.2 V
$Jc0$	Critical current density	5.7×10^5 A/cm ²

A CoFeB/MgO/CoFeB PMA STT-MTJ compact model [20] taking into account related static, dynamic and stochastic behaviors was used to perform transient simulation [17-18]. Table I shows the critical parameters used in the model.

In its simplest form, an OxRRAM memory element relies on a Metal/Insulator/Metal (MIM) stack (Fig. 2a). The MIM structure is generally composed of metallic electrodes sandwiching an active layer, usually an oxygen-deficient oxide. A large number of resistive switching oxides, like HfO_2 , Ta_2O_5 , NiO , TiO_2 or Cu_2O , are reported in the literature [21-23]. An interfacial layer (IL, Fig. 2a) can also appear during the fabrication process. After an initial electroforming process, the memory element may be switched reversibly between a High Resistance State (HRS or OFF state) and a Low Resistance State (LRS or ON state). In this paper, we focus on bipolar switching RS-NVM. Bipolar voltages (positive or negative) over specific threshold voltage (*i.e.* V_{SET} and V_{RESET}) are required to switch the RS-NVM to OFF state or ON state (Fig. 2b).

Even if OxRRAM technology is still in its “infancy”, it is broadly accepted that the field-assisted motion of oxygen vacancies plays a predominant role in bipolar resistance switching [24]. The proposed OxRRAM modeling approach, deriving from a unipolar model [25], relies on electric field-induced migration of oxygen vacancies within the switching layer. This model enables continuously accounting for both set and reset operations into a single master equation and demonstrates its flexibility to match static (switching voltages, current levels) and dynamic behaviors of the most aggressive component from literature [26-28]. Tables II summarizes the cell operation parameters for very short programming pulse used for the OxRRAM-based NVFA transient simulations.

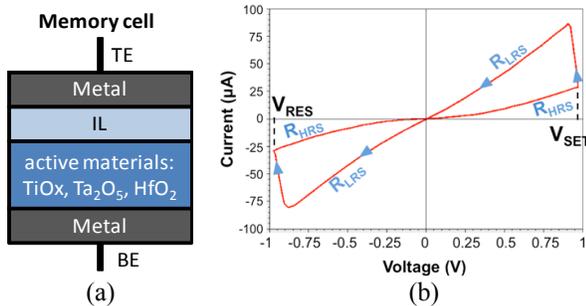


Figure 2. (a) OxRRAM memory stack with metal electrodes sandwiching an interfacial layer (IL) and an active material layer. (b) simulated current-voltage characteristic of a bipolar OxRRAM memory cell.

TABLE II
CELL OPERATION PARAMETERS.

Parameter	V_{TE} (V)	V_{BE} (V)	STATE
SET (Write)	0.95@5ns	0	ON->OFF
RESET (Erase)	0	-0.95V@5ns	OFF->ON
Read	<0.8@10ns	Sensing	ON or OFF

III. RESISTIVE SWITCHING FULL-ADDER ARCHITECTURE

For a 1-bit full-adder, the inputs are “ A ”, “ B ”, “ C_i ” and the outputs are “ SUM ”, “ C_o ”, calculated with the following Boolean equations:

$$SUM = A \oplus B \oplus C_i = ABC_i + A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i \quad (1)$$

$$C_o = AB + AC_i + BC_i \quad (2)$$

In the proposed architecture the input “ A ” is volatile computing data and input “ B ” is a critical data or quasi-constant. MOS transistors and RS-NVM are used to represent data “ A ” and “ B ”, respectively, in the addition. The switching frequency of “ B ” is much lower than “ A ” and “ C_i ”. The RS-NVFA architecture is composed of three parts: (i) a PCSA stage to evaluate the logic value of RS-NVFA outputs; (ii) a write logic block to program the RS memory cells; (iii) a CMOS logic tree including RS cells, implementing the addition sum and outputting carry. The general architecture is depicted in Fig. 3.

In order to evaluate the addition logic function, PCSA circuit enables providing the best sensing reliability and power efficiency while keeping high-speed performance (*e.g.* 200 ps) [11]. As shown in Fig. 4, it consists of pre-charge sub-circuit ($MP_{0,3,4,7}$), a discharge sub-circuit (MN_{16-17}) and a pair of inverters ($MN_{0-1,2,3}$ and $MP_{1-2,5-6}$), which act as current sense amplifier. The PCSA works in two phases: during the first phase, “ CLK ” is ‘0’, the RS-NVFA outputs (“ SUM ”, “ \bar{SUM} ” for the sum output and “ C_o ”, “ \bar{C}_o ” for the carry output) are pulled-up to “ V_{DD} ” or logic ‘1’ through $MP_{0,3,4,7}$ while MN_{16-17} remains off; during the second phase “ CLK ” is ‘1’, $MP_{0,3,4,7}$ are turned off and MN_{16-17} are on. In these conditions, the RS-NVFA outputs are pulled-down through the logic tree (MN_{4-15}) and the RS cells (B , \bar{B}). Depending on the MOS state in the logic tree and the RS element state, the discharge currents are different in both branches and the current sense amplifier latches opposite logic value on “ SUM ”, “ \bar{SUM} ” and “ C_o ”, “ \bar{C}_o ” respectively. While RS-NVFA outputs are evaluated through a differential process, the logic functions are implemented in two identical branches. However, in each branch, MOS transistors are controlled with complementary values and RS cells are programmed in opposite resistance states (*i.e.* R_{HRS} and R_{LRS}).

The RS devices are serially connected with a common central point. In order to generate bi-directional currents to program the complementary RS cells, write logic block, composed of pass transistors (MN_{18-23} and MP_{8-13} , see Fig. 4), is introduced. Pass transistors are connected respectively to bottom (BE) and top electrodes (TE) of the serial branch and to the common point.

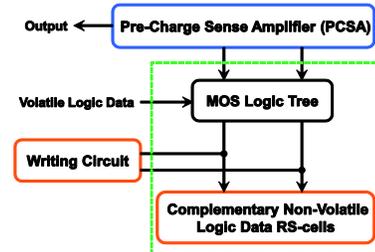


Figure 3. General architecture of RS-NVFA composed of PCSA, CMOS tree for volatile data and non-volatile memory cells for non-volatile data.

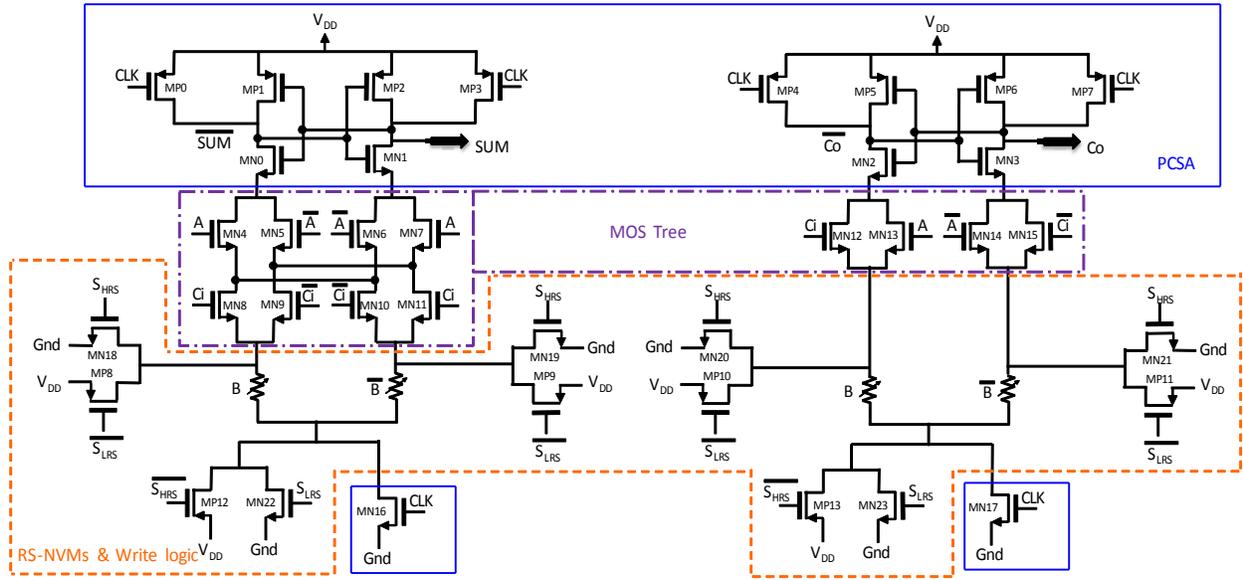


Figure 4. Resistive switching non-volatile full-adder architecture with SUM signal (left) and output carry Co (right) sub-circuit.

In such a manner, as a control signal (S_{LRS} or S_{HRS}) is activated, the first RS device noted B is put in R_{HRS} or R_{LRS} state while the second RS device noted \bar{B} is put in the complementary state R_{LRS} or R_{HRS} . Write circuitry can also serve as current limiting transistors to prevent excess currents during the electroforming of OXRRAM devices.

It is important to note that there is no capacitance for the data sensing and no magnetic field for data programming in this new structure, compared to the previous structures [12-14]. Thereby this design is suitable for advanced technological nodes below 90 nm and allows efficient area minimization.

IV. RS-NVFA VALIDATION WITH BIPOLAR STT-MRAM AND OXRRAM CELLS

This section presents transient simulation results to prove the architectural concept of RS-NVFA using our NVM compact models, shown in section II, and CMOS STMicroelectronics 40 nm design kit [29]. In the simulations, the size of transistors in PCSA and MOS tree is minimal while write circuit transistors are designed to reach SET and RESET states of RS cells.

Using our STT-MRAM compact model [20], we simulate the RS-NVFA architecture shown in Fig.4. Fig. 5 demonstrates the transient simulation results of the hybrid circuit. “CLK”=‘0’ drives the outputs “SUM” and “Co” to be pre-charged to “ V_{DD} ” or logic ‘1’, then the output evaluation will occur when “CLK” is set to ‘1’. We find that the behaviors of the outputs (“SUM” and “Co”) agree with the addition function for the whole truth table. For instance, as “A”=‘1’, “B”=‘0’, “Ci”=‘0’, the result will be ‘1’ and no carry yields; in another case, “A”=‘1’, “B”=‘0’, “Ci”=‘1’, “SUM” will be ‘0’ and the carry becomes ‘1’. It is important to note that the switching duration of input “B” for STT-MRAM cell is about 2 ns [20].

Similarly, the functionality of RS-NVFA circuit was checked through transient simulations with OXRRAM cells and CMOS STMicroelectronics 40 nm design kit [29] (Fig. 6). For OXRRAM cells, the switching time depends on write voltage dynamics. The simulation results obtained with our model [27] give a switching time less than 3 ns and resistance

values R_{HRS} =35.1k Ω and R_{LRS} =1.1k Ω . The outputs “SUM” and “Co” confirm the whole full-adder function. The sense delay is less than 60 ps for both outputs, showing high-speed performance of OxRRAM-based NVFA.

We summarize the performance comparison between three different simulations in Table III. The delay time and dynamic power of RS-NVFAs (with STT-MRAM and OxRRAM cells) are comparable to CMOS FA coming from standard cell library of STMicroelectronics [29]. It is advantageous in terms of standby power since our design allows to be powered off completely during “idle” state. Although its energy-delay product (EDP) exceeds that of CMOS full-adder by ~30%, then RS-NVFA could greatly reduce the whole consumption. Thanks to the 3D integration, the die area of our design (38 MOS + 4 RS cells) is more compact than the CMOS Full-adder (46 CMOS: 28 CMOS for asynchronous full-adder + 18 CMOS for synchronization) as the RS memories are on top of CMOS circuits. This integration allows also the elimination of dynamic power dedicated for data transfer (1 pJ/mm/bit@22 nm [2,30]) between logic units and memory array as the distance between memory and computing unit becomes some μ m instead of some mm for CMOS logic circuits [30].

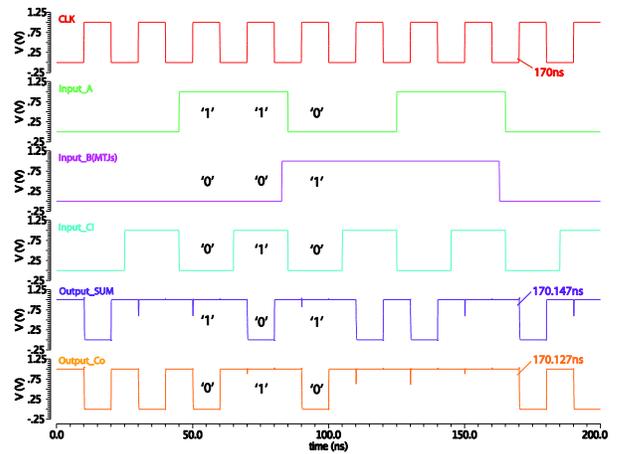


Figure 5. Transient simulations of RS-NVFA with STT-MRAM cells. Outputs are pre-charged as CLK is set to ‘0’ and are evaluated as CLK is set to ‘1’.

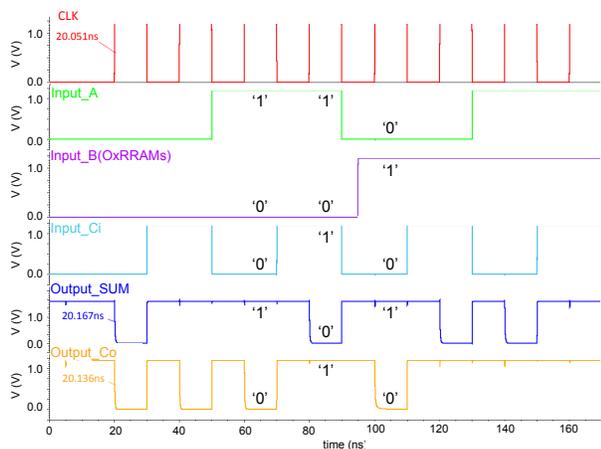


Figure 6. Transient simulations of RS-NVFA with OxRRAM cells. The simulation conditions are identical to those used in Fig. 5.

TABLE III
COMPARISON OF 1-BIT RS-NVFA WITH CMOS-ONLY FA @40 nm

Performance	CMOS-ONLY FA	STT-MRAM NVFA	OxRRAM NVFA
Delay time	75 ps	87.4 ps	52.3 ps
Dynamic power@ 500 MHz	2.17 μ W	2.44 μ W	3.50 μ W
Standby power	71 nW	\sim 0	\sim 0
Data transfer energy	>1 pJ	< 1fJ	< 1fJ
Die Area	46 MOS	38 MOS+ 4 MTJs	38 MOS+ 4 OxRRAMs

As mentioned above, a critical idea of this design shown in Fig. 4 is to use a programming frequency (e.g. 1 KHz) of RS-NVM much lower than the computing frequency (e.g. 1 GHz). Thereby, the switching power for non-volatile storage becomes insignificant to other power consumption in a full system.

V. CONCLUDING REMARKS

This paper presents a generic design of RS-NVFA based on complementary RS memory cells. Our RS-NVFA circuit is suitable for advanced technological nodes as there is neither capacitance nor magnetic fields compared to previous structures [11-15]. This architecture enables scaling down the die area and reducing the power as there is nearly zero standby power and low data transfer energy. It can be very useful for normally off electronics [19]. Using our STT-MRAM and OxRRAM compact models, RS-NVFAs were successfully simulated on 40 nm node and demonstrated their functionality and performance gain.

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