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Importance of complete characterization setup on on-wafer TRL calibration in sub-THz range

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Abstract— In this paper, we present the effect of different sub-mm and mm-wave probe geometry and topology on the measurement results of dedicated test-structures calibrated with on-wafer TRL. These results are compared against 3D EM simulation of the intrinsic test-structures. To analyze difference between the measured and intrinsic EM simulation results, on-wafer TRL calibration performed on EM simulation results of a dedicated test-structure is also presented.

Keywords—*Test-Structures; TRL calibration; characterization; EM simulation; HFSS; Sub-THz; SPICE*.

I. INTRODUCTION

With time, millimeter-wave and sub-millimeter wave are found suitable for diverse applications [1], [2] and require extensive research focus from high speed integrated devices to the system level design for full utilization of these frequency bands. To design a system working in the mm- and sub-mm range, development of an accurate SPICE model of the elementary devices is required. In development of a robust and precise SPICE model for the state-of-the-art high speed devices, its validation against device experimental data is indispensable. Accuracy of the used experimental data is essential to extract correct values of the compact model parameters and to use them further for circuit design. To obtain accurate experimental data, design of test-structures, de-embedding/calibration methods along with characterization techniques play a very important role at the sub-THz frequencies [3-5].

Calibration on Impedance Standard Substrate (ISS)-standard combined with Open-Short de-embedding method is an industry *de-facto* standard but it becomes less accurate above 30 to 40 GHz [6, 7]. More advanced de-embedding methods can be adopted to improve the accuracy [8-10] in cost of the complexity. To reduce reliance from less accurate off-wafer calibrations, to improve accuracy and repeatability of the measured data, on-wafer calibration technique enabling accurate characterization of high speed devices in sub-THz frequency range is highly desirable [11]. In this work, we have adopted thru-reflect-line (TRL) method for the on-wafer calibration of device-under-test (DUT), which is the reference

for on-wafer measurements at sub-mm wave and mm wave frequencies [12].

II. ON-WAFER CALIBRATION AND VERIFICATION STANDARDS

In order to perform on-wafer TRL calibrations, STMicroelectronics BiCMOS55 (B55) technology is used to design and fabricate all the test-structures [13]. The developed test-structures consist of nine metallic layers (copper in M1-M8 + Aluminum layer on top of M8 to realize contact pads) in back-end-of-line (BEOL). Our test-structures are compatible to perform characterization using 50 μm pitch probes and 100 μm pitch probes. In this work, used on-wafer test-structures (see Fig. 1 – Fig. 3) are as follows:

- Classical LINE
- THRU
- REFLECT
- LOAD (for impedance correction)
- Open-M1 (DUT)
- Short-M1 (DUT)
- Meander LINE (DUT).

To obtain high reflection, SHORT and OPEN are used as REFLECT standards. The fabricated classical straight LINE standard and THRU standard have line length equal to 115 μm and 35 μm , respectively.

To carry out 3D electromagnetic (EM) simulation of intrinsic test-structures and to perform on-wafer TRL calibration based on 3D EM simulations, test-structures layout design is imported into EM simulator.

III. EM SIMULATION SETUP

3D EM simulations have been carried out using Ansoft HFSS. In the simulation setup, test-structures placed on silicon substrate are encapsulated inside an air box and absorbing radiation boundary condition is assigned to the faces of the box. The radiation boundary condition emulates

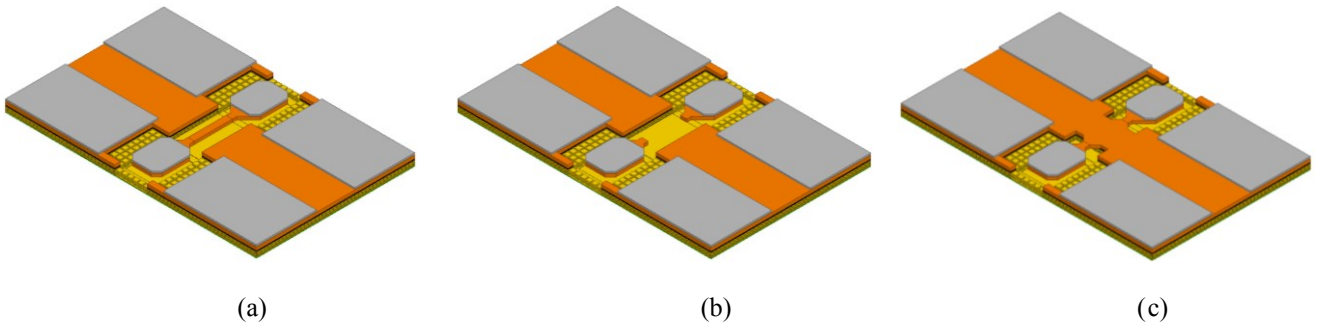


Fig 1: 3D view of THRU, OPEN and SHORT standards used in on-wafer TRL calibration are shown in panel (a), (b), and (c), respectively. Length of the THRU standard is 35 μm .

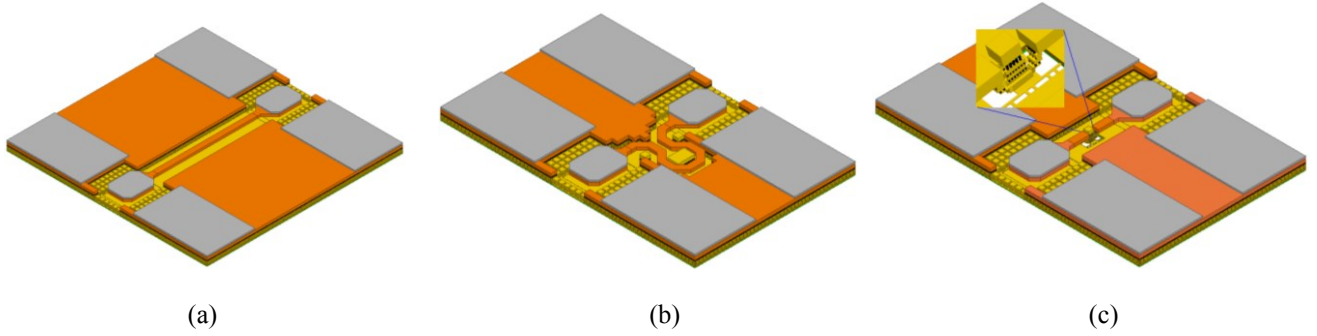


Fig 2: Test-structures used in on-wafer TRL calibration; (a) Classical LINE with 115 μm length, (b) Meander LINE, and (c) Short-M1 standard. In Short-M1, metal-1 (M1) is shorted to the ground as shown in the enlarged view. Meander LINE and Short-M1 are used as verification DUTs.

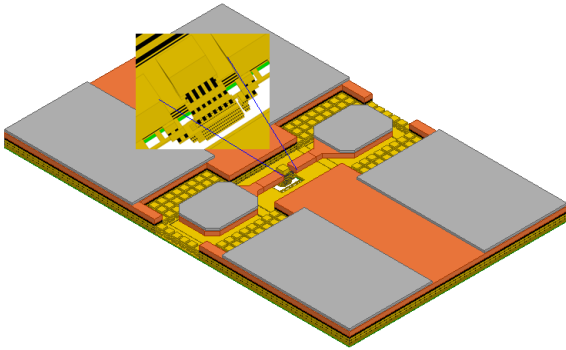


Fig 3: 3D view of the Open-M1 where metal-1 (M1) does not have connection with ground as shown in the enlarged view.

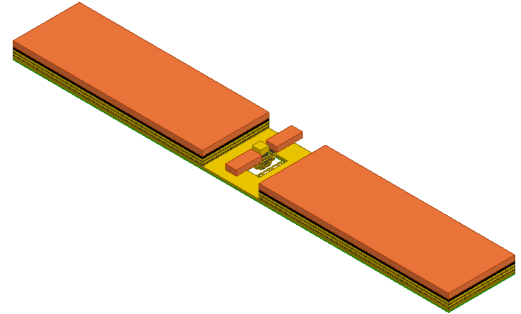


Fig 4: 3D view of intrinsic structure of Open-M1. Complete structure of Open-M1 including signal and ground pads is shown in Fig. 3.

infinite free space like environment during the simulation. In our test-structures design, intermediate insulator layers in back-end-of-line (BEOL) have different dielectric materials. However, in HFSS simulation, an average relative dielectric constant of 4.0 is set for all dielectric materials to reduce complexity. Other material parameter values, lateral and vertical dimensions of test-structures are chosen as per the structures' design. In the simulation, "wave port" is used to provide excitation at each port. To reduce simulation time in the simulation of symmetric test-structures, only half of the test-structure is used and "Perfect H" symmetry boundary

condition is assigned on the symmetry plane to obtain solution equivalent to complete structure. To perform EM simulation on intrinsic structures, only intrinsic parts of structures are taken into account (e.g. see intrinsic structure of Open-M1 shown in Fig. 4 in comparison to its complete structure shown in Fig. 3).

IV. RESULTS AND DISCUSSION

Using fabricated test-standards on the silicon wafer, first on-wafer TRL calibration is performed and the reference plane is



Fig 5: Image of the Picoprobe 50 μm pitch with waveguide used in G-band (140 GHz–220 GHz) measurement. Note that two other Picoprobes are also used in measurement but their images are not shown.

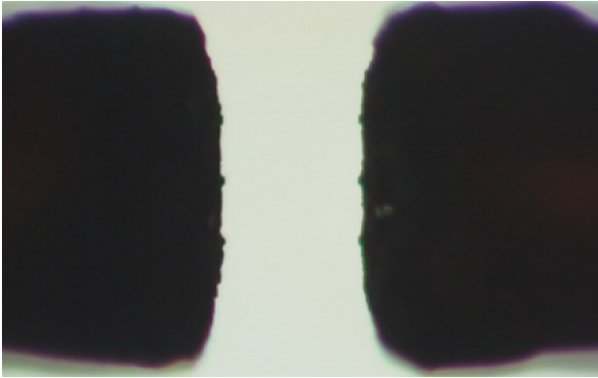


Fig 6: Image of the Cascade Infinity probe used in G-band (140 GHz – 220 GHz) measurement.

set after the pads (as can be recognized on the Open structure, see Fig. 1b). Next, test-structures such as the DUTs Open-M1, Short-M1 (dedicated to de-embedding) and Meander-LINE (see Fig. 2 and Fig. 3) are measured in two frequency bands i.e. 1 GHz – 110 GHz and 140 GHz – 220 GHz. To analyze the impact of the complete characterization setup combined with on-wafer TRL calibration, measurements are carried out using four different probes: 1) Picoprobe of 100 μm pitch (< 110 GHz), 2) Picoprobe of 50 μm pitch with coaxial cable (< 110 GHz), 3) Picoprobe of 50 μm pitch with waveguide (140 GHz - 220 GHz), and 4) Cascade Infinity probe of 100 μm pitch (140 GHz - 220 GHz) (see Fig. 5 and Fig. 6). In order to benchmark the on-wafer TRL calibration performed with different measurement configurations, 3D EM simulation is carried out first on the intrinsic structures. The results obtained after on-wafer TRL calibration and through intrinsic structures simulation in HFSS are shown in Fig. 7 – Fig. 11, where solid black line is used to represent the intrinsic structure EM simulation data and symbols are used to represent the DUT measured characteristics after on-wafer TRL calibration. In Fig. 7 and Fig. 8, magnitude and phase of reflection coefficient S_{11} of Open-M1 are shown up to 220 GHz. In the lower frequency range up to 60 GHz, all the results match reasonably, beyond 170 GHz a clear discrepancy can be obser-

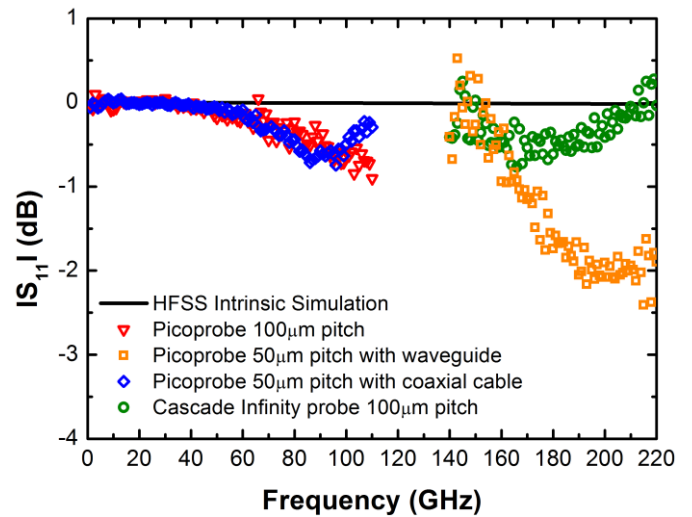


Fig 7: Magnitude of reflection coefficient S_{11} of Open-M1 w.r.t. frequency. Symbols are used to represent the measurement data and line is used for representation of intrinsic simulation performed in HFSS.

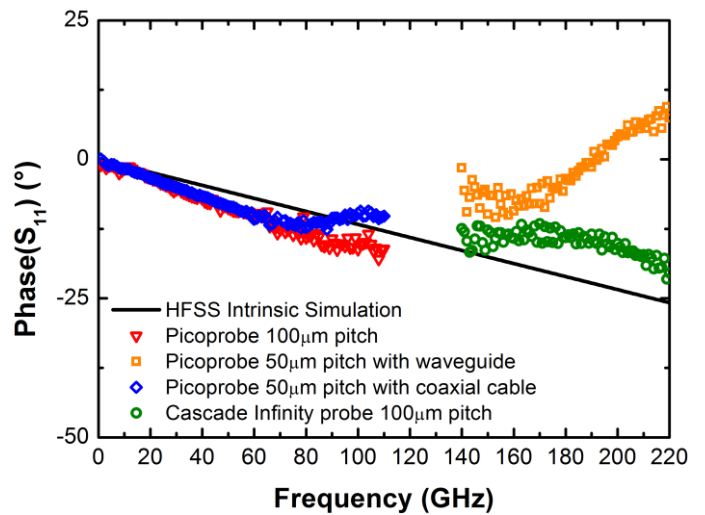


Fig 8: Phase of S_{11} of Open-M1 w.r.t. frequency. Symbols are used to represent the measurement data and line is used for representation of intrinsic simulation performed in HFSS.

ved. In particular, the combination of Picoprobe with 50 μm pitch and TRL on-wafer calibration seems to be not sufficient for accurate representation of the DUT's intrinsic behavior. The magnitude and phase of transmission coefficient S_{21} of a meander-line is shown in Fig. 9 and Fig. 10 up 220 GHz. For this DUT, the different measurement configurations give similar results except in the low frequency range for the Picoprobe with 100 μm pitch. A coupling with neighboring structures may be the origin of this non-ideal behavior. Inductance of the Short-M1 w.r.t. frequency is shown in Fig. 11. From 50 to 110 GHz, the Picoprobe with 100 μm pitch, and from 140-220 GHz, the Cascade-probe with 100 μm pitch, are matching well the theoretically predicted intrinsic DUT characteristic.

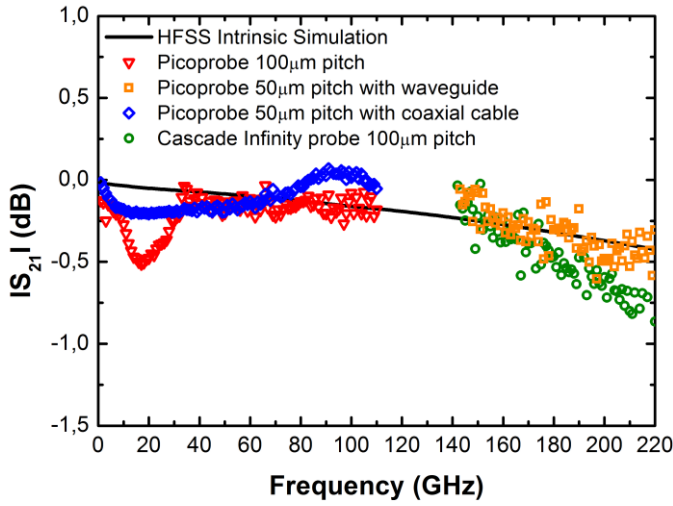


Fig 9: Magnitude of transmission coefficient S_{21} of meander-line w.r.t. frequency. Symbols are used to represent the measurement data and line is used for representation of intrinsic simulation.

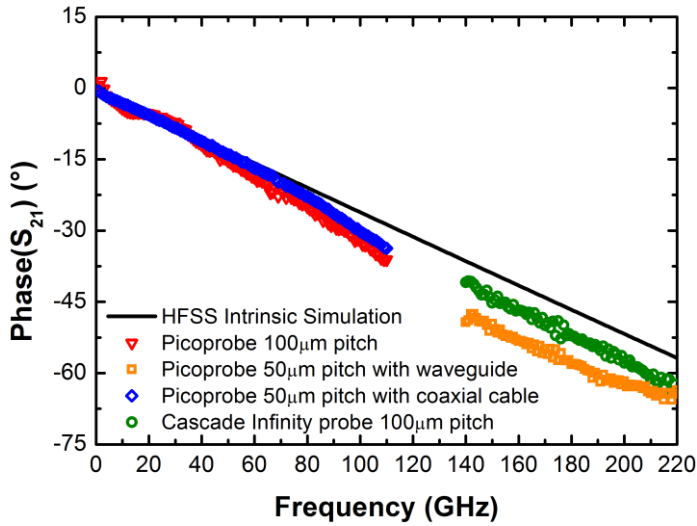


Fig 10: Phase of transmission coefficient S_{21} of Meander-LINE w.r.t. frequency. Symbols are used to represent the measurement data and line is used for representation of intrinsic simulation performed in HFSS.

In order to analyze differences between the intrinsic HFSS simulation results and measured data, we prepared 100 μm pitch probe model in HFSS based on the coplanar + coaxial topology (similar to Picoprobe with 100 μm pitch). Using the probe model, 3D EM simulations with and without neighboring structures are carried out on test-structures shown in Figs. 1 – 3. After performing on-wafer TRL calibration on EM simulation data, magnitude of reflection coefficient S_{11} of Open-M1 is shown in Fig. 12. From Fig. 12, it can be observed that HFSS probe model gives different results than the intrinsic simulation and upto some extent mimic behavior of measurement data of Fig. 7. From Fig. 12, it can also be observed that measurement results are more prone to probe design and presence of neighboring structures around DUTs at higher frequencies. Therefore, effects predicted by calibrated

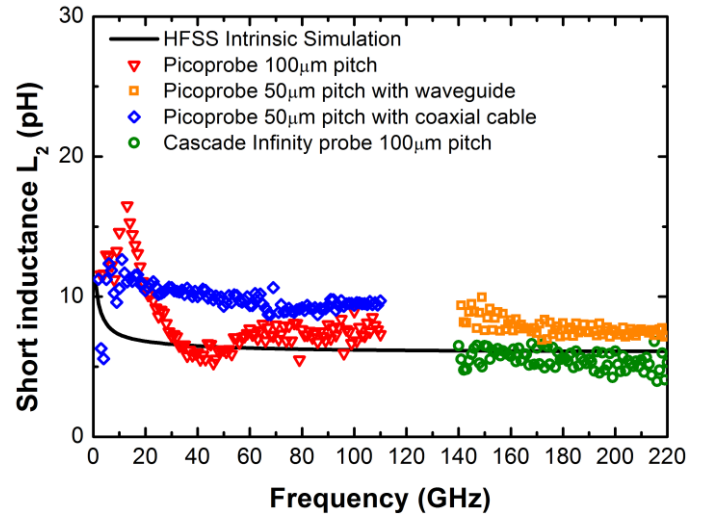


Fig 11: Inductance of the Short-M1 with respect to frequency. Symbols are used to represent the measurement data and line is used for representation of intrinsic simulation performed in HFSS.

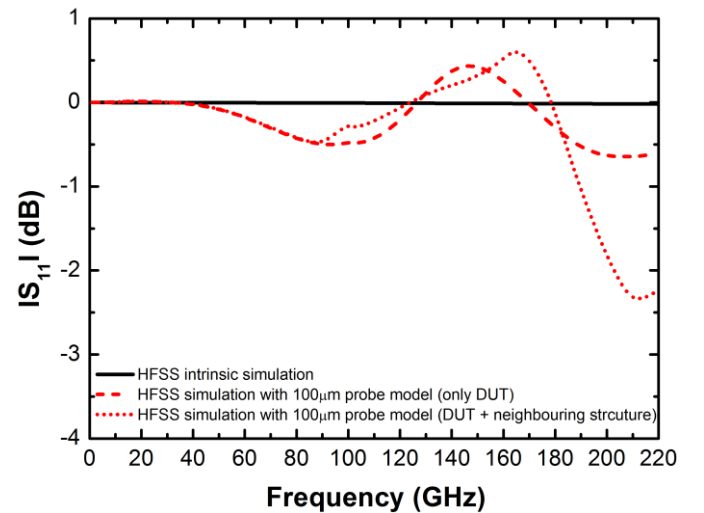


Fig 12: Comparison of reflection coefficient S_{11} of Open-M1 w.r.t. frequency. These results are obtained from EM simulation of intrinsic structure and on-wafer calibration performed on EM simulation of complete structure. Differences between intrinsic simulation and simulation using probe model has very similar pattern as observed in Fig. 7 between the measured data and intrinsic simulation. Simulation with and without neighboring structure around DUT indicates surrounding condition can impact the measurement.

EM simulation results shown in Fig. 12 could be the possible reasons behind difference between the intrinsic simulation and measured data visible in Fig. 7 – Fig. 11. In addition, these results also show importance of the complete characterization setup in the on-wafer TRL calibration.

V. CONCLUSION

In conclusion, we want to point out that considering intrinsic simulation data as a reference, we observe that after on-wafer TRL calibration the measurements of dedicated test-structures

using different probes topologies (i.e. based on coplanar and microstrip) give different results. It is interesting to see that after on-wafer TRL calibration the measurements done on the same DUT with same probe topology but with different pitch also shows variation in results as frequency increases. These results show the importance to take into account the complete characterization setup when performing on-wafer TRL calibration. In particular, depending on the design of the test-structures together with the probe geometry, on-wafer TRL calibration is not sufficient for some particular cases and coupling correction becomes mandatory.

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REFERENCES

- [1] T. W. Crowe, W. R. Deal, M. Schröter, C. K. Clive Tzuang and K. Wu, "Terahertz RF Electronics and System Integration [Scanning the Issue]," in *Proceedings of the IEEE*, vol. 105, no. 6, pp. 985-989, June 2017.
- [2] M. Tonouchi, "Cutting-edge terahertz technology" *Nature photonics*, pp. 97-105, Feb. 2007.
- [3] A. M. Mangan, S. P. Voinigescu, Ming-Ta Yang and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," in *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 235-241, Feb. 2006.
- [4] A. Issaoun, Y. Z. Xiong, J. Shi, J. Brinkhoff and F. Lin, "On the Deembedding Issue of CMOS Multigigahertz Measurements," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 9, pp. 1813-1823, Sept. 2007.
- [5] P. Manuel, S. Fregonese, A. Curutchet, P. Baureis and T. Zimmer, "New 3D-TRL structures for on-wafer calibration For high frequency S-parameter measurement," *2015 European Microwave Conference (EuMC)*, Paris, 2015, pp. 167-170.
- [6] M. Potereau, C. Raya, M. D. Matos, S. Fregonese, A. Curutchet, M. Zhang, B. Ardouin, et T. Zimmer, "Limitations of On-Wafer Calibration and De-embedding Methods in the Sub-THz Range", *J. Comput. Commun.*, vol. 01, no. 06, pp. 25-29, 2013.
- [7] C. Raya and B. Ardouin, "Méthodes de caractérisation en hautes fréquences des technologies de circuits intégrés en silicium dédiées aux applications Téra hertz et sub-Téra hertz, " *Proceedings of Journées Scientifiques 2013*, Paris, France.
- [8] F. Pourchon, C. Raya, N. Derrier, P. Chevalier, D. Gloria, S. Pruvost, et D. Céli "From measurement to intrinsic device characteristics: Test structures and parasitic determination," *2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Monterey, CA, 2008, pp. 232-239.
- [9] N. Derrier, A. Rumiantsev, and D. Celi, "State-of-the-art and future perspectives in calibration and de-embedding techniques for characterization of advanced SiGe HBTs featuring sub-THz f_T/f_{MAX} ", in *2012 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2012, pp. 1-8.
- [10] M. Potereau, M. Deng, C. Raya, B. Ardouin, K. Aufinger, C. Ayela, M. De Matos, A. Curutchet, S. Frégonèse, T. Zimmer, "Meander type transmission line design for on-wafer TRL calibration," *2016 46th European Microwave Conference (EuMC)*, London, 2016, pp. 381-384.
- [11] A. Rumiantsev, S. L. Sweeney and P. L. Corson, "Comparison of on-wafer multiline TRL and LRM+ calibrations for RF CMOS applications," *2008 72nd ARFTG Microwave Measurement Symposium*, Portland, OR, 2008, pp. 132-136.
- [12] D. F. Williams, P. Corson, J. Sharma, H. Krishnaswamy, W. Tai, Z. George, D. Ricketts, P. Watson, E. Dacquay, and S. P. Voinigescu, "Calibration-Kit Design for Millimeter-Wave Silicon Integrated Circuits," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 7, pp. 2685-2694, July 2013.
- [13] P. Chevalier *et al.*, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz f_T / 370 GHz f_{MAX} HBT and high-Q millimeter-wave passives", in *Electron Devices Meeting (IEDM), 2014 IEEE International*, 2014, p. 3.9.1-3.9.3.