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Dc and ac electrical response of MOCVD grown GaN in p-i-n structure, assessed through I - V and admittance measurement

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Abstract. The electrical response of gallium nitride (GaN), produced through metal-organic chemical vapor deposition in p-i-n structure was investigated through temperature-dependent current-voltage (I - V) and admittance measurement. The I - V curves showed double diode behavior together with several distinct regions in which trap-assisted tunnelling current has been identified at low and moderate forward/reverse direction and space charge limited current (SCLC) at large forward/reverse bias. The value of extracted energy (~ 200 meV in forward and ~ 70 meV in reverse direction) marked the tunnelling entity as electron and heavy hole in the present structure. These values were also obtained in space charge limited regime and considered as minority carriers which might originate the experimentally observed negative capacitance issue at low frequencies over the junction under both forward and reverse bias directions. Analytically derived expression for the admittance in the revised versions of SCLC model was also applied to explain the inductance effect, yielding good fits to the experimentally measured admittance data.

Keywords: Temperature-dependent current-voltage characteristics, Capacitance voltage characteristics, P-i-n diodes, Gallium nitride, Trap-assisted tunnelling current.
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1. Introduction

Due to its wide band gap and chemical stability, gallium nitride (GaN) is a promising material for applications in high-power and high-temperature electronic devices [1]. Meanwhile, GaN is a convenient material which is used in the light emitting devices operated in the blue and ultraviolet spectral ranges [2]. As a consequence of that GaN-based light emitting diodes (LEDs) shall be used in Refs. [3, 4] as general illumination sources instead of incandescent and fluorescent lamps [5]. In addition, GaN-based semiconductor is also investigated as optical detectors in the long wavelength (1.2 to 1.6 μm) light wave telecommunication. Mostly, these diodes show significantly high dark currents under reverse biases which limits their sensitivity in usage of photodetectors.

In this work, we present tunnelling of heavy holes is a major source of leakage current under reverse bias condition. Additionally, dependence of current on temperature and bias voltage are in agreement with the tunnelling [6, 7]. At large reverse bias voltages, power-law dependence verified the presence of space charge limited conduction mechanism. Under whole forward bias condition, that LED devices require to obtain sufficient carrier injection, electron as the tunnelling entity is identified. Remarkably, double diode behavior is observed together with several distinct regions in which trap-assisted tunnelling current has been identified at low and moderate forward bias and SCLC at large one [8, 9, 10, 11]. The extracted energy value in SCLC regime claims that electrons are still the tunnelling entity and behave as minority carriers within p^+/p -layer and might originate the experimentally observed negative capacitance issue at low frequencies

in admittance data, so called SCLC model in the literature [12]. Analytically derived admittance expression in the revised version of SCLC model by Ehrenfreund et al. [13] was applied to explain the inductive effect yielding good fits to the experimentally measured admittance data. In this work, it is worth to note that inductance manifested not only in forward bias direction, but also in the reverse one that is reported in the work of Perera et al. [14] where interface-mediated recombination is the origin of observation of negative capacitance, as given in the Refs. [3, 13, 15, 16, 17, 18, 19, 20]. The expression they used corresponds to the additive term in the revised version of SCLC model. These two mentioned source (minority carrier injection and presence of recombination phenomena) might cause to get inductance effect in admittance data of present p-i-n junction.

2. Experimental methods

Four samples were produced through using a metal-organic vapor phase epitaxy (MOVPE) technique. These structures consisted of 1.8 μm not intentionally doped (NID) layer, 1 μm n-layer with Si-doped ($5 \times 10^{18} \text{ cm}^{-3}$), an undoped layer and 0.27 μm p^+/p -layer with Mg-doped ($1 \times 10^{17} \text{ cm}^{-3}$). Schematic structure of the GaN-based p-i-n structure was depicted as the inset of Fig. 1(a) where the thicknesses of undoped GaN layer were 0.6 μm and 0.2 μm for Q10-E1/Q10-H2 and Q9-E2/Q9-H2, respectively. The mesa was dry etched, using $\text{BCl}_3/\text{Cl}_2/\text{N}_2$ inductively coupled plasma reactive ion etching, to reach the n-layer. A thin spreading layer of palladium (Pd) and gold (Au) (20 nm / 20 nm) was deposited as a p-contact, over an area of $4 \times 4 \text{ mm}^2$. The n-contact was made of titanium (Ti), aluminum (Al) and gold (Au) (10 nm/ 30

nm / 300 nm). To ensure good ohmic contacts, the diodes are finally rapid thermal annealed under N_2 atmosphere.

In the experiment, forward bias condition was satisfied when the Pd/Au contact was wired (+) terminal and Ti/Al/Au contact was wired (-) terminal. For a temperature-dependent current-voltage measurement, Keithley 2400 source meter, equipped with Lake Shore 334 temperature controller, was used. An HP4192A LRC-meter operated in the frequency range $f = \omega/2\pi = 7\text{-}10^6$ Hz was employed to measure the admittance (Y) from which the capacitance $C \equiv \text{Im}[Y(\omega)/\omega]$ and the conductance $G(\omega) = \text{Re}Y(\omega)$ were extracted.

3. Results

Room temperature current-voltage (I - V) characteristic are obtained through I - V measurement within dark ambient at room temperature and illustrated in Fig. 1(a). Clearly, the junction possesses diode characteristic with poor rectification. Moreover, as anticipated though Fig. 1(b), different exponential current regimes are clearly identified in the forward bias voltage curves, denoting multiple types of transport of carriers across the junction i.e., double diode behavior [8, 9, 10, 11]. In such case, one of the ways to identify the number of equivalent diodes and the behavior of each of these diodes are to plot the first derivative of the logarithm of the current against voltage rather than the logarithm of current versus voltage (see Fig. 1(b)). Through this approach (see Fig. 1(b)), not only peak values are obtained for the electrical transport of each of diodes, but also the associated bias voltage interval is precisely determined. Although both of them contribute to the I - V characteristic, each one is dominant at a certain volt-

age range, and hence three bias intervals are exhibited and show the presence of different carrier conduction mechanism. The interval of $0.4 < V_F < 2.2$ V is attributed to low voltage, $3.0 < V_F < 4.5$ V is ascribed to intermediate voltage interval and $V_F > 5.0$ V denotes the space charge limited region.

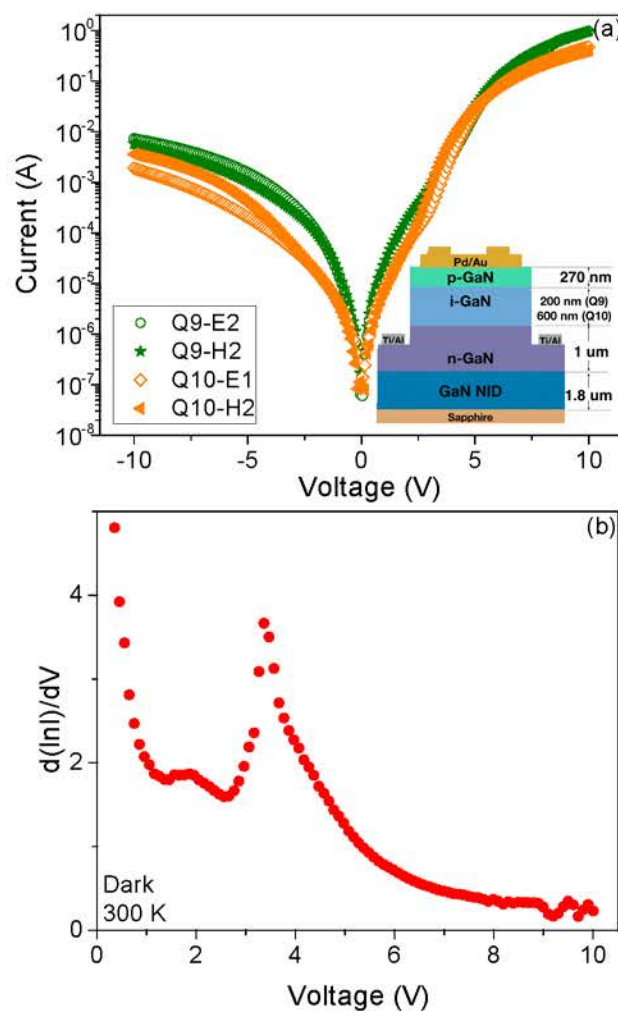


Figure 1. (a) Current-voltage characteristics of GaN p-i-n diodes within dark ambient at room temperature, (b) demonstration of double diode behavior, i.e., first derivative of logarithm of current against voltage curve, on Q10-E1.

3.1. Temperature-dependent current-voltage measurement of GaN p-i-n diodes

To discern the charge carrier path, a general diode equation is fitted and the results are analyzed in terms of activation energy of the saturation currents, I_0 , and temperature dependence of the exponential factor, $A(= q/nkT)$, by performing temperature-dependent current-voltage measurement. Fig. 2 shows temperature-dependent I - V measurements within the studied temperature range from 300 to 400 K at 10 K intervals. Considering the general expression of current-voltage relation as

$$I = I_0 \exp[A(T)V - 1] \quad (1)$$

with

$$I_0(T) \propto \exp\left(\frac{E_A}{kT}\right) \quad (2)$$

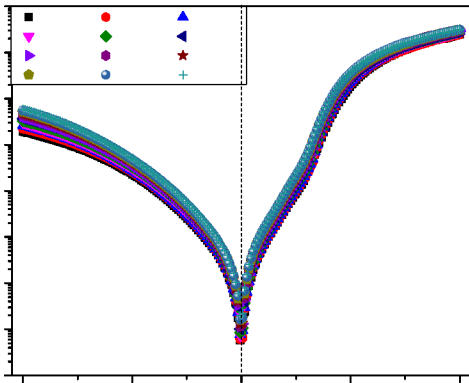


Figure 2. Temperature-dependent current-voltage characteristics of GaN p-i-n diodes within dark ambient.

where $I_0(T)$ and $A(T)$ are temperature-dependent quantities that represent the governing current mechanism [21]. Transport models and their functional form of $I_0(T)$ and

$A(T)$ are given in Table.1. Clearly, temperature dependence of $I_0(T)$ and $A(T)$ differs as to the transport model. In general, diode quality (n) of unity together with energy band gap (E_G) value of semiconductor as activation energy (E_A) indicates diffusion kind conduction mechanism. For the recombination type carrier conduction, one expect n as 2 with $E_A \simeq E_G/2$. Furthermore, temperature independent A with unrealistic quality factor ($n > 2$) shows tunnelling type carrier conduction [22].

3.1.1. Forward Bias Condition Forward I - V characteristic of the p-i-n structure demonstrates two main exponential region at low and intermediate bias region (see Fig.3). From the slope of straight line, diode quality factor and saturation current is extracted. In order words, through variation of $A(= q/nkT)$ versus $1/T$ and $\ln I_0$ versus $1/T$, shown in Fig.3, diode quality factor and activation energy are obtained. Temperature insensitive of A together with unrealistic quality factor are characteristic of tunnelling current in the p-i-n structure. The activation energy for the first region (at low voltage) is determined 75 meV for the moderate temperature interval while it is 120-140 meV at high temperature side. For the second exponential regime, E_A is obtained as 208 meV with temperature insensitive of A , proving tunnelling type conduction continues for the intermediate bias voltage interval. These E_A values are in good agreement to those that have been previously reported as a characteristic energies in tunnelling process for electron (120-220 meV) [4, 7, 23] and heavy hole (50-80 meV) [4]. Upon V_F exceeds 5.0 V ($V_F > 5.0$ V), another conduction mechanism, namely space charge limited regime, appears in I - V curves.

Table 1. Transport models and their functional form for I_0 and A .

Model	$I_0(T)$	$A(T)$	n
Schottky diffusion	$T^{3+\gamma/2} + e^{-E_g/kT}$	q/kT	1
Generation/Recombination	$T^{3+\gamma/2} + e^{-E_g/2kT}$	$q/2kT$	2
Thermionic emission	$T^2 e^{-\Phi_B/kT}$	q/kT	1
Multi tunnelling capture emission	$e^{-(E_T-E_V)/kT} - e^{-(E_C-E_T)/kT}$	constant	>2

3.1.2. Reverse Bias Condition In the reverse bias direction (see Fig.4) activation energies are determined as 80 meV and 144 meV for low bias voltages ($V_R < 1.3$ V). For the reverse bias interval of 1.3 and 2.3 V, temperature invariant A shows tunnelling kind conduction mechanism with an activation energy as 60 meV. At large reverse bias voltages ($2.3 < V_R < 10$ V), power-law dependence ($I \sim V^{3.5}$) indicates the presence of space charge limited currents in the third region. Remarkably, tunnelling type conduction process occurs in the reverse direction and reported in the literature [6, 7, 24, 25].

3.2. Admittance measurement of GaN-based p-i-n structure

Admittance measurements are performed over the four samples and one of them (Q10-E1) is selected for presentation. Room temperature C - V characteristic of GaN-based p-i-n structure is depicted in Fig. 5 within the frequency range of 1 kHz-1 MHz. In the C - V experiment, the bias voltage is scanned from negative to positive side, i.e., from reverse to forward bias direction. As shown in Fig. 5, bias and frequency independent capacitances are eventual for the bias range of -10 V up to 2 V. The value of capacitance (2.2 nF) denotes each p- and i-layer's capacitance, determined by the geometry and dielectric constant by

$C = 9.5\epsilon_0 S / < d >$, that is connected in series and hence total measured capacitance is given by

$$C_m^{-1} = C_{t,p^+/p}^{-1} + C_{t,i}^{-1} \quad (3)$$

where $C_{t,p^+/p}$ and $C_{t,i}$ correspondence to the geometric capacitances of p⁺/p- and i-layers of the present structure. In reverse and small forward bias voltage, apparent frequency invariant property at the 1 kHz-1 MHz range with a constant value of capacitance shows that the structure is in depleted/inverted regime so the measured capacitance is independent of bias voltage (see Fig. 5(a)). As the bias is increased from 2 V to 4 V, measured capacitance begins to rise gradually towards 5 nF, corresponding to geometric capacitance of p⁺/p-layer. Remarkably, the step in capacitance has frequency-dependent. Moreover, it also shows the reduction in distance among parallel plate capacitor, i.e., $< d >$ decreases. After that sharp increase in capacitance is eventual within a narrow bias voltage interval (in between 4.5 to 5.5 V). After reaching a maxima, the measured capacitance begins to decline. Obviously, the maxima shifts to lower bias voltage, when f decreases in C - V curves. Moreover, it is worth to note that sharp increase reaching a maxima and reduction in capacitance features is totally occurred within p⁺/p-layer in the p-i-n structure. The voltage dependence of the measured conductance

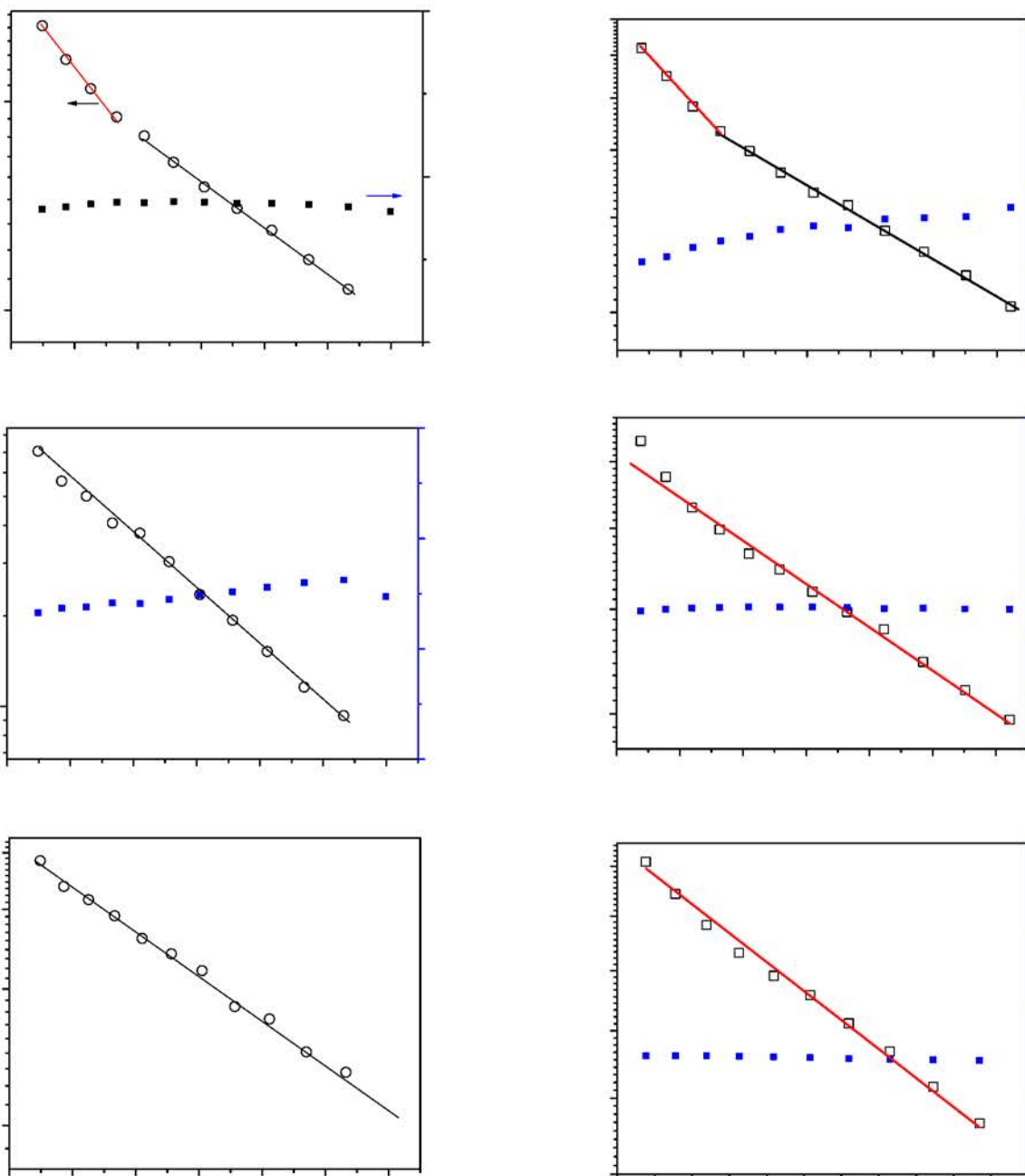


Figure 3. Temperature variation of both I_0 and A of GaN p-i-n diode for the bias intervals: (a) $0.4 < V_F < 2.6$ V (b) $3.0 < V_F < 4.5$ V and (c) $V_F > 5.0$ V.

Figure 4. Temperature variation of both I_0 and A of GaN p-i-n diode for the reverse bias intervals: (a) $0.1 < V_R < 1.3$ V (b) $1.3 < V_R < 2.3$ V (c) $2.3 < V_R < 8.0$ V.

(shown in Fig. 5(b)), on the other hand, follows that of the static conductance (dI/dV) in which $G(V) \propto dI/dV$ for the entire bias range, supporting the consistency of dc (from

the I - V measurement) and ac (from the admittance spectroscopy) experiment results. For the small frequency range ($1 < f < 1000$ Hz),

$G/C-V$ characteristic is displayed in Fig. 5(c) and Fig. 5(d), respectively. Under the reverse bias direction at low values, a hump appears in $C-V$ plot (see also the inset in the Fig. 5(d)) while at large reverse bias voltage, the geometric capacitance begins to decline even below zero whence frequency decreases from 1000 Hz to 7 Hz. Log-log variation of conductance reverse bias voltage, depicted in Fig. 5(c), demonstrates three bias ranges as in the reverse $I-V$ characteristic without frequency-dependent feature.

Apart from bias dependence, frequency variation of capacitance is presented for the predetermined bias voltages under the forward/reverse direction and depicted in Fig. 6 and Fig. 7. For the first bias region in the forward direction ($1.0 < V_F < 2.6$ V), C versus $\log f$ curve (shown in Fig. 6(a)) indicates a frequency dispersed capacitance step; varying from high capacitance value (~ 12 nF) at low-frequency (7 Hz) to geometric value (2.2 nF) at high-frequency (1 kHz and above). Moreover, the step has bias-dependent; as the bias gets larger from 1 V to 2.6 V, the saturated capacitance grows in values and differs from the geometric capacitance of $p^+/p-$ and i -layers of present structure towards the location within interior region in p^+/p -layer, turning the $p-i-n$ structure to an Schottky one. For the second bias region in the forward direction ($3.0 < V_F < 4.5$ V), frequency-dependent capacitance of a $p-i-n$ structure as a function of bias voltage is displayed in Fig.6(b). As shown, the negative contribution to the measured capacitance exists and its effect becomes more pronounced at higher forward bias voltages as the frequency decreases. Moreover, onset of negative contribution to the capacitance moves to the higher frequencies when applied bias increases. Furthermore, above 1 kHz, negative capacitance issue disappears and saturates

around 3 nF that roughly corresponds to the geometric capacitance of $p^+/p-$ and i -layers of present structure.

As the forward bias is further increased ($V_F > 5.0$ V), the behavior changes drastically and presented in Fig.6(c); it shows a minimum at a distinct frequency. The minimum shifts to higher values as the bias increases and additionally it strongly increase towards low frequency, indicating presence of dispersive transport [19, 26] that would be discussed in the next section. Remarkably, similar characteristics are observed in negative biases, and is illustrated in Fig. 7 for the predetermined reverse bias voltage intervals.

4. Discussion

Temperature-dependent current-voltage and admittance measurement were performed to find out dc and ac electrical properties of the GaN-based $p-i-n$ structure at hand. Several distinct regions were observed at the forward bias direction. In the low forward bias range (called as region I), temperature independent A together with unrealistic quality factor suggested tunnelling kind carrier transport [4, 7, 8, 24, 27]. Also, the activation energies, which is deduced plotting $\ln I_0$ versus $1/T$ (Arrhenius plot), were determined as 75 meV and 114 meV at the moderate and high temperature intervals. They were the characteristic energies for heavy hole and electron in tunnelling current of GaN $p-n$ junction [4, 7, 24, 27]. The activation energy value of 208 meV of intermediate bias range (region II) and temperature insensitive of A were obtained, proposing electron tunnelling and it reinforced the proposition.

For the bias value greater than 5 V, space charge limited conduction process was discerned. As the tunnelling entity, electron

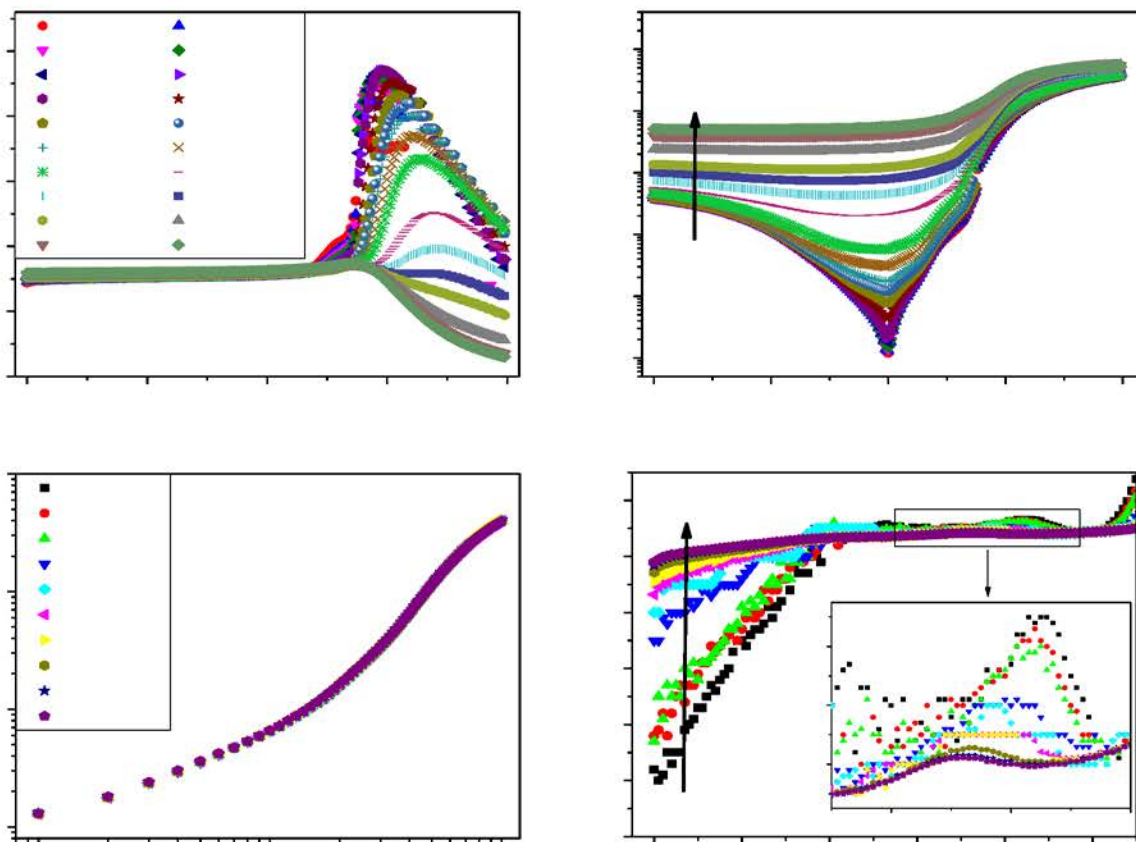


Figure 5. (a) The capacitance-voltage (b) the conductance-voltage curves in the frequency range of 1 kHz-1 MHz and (c) the conductance-voltage (d) the capacitance-voltage curves in the frequency range of 0.07-1 kHz of GaN p-i-n structure at room temperature.

was identified since activation energy was determined as 117 meV. In reverse bias direction, three bias intervals were shown as in the forward case; at low values, two activation energies were obtained as 144 meV and 80 meV for the first region and they were attributed as electrons and holes as tunnelling entity. For an intermediate bias interval and space charge limited region, the extracted activation energy implied that hole was the tunnelling entity. Also, the power-law dependence ($I_R \propto V^{3.5}$) verified the presence of space charge limited currents, taking place in the third region at reverse bias direction.

The presence of tunnelling current at

forward/reverse bias direction implied the existence of trap-assisted (probably Mg related [24, 28, 29, 30, 31, 32]) multi-step tunnelling as the carrier conduction mechanism for the present GaN-based p-i-n structure [8, 33]. On other hand, for the intermediate and large bias values, electrons (holes) tunneled in the forward (reverse) direction and this carrier behaved as minority carrier in the present structure. $C-V$ curves revealed that the measured capacitance corresponded to the charge present within interior region of p-layer of present p-i-n structure, where electrons were considered as minorities. This was hold for reverse bias direction as well in which holes

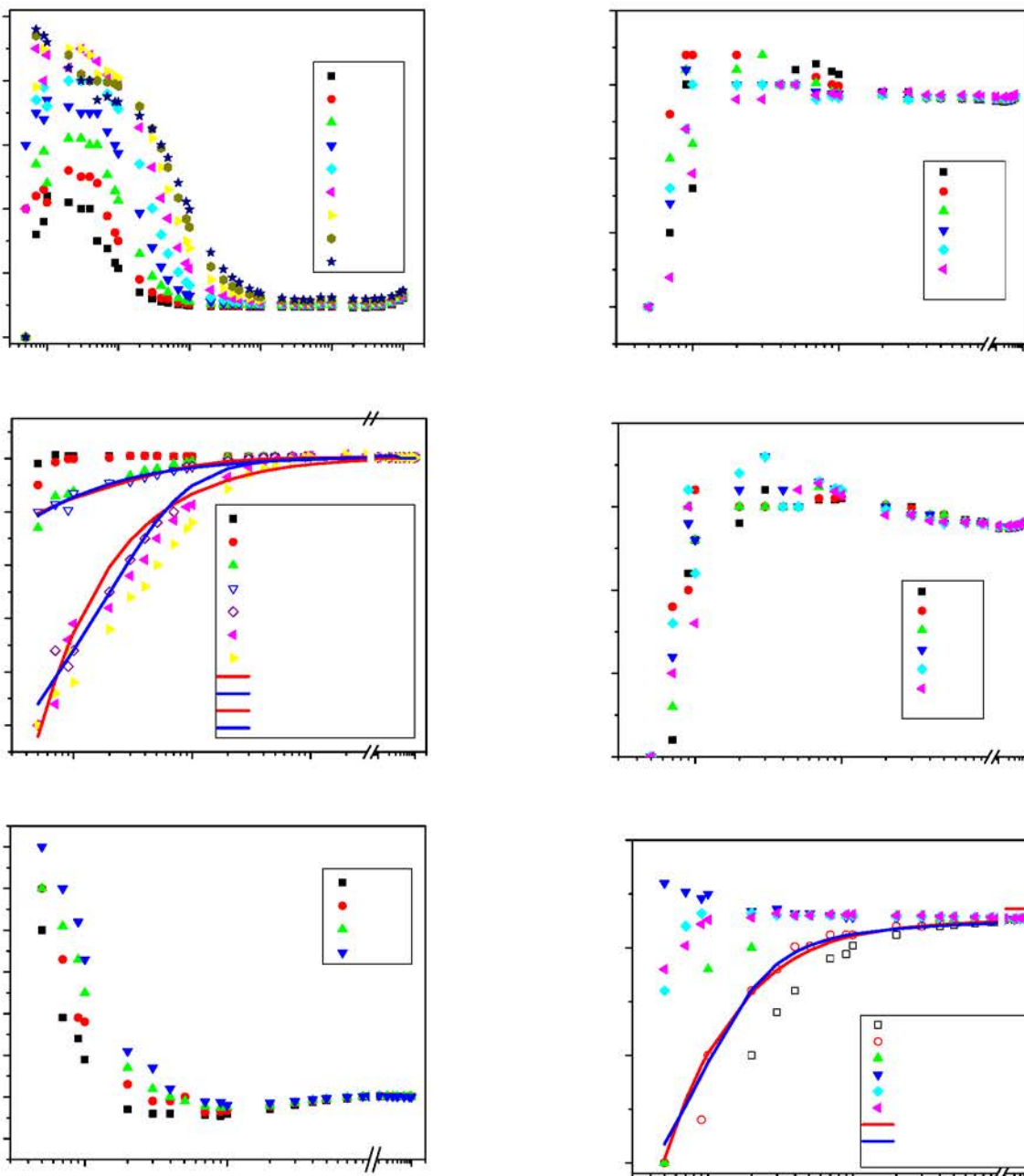


Figure 6. The capacitance-frequency curves of GaN-based p-i-n structure for the forward bias intervals: (a) $1.0 < V_F < 2.6$ V (b) $3.0 < V_F < 4.5$ V (c) $5.0 < V_F < 5.7$ V.

Figure 7. The capacitance-frequency curves of GaN-based p-i-n structure for the reverse bias intervals: (a) $0.1 < V_R < 1.3$ V (b) $1.3 < V_R < 2.3$ V (c) $2.3 < V_R < 8.0$ V.

were minorities within i-layer of the structure. Minority carrier injection and trap-mediated tunnelling/recombination originated from the

eventual inductance effect in admittance measurement. Therefore, capacitance together with conductance-voltage characteristics of

the GaN-based p-i-n structure over a wide frequency (7 Hz-1 MHz) at room temperature were presented in Fig. 5. We presented the bias dependence of admittance measurement in two part; one was in between 1 kHz and 1 MHz range, while the other was in the range of 7 Hz-1000 Hz. In the range of 1 kHz-1 MHz frequencies, striking feature of $C-V$ measurement was in the positive bias voltage (forward bias condition) where capacitance went over a peak and decreased as the bias was further increased. Also, the capacitance was completely negative for the frequency above 2 MHz (not shown). Meanwhile, bias dependence of conductance exhibited similar feature as in $I-V$ curves at low-frequencies and demonstrated the bias intervals that were used in $I-V$ curves in the forward/reverse directions. In the negative values of bias voltage, on the other hand, apparent stagnant value of capacitance (around 2.2 nF) for the frequencies 1 kHz-1 MHz range showed drastically different feature, in which negative capacitance was clearly observed (see Fig. 5(d)) beyond -7 V. Also, barely seen hump in $C-V$ curves within the bias interval of 1 and 2 V was highlighted and presented as the inset of Fig. 5(d), indicating a transition of junction limited to bulk limited process under reverse bias condition. Negative capacitance became more pronounced when f decreased towards 7 Hz. Conductance variation, on the other hand, manifested slight dependence over frequency compared to capacitance changes and depicted in Fig. 5(c).

On the other side, the frequency dependence of capacitance at selected bias range are shown in Fig. 6 and Fig. 7, respectively, under forward and reverse directions. The capacitance at lower biases (first region in both forward/reverse direction) was positive for whole scanned frequency interval but at higher bi-

ases (the second region in forward direction and third region in reverse direction), the capacitance changed from its geometric value at high frequencies to negative values with decreasing in frequency below 1 kHz. Negative capacitance phenomenon has been displayed over different kind junctions like p-n junction, Schottky diodes, p-i-n junction and light emitting diodes (LED) formed through inorganic and organic materials [13, 20, 34] such as In-GaN/GaN multi quantum wells [3], Au/n-GaN and Pt/n-GaN Schottky diodes [11, 35] and a-Si:H based $p^+ - i - n^+$ diodes [16] and finally polymer LED [13, 15, 17, 18, 19, 26]. The mechanisms over the negative capacitance in different devices have been attributed to the contact injection [36] interface state [37] and minority carrier injection [12]. Overall, the negative capacitance issue was the consequence of charge in the current flowing in the structure as a result of changing the applied bias voltage, leading to a frequency-dependent electrical response. In literature, this ac response was well explained in space charge limited region in forward bias direction (so called SCLC model) for a low mobility disorder material [13, 15, 18] and admittance relation was derived as

$$Y(\Omega) = \frac{\epsilon A}{\tau_t L} \times \frac{\Omega^3}{2i(\tilde{\mu}(\Omega))^2[1 - e^{-i\Omega/\tilde{\mu}(\Omega)}] + 2\tilde{\mu}(\Omega)\Omega - i\Omega^2} \quad (4)$$

where $\Omega (= \omega\tau_t)$ is normalized frequency, $\tilde{\mu}(\Omega) (= \mu(\Omega)/\mu_{dc})$ is normalized mobility over the dc mobility (μ_{dc}), τ_t is the transit time. In the sense of Scher and Montroll (SM) theory, dispersive transport of carriers appears in the mobility expression as

$$\tilde{\mu}(\Omega) = \frac{\mu(\Omega)}{\mu_{dc}} = 1 + M(i\Omega)^{1-\alpha} \quad (5)$$

where M is proportionality constant and α

denoted a dispersion parameter and charges in between 0 and 1.

The derived admittance expression is in good agreement with the measured capacitance ($Im[Y(\omega)/\omega]$) and the conductance ($= ReY(\omega)$) data in which frequency-dependent of conductance/capacitance as a function of applied bias voltage are similar to that we presented in Fig. 6 and Fig. 7 of this work. Lately, Ehrenfreud et al. revised the expression by a term

$$\Delta C_r(\omega) = \frac{-XC_g}{1 + \omega^2\tau_r^2} \quad (6)$$

where X is dimensionless parameter and τ_r is the recombination time that denotes a time interval for electron-hole recombinations. In fact, this additive term in capacitance $C(\omega)$ is also proposed in before by Perera et al. [14] to account the transient current $\delta I(t) [= I(t) - I(\infty)]$ as

$$C(\omega) = \frac{1}{\delta V} \int_0^\infty \delta I(t) \cos(\omega t) dt \quad (7)$$

with δV is the small voltage step superimposed over a dc bias. Finally, the equation for the capacitance turn into the expression as

$$C(\omega) = C_0 - \frac{\Delta G_i \tau - \Delta C_i}{1 + (\omega\tau)^2} \quad (8)$$

where C_0 is geometrical capacitance, ΔG_i is the variation in conductance and τ is a time constant of the trap and reflects the relaxation time of current. In the simulation work of Perera et al. [14], frequency dependence of the measured capacitance as a function of bias is well produced and interpreted as this negative capacitance issue is originated from the carrier capture and emission of interface states. Also, it successfully explains the presence of an inductive contribution over the measured capacitance not only under forward bias condition, but also at reverse biases. However, although this approach

satisfactorily explains C - $\log f$ characteristic under forward/reverse condition (given in Fig. 6(b) and Fig. 7), it fails to interpret C - $\log f$ variation presented in 6(c). Besides, this approach predicts symmetric dark current-voltage behavior. Luckily, SCLC model incorporating the transit time dispersion seems adequate to resolve such C - $\log f$ variation in the present structure [13, 15, 35]. Therefore, the measured admittance data were fitted to the relation with and without the additive term and demonstrated as solid lines in Fig. 6(b) as examples at selected forward bias voltages for clarity. Clearly, fitting of the derived admittance expression to the experimentally measured capacitance is well. However, though SCLC model based on single type charge carrier, the relation 6 included not only bipolar charge injection, but also radiative recombination in which light emission was observed as in this work. Indeed, light emission began around 4 V (not shown) under forward bias condition for the present p-i-n structure. Although the expression given in the Eqns. 4-6 seemed adequate to resolve the negative capacitance issue in both forward/reverse direction, we can not exclude minority carrier injection effect that also results similar C - $\log f$ variation. Minority carrier injection and SCLC model might be coexist and played a major role in inductance effect in present junction, but we cannot discriminate which of them is dominant in the observations of negative capacitance issue.

5. Conclusion

The electrical response of MOCVD grown GaN based p-i-n structure was investigated by temperature-dependent current-voltage and admittance measurements. Trap-assisted tunnelling was discerned as the carrier conduc-

tion mechanism; in the forward direction, electron was tunnelling entity, while in the reverse case, heavy hole was the tunnelling entity. Extracted activation energy was used in determination of tunnelling entity and they were in close agreement with the published results in the literature. These tunnelling entities behaved as minority carrier that might originate negative capacitance issue together with the well-known space charge limited current (SCLC) model. Applications of the revised SCLC model that took into account both recombination phenomenon and trap-mediated tunnelling issue, resulted in good agreement of calculated capacitance to the experimentally measured one. We tentatively proposed that both minority carrier injection effect and revised SCLC model played a major role in observations of negative capacitance over the GaN-based p-i-n structure.

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