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# Impact of PCM Resistance-Drift in Neuromorphic Systems and Drift-Mitigation Strategy

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***Abstract*—Neuromorphic architectures that exploit emerging resistive memory devices as synapses are currently receiving a lot of interest. Phase Change Memory (PCM), in particular, is a strong candidate for such architectures. However, it suffers from a resistance-drift effect in the amorphous phase (high-resistance). In this work, we investigate the impact of resistance-drift in 'Learning-' and 'Read-' mode operation of large-scale hybrid neuromorphic architectures that use bio-inspired 'STDP-type' learning rules. We show that our '2- PCM Synapse' approach is inherently tolerant to resistance-drift. We also present a new architecture ('Binary-PCM Synapse') and programming strategy based on partial-reset states of PCM devices, which strongly minimizes the impact of resistance-drift. To benchmark the two programming approaches and architectures, we perform system-level simulations on a complex visual pattern extraction application. A power consumption analysis for the two approaches is finally presented. It highlights the ultra low-power potential of PCM-based neuromorphic computing.**

## I. Introduction

Interest in the field of bio-inspired computational hardware has increased dramatically over the last few years. Several research groups [1], [2], [3], [4] are actively exploring neuromorphic hardware due to its promising advantages such as low-power, high defect/variability- tolerance, and efficient handling of large scale non-linear computations. Among the different implementations of neuromorphic hardware, of particular interest are the ones that exploit hybrid architectures: CMOS + emerging resistive memory (RRAM). In these hybrid architectures, the neuronal functionality is implemented by using standard CMOS circuits while the synaptic functionality is implemented through densely integrated arrays or crossbars of RRAM technologies. These RRAM technologies may include devices such as phase change memory (PCM) [5], [6] conductive-bridge (CBRAM) or programmable-metallization cell (PMC) [4], [7] and oxide based resistive memory (OXRAM) [8], [9], [10]. Owing to their compact size, resistive-memory devices help in achieving a high synaptic density which is not possible with pure CMOS-synapse circuits, as a large number of transistors are required (>10) per synapse [11]. RRAM also provides the much needed non-volatility to the neuromorphic system.

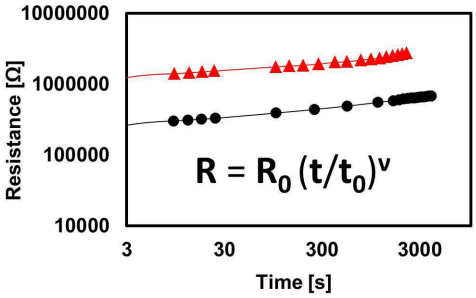


Fig. 1. Resistance drift with time for different initial programming conditions. Measurement was carried out on GST PCM devices. Equation governing the drift dynamics is also shown.

Here, we focus on hybrid neuromorphic architectures that use PCM devices as synapses. PCM devices consist of an active chalcogenide layer sandwiched between two metal electrodes. The working principle exploits reversible and non-volatile phase-change phenomena inside chalcogenide layers such as $Ge_2Sb_2Te_5$ (GST). Phase-change is obtained through joule-heating, when electrical bias or pulses are applied. PCM devices can be programmed to a high-resistance (or reset) state by creating a resistive amorphous region inside the chalcogenide layer. Heating the chalcogenide layer above its melting temperature and then quickly quenching it gives rise to formation of amorphous region. A low-resistance (or set) state can be obtained by creating crystalline regions in the chalcogenide layer. Crystallization occurs when the chalcogenide layer is heated at its crystallization temperature for sufficient duration. Intermediate resistance states can also be obtained by carefully tuning the programming conditions (i.e pulse-width and amplitude) [12]. These properties have led to proposed use of PCM devices for mimicking synaptic-plasticity effects such as potentiation (LTP-like) [13], depression (LTD-like) and bio-inspired learning rules like spike-timing dependent plasticity (STDP). In previous works [6], we presented a novel low-power PCM based neuromorphic architecture called the '2-PCM Synapse'. Using our architecture we demonstrated a two-layer spiking neural network (SNN) capable of complex visual pattern extraction.

However, in PCM devices, the amorphous or high-resistance states are not entirely stable. Melt-quenched amorphous regions created inside the chalcogenide layer undergo structural relaxations and the resistance of PCM device tends to increase with time (known as resistance-drift). The resistance-drift follows an empirical exponential rule which depends upon

the initial programmed resistance and a parameter known as the drift coefficient ($\nu$) [14]. The crystalline or low-resistance states of PCM are shown to be free from resistance-drift [15]. Fig.1 shows the resistance-drift measured in our GST-PCM devices and the equation governing the drift dynamics. The devices were programmed in two different initial (reset) states and the resistance was read at different time intervals. Inside a neural network such resistance-drift may cause undesired change of trained synaptic weights.

In this paper, we discuss how our '2-PCM Synapse' architecture is inherently tolerant to PCM resistance-drift. We also introduce a new 'Binary-PCM Synapse' architecture with a stochastic STDP learning rule. We show that by carefully defining the reset state (partial-reset) in the 'Binary-PCM Synapse' architecture the effects of drift can be mitigated even further. Section II describes the two different PCM based architectures and programming schemes. Section III, discusses the visual pattern extraction simulations, the impact of drift, and overall system performance.

## II. PCM BASED SYNAPTIC ARCHITECTURES

### A. The '2-PCM Synapse'

Our main motivation for developing the '2-PCM Synapse' architecture was to emulate synaptic behavior (i.e. gradual synaptic-potentiation and -depression) using identical neuron spikes (Fig.2) [6]. In this approach, we use two PCM devices to implement a single synapse and connect them in a complementary configuration to the post-synaptic output neuron. One of the PCM device implements synaptic potentiation (LTP-device), while the other implements synaptic depression (LTD-device). Both devices are initialized to a high resistive amorphous state. When synaptic potentiation is required, the LTP device is crystallized, while when synaptic depression is required, the LTD device is crystallized. Fig.3 shows the characteristic resistance evolution of our GST-PCM devices with gradual crystallization events. The detailed programming schemes and the simplified STDP learning rule used are described in [6]. Note that as the neural network undergoes learning, with time the PCM devices become more and more crystallized and finally saturate to a minimum resistance value. In order to enable continuous learning of the network, we defined a refresh-sequence, explained in detail in [16]. In this

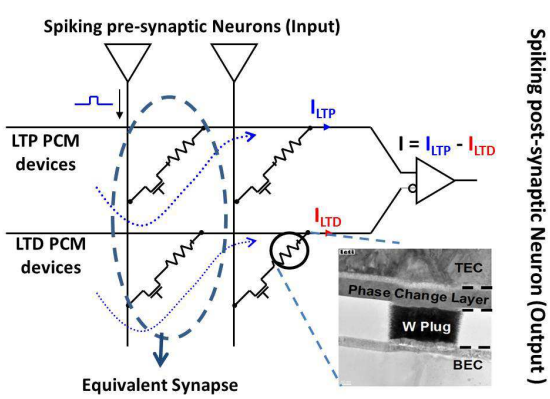


Fig. 2. Schematic of the '2-PCM Synapse' architecture. Inset shows a TEM image of GST PCM device.

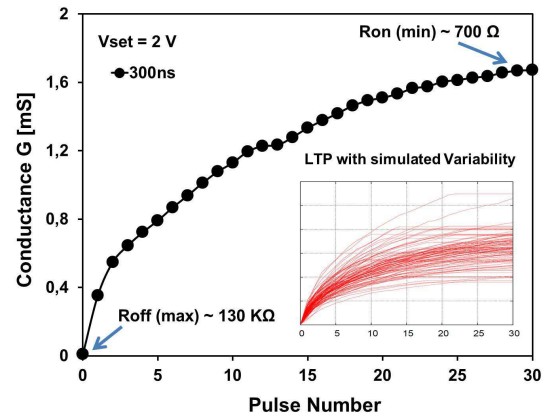


Fig. 3. Experimental LTP curve for pulse width of 300ns. Inset shows 100 different simulated LTP curves with a 20% standard deviation variability included on all synaptic parameters described in equation 3 of [6].

refresh-sequence, the saturated PCM devices are amorphized (reset) and the effective weights of the corresponding synapses are re-programmed.

### B. 'Binary-PCM Synapse' and Partial-Reset

Alternatively, we propose for the first time, to use PCM devices as binary synapses but with a stochastic-STDP rule, similar to the one we developed for bipolar CBRAM devices [4]. In this approach, there will be 1-PCM device per synapse. Two resistance states (or weights) can be defined for the PCM synapse. The high-resistance state should be chosen such that it is a partial-reset (Fig. 4) state. The partial-reset state should lie in the negligible or low-driftable region. For GST based devices a resistance value $< 50$ k$\Omega$ will lie in low or negligible drift regime [15], [14]. Fig. 5 shows an example of our stochastic-STDP rule. The y-axis represents a probability to switch from the set-to-reset or reset-to-set states for the PCM synapses. Fig. 6 shows the architecture and the programming scheme required to implement the stochastic learning with binary PCM synapses.

The stochasticity is controlled by an extrinsic PRNG (pseudo-random number generator) circuit. The PRNG circuit controls the probability of LTP and LTD with a 2-bit signal. Initially, the input neurons (A-D) generate small read pulses when they encounter any stimuli event. The read current is integrated in the output neurons A' and B'. When the output neuron reaches its firing threshold it generates a feedback signal(3) and a post-spike signal. In the example shown in Fig. 6 output neuron A' fires and B' doesn't fire. The signal(3) activates the gates of all the select transistors on the synaptic line connected to A'. If LTP is to be implemented the Input neuron will send a signal(1), as shown for Input neuron A in this example. In the case of LTD the input neuron will send a signal(2), as shown for the input neuron D. The probabilities of LTP/LTD can be tuned according to the learning rule (Fig. 5).

## III. RESULTS AND DISCUSSION

In this section, we benchmark impact of drift on the two different architectures discussed in the previous section, by

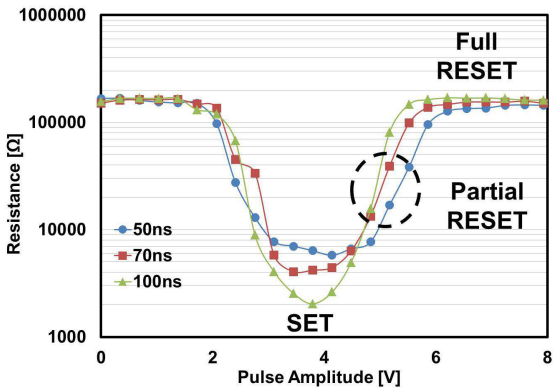


Fig. 4. Experimental Resistance-Voltage curves for different programming pulse widths on GST PCM devices.

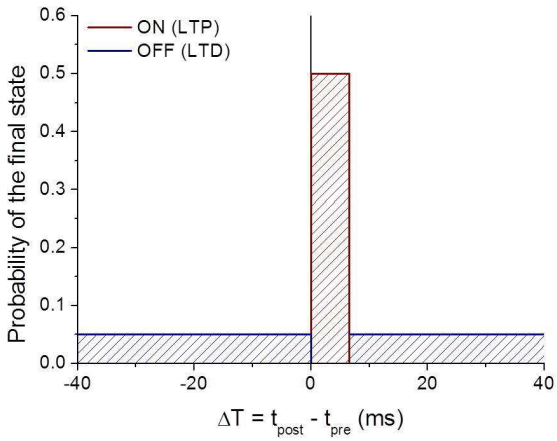


Fig. 5. Simplified stochastic STDP learning rule. 'On' corresponds to set and 'Off' to reset of the PCM synapse.

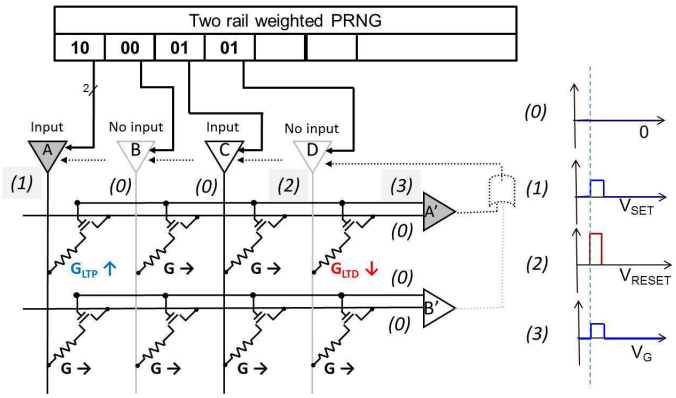


Fig. 6. Schematic of the 'Binary-PCM Synapse' architecture and the proposed programming-scheme.

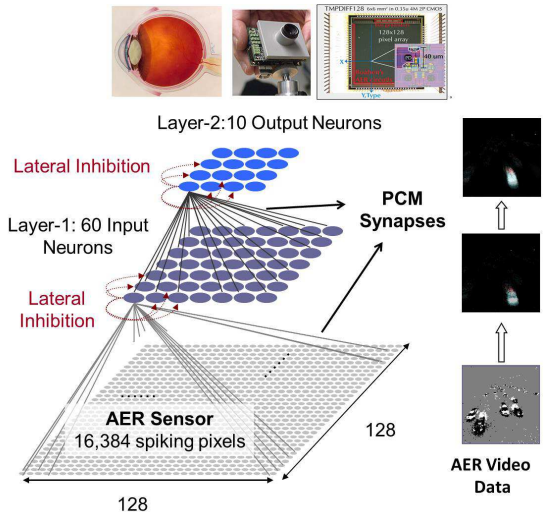


Fig. 7. (Top) Model of the retina and DVS sensor [18] used for generating AER data. (Bottom) Schematic of the two-layer SNN used for complex visual pattern extraction.

simulating a large-scale real world pattern extraction application. We used our custom built XNET SNN simulator [17] to simulate a complex visual pattern application. Our 2-layer SNN with 70 neurons and about 2 million PCM synapses is shown in Fig. 7. AER video of cars passing on a freeway was recorded using a special DVS-Sensor [18] and used as the input data for our SNN. During the learning, the neurons were able to extract patterns (car-shapes) in different lanes (different positions and orientations) in a fully unsupervised manner. The detailed learning mechanism of the network is described in [19]. Table. I and Table. II summarize the SNN performance and detection rates for all the simulations performed for this paper.

### A. Drift Impact

In order to study the impact of PCM resistance-drift in our network we first classify its operation in two different modes: (a) Learning-mode and (b) Read-mode. In learning mode the synaptic programming is enabled and the network is trained using various datasets or stimuli. It is only during this mode that the synaptic weights can be changed. For the '2-PCM Synapse' architecture, in the learning-mode, the PCM are typically not experiencing drift. Only, whenever a refresh-sequence is applied to a synapse, it pushes the respective PCM devices into the driftable region. In the refresh-sequence, both devices are reset and one of them is reprogrammed to a lower resistance state. For the device which stays in the fully reset state, drift is irrelevant: the more reset it is, the better. The other device, which is reprogrammed to a high resistance but intermediate state, may experience drift until it encounters sufficient crystallizing events (LTP or LTD) that push it in the non-driftable region. Such drift can delay learning, and its occurrence can be attributed to the refresh-frequency. More precisely, the drift in learning will be a consequence of the on-going competition between the refresh-frequency and the set-frequency.

Set-frequency depends on (1) nature of the learning rule and (2) nature of the stimuli used for training, while the

refresh-frequency mainly depends on the type of chalcogenide material used. A chalcogenide material which crystallizes slowly and offers more intermediate resistance states before saturation will require less frequent refresh. In previous works we showed that growth dominated materials like GeTe have almost double the refresh-frequency compared to nucleation dominated material such as GST [20]. While interface engineering (GST+$HfO_2$) can further improve the number of intermediate resistance states thus decreasing the refresh frequency [21]. From Table. I, we can see that for the '2-PCM Synapse', the ratio of set-frequency (/device/s) to reset-frequency (/device/s) is about 25. In the case of interface engineered devices [21] this ratio further increases to a value of 55.

Drift is more dramatic in the case of the read-mode compared to learning mode, since the system has no means to compensate for it through learning. In the read-mode, synaptic programming is disabled and a pre-trained neural network is used to identify patterns in new datasets or stimuli without changing the synaptic weights. Thus impact of resistance-drift in the read-mode is proportional to the final weight distribution of the synapses at the end of the training, and the time interval after which the network is operated in read-mode post training.

Synaptic weight distribution at the end of learning mode gives the number of synapses that are left in the high-resistance or driftable state. An inherent advantage of the '2-PCM Synapse' approach, compared to the methodology used in [22], is that we implement both potentiation and depression by crystallization. Thus the majority of PCM devices at the end of the learning are programmed in low resistance or non-driftable states. This is irrespective of the fact that we use a pre-dominantly depression (LTD) based learning rule. As crystalline or low resistance states are more stable and immune to the resistance drift [14], [15], [23] the '2-PCM Synapse' diminishes the loss of synaptic information in the read-mode. Fig. 8, shows the final synaptic resistance (weights) distribution at the end of the cars learning simulation. About 60% of the devices are in the non-driftable region. The strong reduction in percentage of devices in driftable region is more evident from Table. I. We can see that the number of set events is about ten times greater than number of reset events for the '2-PCM Synapse' as LTD is also implemented by set or crystallization.

In the case of 'Binary-PCM Synapse' architecture the impact of drift in learning-mode can be fully mitigated if the reset state of the PCM devices is tuned carefully to a partial-reset state (negligible drift region). Fig. 9 shows the final synaptic resistance distribution at the end of learning when the simulation was performed for the 'Binary-PCM Synapse' architecture with stochastic learning. In this simulation the mean reset state was defined as 20 kΩ, which lies in the non-driftable region. At the end of the learning, about 97% of the synapses are in the reset state. This is due to the strongly LTD dominant nature of our learning rule (Fig. 5). Even though majority of the synapses are in reset state, they will not drift as they lie in the non-driftable region.

We performed the cars-learning simulations for the 'Binary-PCM Synapse' architecture with 3 different PCM reset resistance states, keeping the set state constant: (1) negligible drift region (mean Roff = 20 kΩ), (2) Low drift region (mean Roff = 30 kΩ), and (3) high drift region (mean Roff $>$ 100 kΩ). The final synaptic resistance distributions for the reset devices and the set devices in the 3 cases are shown in Fig. 10 and Fig. 11 respectively.

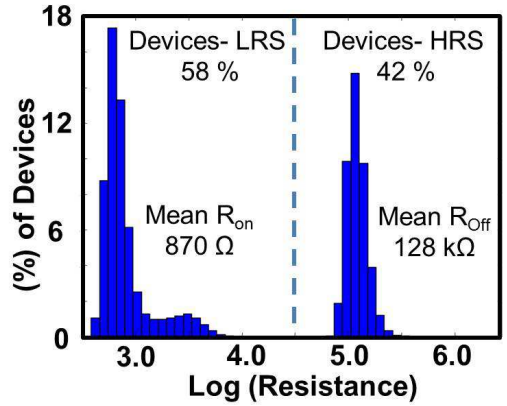


Fig. 8. Distribution of synaptic resistance states for the '2-PCM Synapse' architecture at the end of the visual learning simulation.

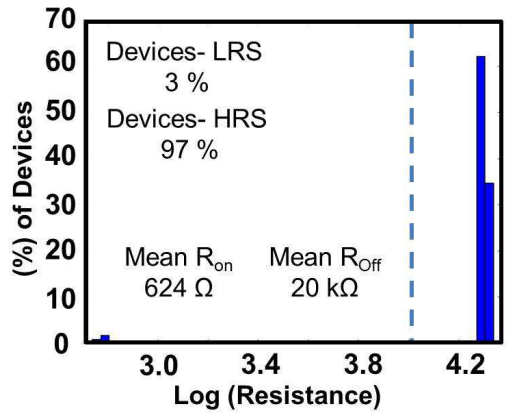


Fig. 9. Distribution of synaptic resistance states for the 'Binary-PCM Synapse' architecture with 20 kOhm mean Roff.

### B. Overall System Performance

Fig. 12 shows the final neuron sensitivity maps for the 6-lanes at the end of cars-learning simulation for the case of '2-PCM Synapse' and 'Binary-PCM Synapse' (20 kΩ) architectures. Table. 2 gives the exact value of detection rate for each individual lane. Lanes 1 and 6 were classified as not-learnt as their detection rates were $<$ 85%. The average detection rate was 91% for the '2-PCM Synapse' and 95% for the 'Binary-PCM Synapse'. Obtaining a high detection rate with an unsupervised system is a strong accomplishment from a machine learning point of view. It is also interesting that the binary synapses performed better. Binary synapses appear especially fit to process this kind of highly dynamic video data.

From Table. 1 we can see that, as we move from the '2-PCM Synapse' architecture to the 'Binary-PCM Synapse', the number of read-events becomes half as the number of PCM devices is also halved. However the read frequency/device/s stays constant. The read-frequency stays constant as it depends

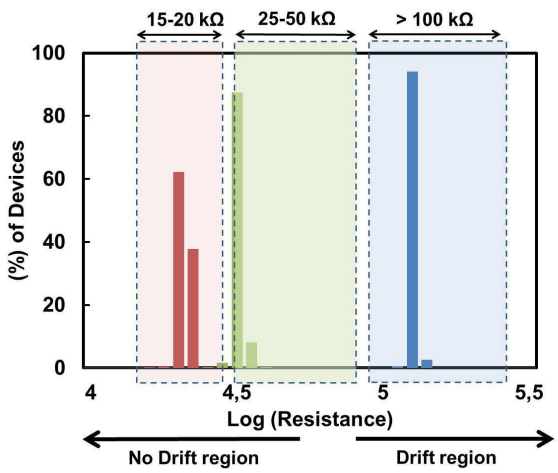


Fig. 10. Distribution of synapses in off-state for the 'Binary-PCM Synapse' with mean Roff values of 20 kOhm, 30 kOhm and 123 kOhm.

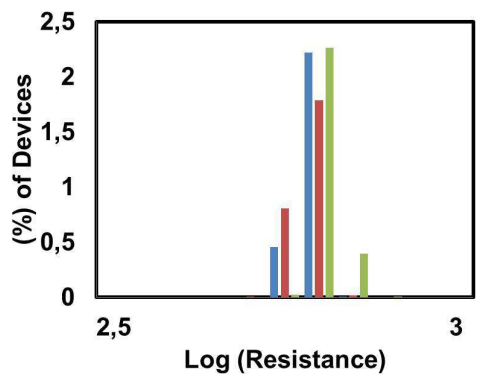


Fig. 11. Distribution of synapses in on-state for the three cases shown in Fig.10.

on the nature of stimuli used to train the network. In the case of 'Binary-PCM Synapse' the set and reset events are a direct representative of the number of LTP and LTD events. However in the case of '2-PCM Synapse' the reset events represent the number of refresh-sequences while the set events denote both LTP and LTD.

To estimate the energy consumption by the PCM devices during the learning process, we use the following equations (CMOS or neuron power consumption is not included):

$$E_{set/reset} = V_{set/reset} \times I_{set/reset} \times t_{pulse}$$

$$E_{total} = (E_{set} \times \text{total set events}) + (E_{reset} \times \text{total reset events})$$

$$Power_{synaptic\ learning} = E_{total}/Duration_{learning}$$

The total duration of learning for all the simulations is fixed (680 s). The energy consumption decreases in the case of 'Binary-PCM Synapse' as the current required to program partial-reset states (20 kΩ and 30 kΩ) is much less compared to the current required to program a strong reset state (128 kΩ). However the energy consumption doesn't decrease drastically as the number of reset-events increases in the 'Binary-PCM Synapse' architecture.

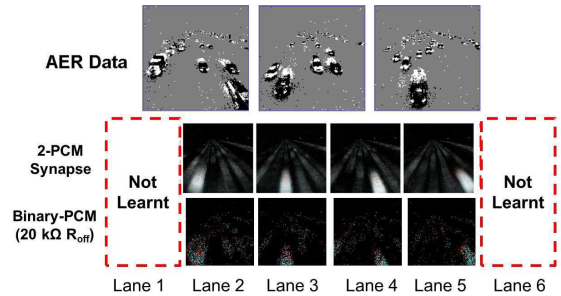


Fig. 12. Final neuron sensitivity maps for the '2-PCM Synapse' and the 'Binary-PCM Synapse' (20 kOhm partial-reset state) architectures.

TABLE I. COMPARISON OF LEARNING STATISTICS AND PERFORMANCE FOR THE DIFFERENT ARCHITECTURES.

| Quantity | *'2-PCM Synapse'* | *Binary-PCM Synapse* | |
|---|---|---|---|
| | Roff = 128 kΩ | Roff = 20 KΩ | Roff = 30 KΩ |
| Total Read | $4.97 \times 10^9$ | $2.48 \times 10^9$ | $2.48 \times 10^9$ |
| Total Set | $3.86 \times 10^8$ | $5.13 \times 10^5$ | $4.84 \times 10^5$ |
| Total Reset | $1.56 \times 10^7$ | $1.90 \times 10^7$ | $1.78 \times 10^7$ |
| Frequencies of events ( event / device / sec) | | | |
| *F* read/d/s | 1.9 | 1.9 | 1.9 |
| *F* set/d/s | 0.14 | 0.00038 | 0.00036 |
| *F* reset/d/s | 0.0058 | 0.014 | 0.013 |
| Energy/ Power Consumption | | | |
| Set Energy | 33.6 mJ | 0.1 mJ | 1.6 mJ |
| Reset Energy | 37 mJ | 36.2 mJ | 42.6 mJ |
| Total Energy | 71.4 mJ | 36.3 mJ | 44.2 mJ |
| Total Power | 105 μW | 53.8 μW | 65 μW |
| Read Energy* | 402 μJ | 51 μJ | 48 μJ |
| Read Power* | 600 nW | 75 nW | 70 nW |

In both cases (Roff:20 kΩ, 30 kΩ ), the power consumption by the PCM devices during learning remains low (<80 $\mu$W). Additionally, use of aggressively scaled PCM devices may futher decrease the power to a few nanowatts [6]. During read, the devices are not programmed anymore and their power consumption is much smaller (about 75 nW). The total read energy and power dissipation for all the cases is provided in Table.1. Read-energy is estimated using the following equation:

$$E_{read} = \Sigma \frac{(V_{read})^2 \cdot T_{read}}{R_i}$$

where, $R_i$ is the instantaneous resistance value of a specific PCM device that received the 'ith' read-pulse. The $R_i$ values are recorded in real time using the XNET simulator.

## IV. CONCLUSION

In this paper, we show how our '2-PCM Synapse' architecture is inherently tolerant to the impact of PCM resistance-drift. We show that the synaptic weight distribution post-learning are concentrated more in the non-driftable region, as in our approach even LTD is obtained by crystallization. We introduce, for the first time, a new architecture 'Binary-PCM Synapse' with stochastic STDP learning rule and partial-

TABLE II. AVERAGE CAR DETECTION RATE FOR DIFFERENT LANES.

| Lane | '2-PCM' Synapse | 'Binary-PCM' Synapse | |
|---|---|---|---|
| Roff | 128 kΩ | 20 kΩ | 30 kΩ |
| 1 | 72 | 79 | 78 |
| 2 | 95 | 97 | 98 |
| 3 | 94 | 93 | 92 |
| 4 | 90 | 94 | 93 |
| 5 | 85 | 99 | 96 |
| 6 | 80 | 84 | 82 |
| Avg* | 91 | 96 | 95 |

reset states. The programming methodology is also presented. We show that by carefully tuning the partial-reset state the impact of drift can be mitigated even further as almost all the synapses post-learning lie in the non-driftable regime. System-level simulations show that both approaches can perform complex problems of machine learning with ultra low power consumption. This highlights the potential of PCM technology for future intelligent ubiquitous embedded systems.

## ACKNOWLEDGMENT

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