High capacitance density of 185 nF/mm2 achieved in three-dimensional MIM structures using TiO2 as a dielectric

A. Chaker, P. Gonon, Corentin Vallée, A. Bsiesy

High capacitance density of 185 nF/mm^2 achieved in three-dimensional MIM structures using TiO_2 as a dielectric

A. Chaker, P. Gonon, C. Vallée, and A. Bsiesy[a)]
University Grenoble Alpes, CNRS, LTM, F-38000 Grenoble, France

(Received 5 April 2017; accepted 2 June 2017; published online 12 June 2017)

In this paper, three-dimensional (3D) metal-insulator-metal (MIM) structures were obtained by atomic layer deposition of an aluminum doped TiO_2 layer on a dense array of truncated conical holes etched in a silicon substrate. Different features of conical holes were fabricated in order to increase the developed area of the MIM structure. A capacitance density of nearly 185 nF/mm^2 was obtained on an array of 19.2 μm deep holes with 5 and 10 μm bottom and top conical hole diameters, respectively. Interestingly, the increase in capacitance density scales with the developed area and no degradation of the electrical properties of the MIM structure has been observed. Indeed, the leakage current across the 3D MIM structures remains as small as in planar (2D) MIM structures. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4986196]

Metal-Insulator-Metal (MIM) capacitors are passive components used in DRAM devices. In order to increase the capacitance density required in advanced DRAM applications while keeping device footprint constant, silicon oxide (SiO_2) was replaced by alternative insulators (medium- κ or high- κ).[1] For example, medium- κ dielectrics like Si_3N_4, Al_2O_3, HfO_2, and ZrO_2 were used in DRAM devices where capacitance densities between 1nF/mm^2 and 22nF/mm^2 have been achieved.[2–7] However, future DRAM applications require capacitance densities larger than 100nF/mm^2 that can be achieved only through the use of high- κ dielectrics. Titanium dioxide (TiO_2) is a very promising candidate thanks to its high permittivity constant that can reach 170 in its rutile crystalline structure.[8] In general, rutile TiO_2 can be obtained only at high temperature (800 °C). Fortunately, rutile TiO_2 can be grown at low temperature (250 °C) if it is deposited on a ruthenium oxide (RuO_2) layer thanks to the small lattice mismatch between TiO_2 and rutile RuO_2.[9,10] The major drawback of rutile TiO_2 is its small bandgap (3.1 eV) that leads to an increase of leakage current of the MIM structure. To reduce this current, the TiO_2 layer can be doped by aluminum atoms that compensate the oxygen vacancies in the TiO_2 layer and thus suppress conduction paths.[11]

Capacitance densities around 40 nF/mm^2 are recorded with an aluminum doped TiO_2 layer (ATO) of 12 nm in planar MIM structures. This is below the targeted 100 nF/mm^2 density. The three-dimensional MIM capacitor allows us to increase the capacitance density without increasing the device footprint. Indeed, several reports have been published on 3D MIM structures. For example, a capacitance density of 17nF/μm^2 was obtained using Ta_2O_5 deposited in 3D damascene MIM architecture (0.65 μm depth); this value was increased to 30nF/mm^2 when the depth is increased from 0.65 μm to 3 μm.[12,13] Another interesting example is the complex triple MIM capacitor based on TiN/Al_2O_3 deposited by atomic layer deposition (ALD), which achieves a capacitance density of 440 nF/mm^2.[14]

In this work, we report a study that demonstrates the possibility to use Al-doped rutile TiO_2 as a high- κ dielectric with the deposition of the ruthenium bottom electrode by physical vapor deposition (PVD) and the platinum top electrode by e-beam evaporation, to build 3D MIM capacitors with a capacitance density of around 185 nF/mm^2.

The 3D MIM test devices were built on arrays of truncated conical holes formed by reactive ion etching (RIE) of patterned silicon wafers. The circular holes were defined by lithography on a 5.7 μm AZ 4562 photoresist exposed to UV line in a mask aligner. The holes were etched by a two-step plasma process. The first step used a sulfur hexafluoride (SF_6) and oxygen (O_2) gas mixture, which led to the formation of holes with inclined sidewalls and an undercut beneath the photoresist mask layer. The photoresist mask was then removed by sample exposure to a radical rich O_2 plasma reactor and then to a dip in piranha solution (H_2SO_4/H_2O_2). In the second step, the undercut on top of the sidewalls was removed by isotropic RIE using SF_6 gas. An inductive coupled plasma (ICP) reactor from surface technology systems (STS) was used for RIE processes. This tool has one RF coil (13.56 MHz) to generate the plasma and two RF platens (13.56 MHz and 380 kHz) to control ions' energy.

In order to increase the capacitance density, different patterns were designed with circular hole arrays of diameters 3, 5, 8, and 10 μm with four different hole initial spacings of 3, 5, 10, and 20 μm. For MIM stack deposition, we proceeded as the following. First, a 70 nm ruthenium layer was deposited by physical vapor deposition (PVD) on top of which 3 nm of RuO_2 was obtained by oxidizing the Ru layer surface under the O_2 plasma at 400 °C. Second, 12 nm of ATO layer was deposited by plasma enhanced atomic layer deposition (PEALD) using one cycle of trimethylaluminum (TMA) and O_2 plasma precursors every 60 cycles of TiO_2.[15] Third, a 100 nm platinum layer was deposited by e-beam evaporation using a shadow mask to achieve patterned electrodes. More details on the preparation of MIM structures can be found in Ref. 15. The isolation between the MIM structure and the silicon substrate was achieved by depositing a 400 nm silicon oxide (SiO_2) layer by plasma enhanced

[a)]Author to whom correspondence should be addressed: Ahmad.bsiesy@univ-grenoble-alpes.fr

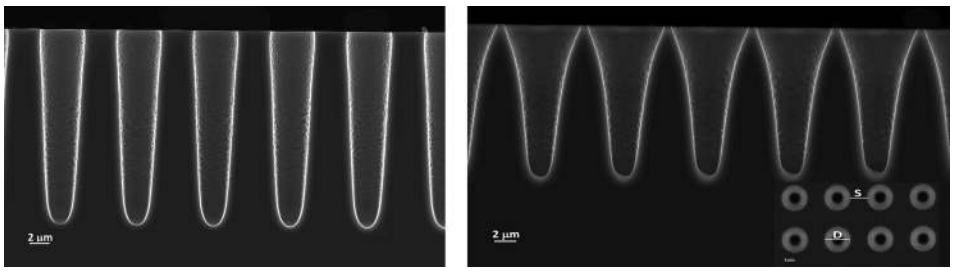

FIG. 1. SEM cross-sectional images for the 3-3 conical hole array (a) after first RIE etch and (b) after second RIE etch; inset: top view where conical holes are shown with D diameter and S spacing.

chemical vapor deposition (PECVD). However, previous work performed on TiO_2 deposited by ALD in the same conditions showed the rutile phase for doped and undoped TiO_2 layers with a dielectric constant equal to 55 for the doped layer.[16,17]

A Scanning Electron Microscope (SEM) from ZEISS ULTRA plus was used to analyze the cross-sectional profile of the hole array. Capacitance measurements were carried out at low frequencies (1 Hz–1000 Hz) using an impedance analyzer from Novocontrol Company.

Figure 1 shows an example of typical conical hole array used in this study to elaborate the 3D MIM structures. The initial lithography patterns form a 2D circle array of 3 μm diameter with 5 μm spacing. The cross-sectional SEM image of Fig. 1(a) shows the hole array of 20 μm after the first etch step where inclined walls as well as small undercuts can be seen. Figure 1(b) shows the hole array after the second etch step where steeper walls were achieved and the undercut at the hole openings has disappeared. The resulting features can be seen as truncated 17 μm deep conical holes with diameters of 7 μm at their opening and 3 μm at their tip, respectively.

It is worth noting that this kind of hole feature with inclined walls is similar to those currently used in 3-D interconnections for conformal deposition of the copper diffusion barrier and copper seed metal.[18–21]

The plasma process parameters had to be optimized in order to achieve the desired hole features and in particular to control the wall tilt angle. Table I shows the values of the main plasma parameters used in this study. Briefly, in the SF_6/O_2 gas mixture (first etch step), SF_6 produces F* radicals responsible for the silicon etching and SF_5^+ ions that are responsible for the etching of the $Si_xO_yF_z$ passivation film grown by oxygen radicals originating from the O_2 plasma.[22] Consequently, the SF_6/O_2 flow ratio is the most important parameter that controls tilted wall features. Indeed, when the SF_6 flow increases, the etching is more isotropic due to the larger flow of F* radicals and SF_5^+ ions. Higher O_2 flow leads to an increase in the $Si_xO_yF_z$ passivation layer and then to a reduction in the etch rate. Finally, an increase in the platen power yields more energetic ions that lead to larger undercut.

TABLE I. Plasma etch parameters used to achieve inclined wall holes in silicon substrate.

Parameters	First etch	Second etch
O_2 Flow (sccm)	75	20
SF_6 Flow (sccm)	85	200
Pressure (mTorr)	35	10
Coil power (W)	2000	2000
Platen power (W)	24	10
Temperature (°C)	10	10

Considering one 3D MIM device means that a large number of MIM stack filled holes are involved since the deposited Pt top electrode covers a given number of holes (Fig. 2). Consequently, a given 3D MIM capacitor has two different surface areas; the area of the device top electrode pattern corresponds to the projected area (1×10^6 μm^2 for all diameter-spacing conical holes), whereas the sum of the hole area corresponds to the developed area. A few features of conical holes have been selected to calculate the projected area, and the result is presented in Table II. These calculations have been performed by assuming that the truncated conical holes are cylinders with diameters equal to half-depth conical hole diameters extracted from SEM images.

Figure 3 displays capacitance density as a function of measurement frequency for planar MIM and 3D MIM (5–5), (8–10), and (10–20) conical holes. As expected, the capacitance density increases when the hole array becomes denser. Moreover, between 1 Hz and 1 kHz, a small decrease in capacitance density is observed, more pronounced for denser holes as presented in Fig. 4. This decrease is probably due to series resistances at the origin of a cut-off frequency. When capacitance increases, this cut-off frequency decreases and hence an increase in the C-f curve slope.

Figure 4 shows that the capacitance density increases as a function of the calculated developed area for different 3D MIM arrays. More precisely, the capacitance density is around 40 nF/mm^2 in the 2D MIM case and increases to 185 nF/mm^2 for denser 3D (5–5) arrays and then to 205 for 3D (3–3) at 1 Hz. It should be noted that this increase is linear for low to medium developed area but shows a slower increase for the high developed area [dense arrays (3–3) and (5–3)]. This deviation from the linear yield can be seen more

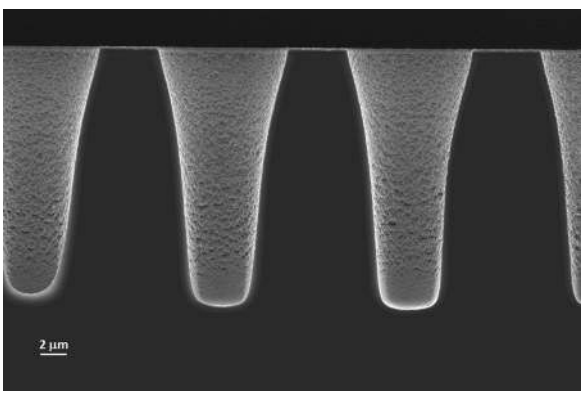

FIG. 2. SEM cross view of the hole array after MIM ($Ru/RuO_2/ATO/Pt$) stack has been deposited.

TABLE II. Calculation of the developed area of each diameter-spacing conical hole arrays.

Diameter (μm)-spacing (μm)	Developed area (μm^2)	Diameter (μm)-spacing (μm)	Developed area (μm^2)
3-3	7×10^6	5-5	4.4×10^6
3-5	4×10^6	5-20	1.5×10^6
3-10	2.2×10^6	8-10	2.9×10^6
3-20	1.4×10^6	10-20	1.9×10^6
5-3	6.7×10^6		

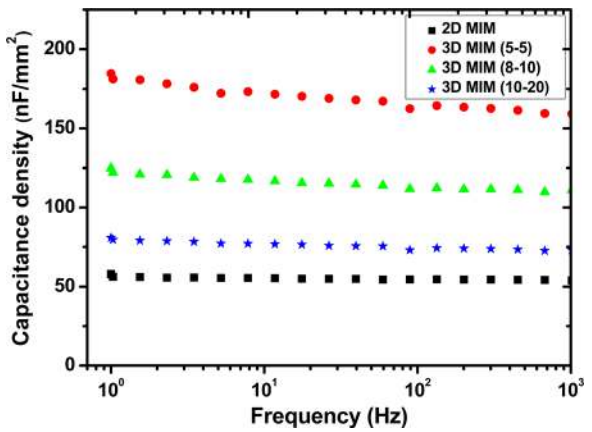

FIG. 3. Capacitance density normalized by the projected area, in the 1 Hz–1000 Hz range for 2D MIM and 3D MIM stacks.

clearly in Fig. 5, where the percentage of the relative difference between calculated and measured capacitance density is represented as a function of the MIM array density.

No deviation between expected and measured capacitance density was found in the cases of 3–20, 5–20, 10–20, 8–10, and 5–5 arrays. However, an increasing deviation was observed for denser hole arrays [(3–3) and (5–3) arrays]. This can be explained by an over-etching of silicon sidewalls separating the holes. Indeed, during the second step RIE process, isotropic etch of silicon sidewalls leads to an enlargement of hole openings which can end up by total shrinking of the silicon wall between neighboring holes. This could decrease the developed area and lead to smaller capacitance

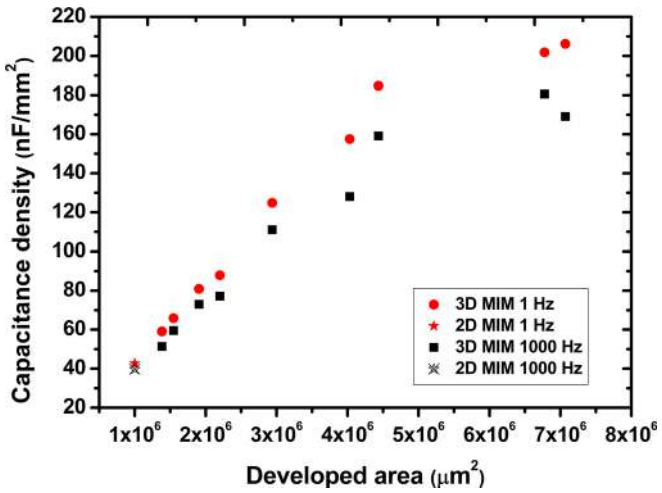

FIG. 4. Capacitance density versus MIM developed area for 3D MIM structures measured at 1 Hz and 1 kHz.

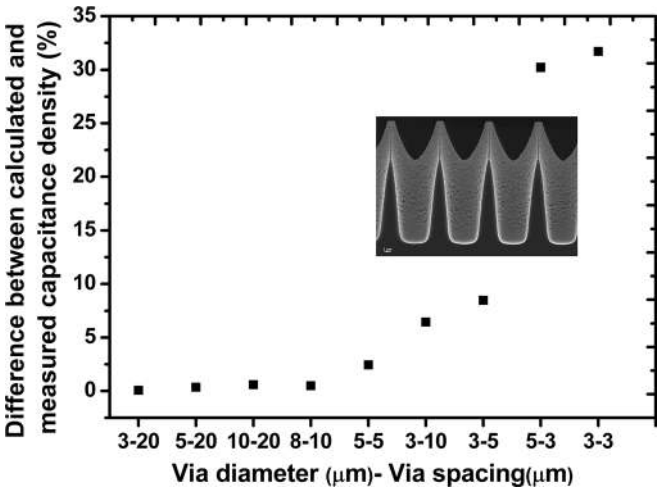

FIG. 5. Relative difference between calculated and measured capacitance density (in %) as a function of the MIM array geometry. Arrays developed surface increases from left to right. The inset shows the silicon sidewall over-etch effect in dense arrays.

density. This effect is shown by the SEM image in the inset of Fig. 5 and is expected to have a larger impact on dense hole arrays.

Figure 6 shows the leakage current density for planar 2D MIM and for different 3D MIM arrays. No significant differences were detected between 2D and 3D structures. This result strongly suggests good conformity of the ATO layer deposited on conical hole array and good uniformity of its thickness in the $Ru/RuO_2/ATO/Pt$ stack.

In summary, in this paper, we have shown the possibility to build 3D MIM structures based on TiO_2 as a dielectric in order to increase the capacitance up to 185 nF/mm^2. Arrays of truncated conical holes etched in the silicon substrate allow to process conformal 3D MIM structures that show good electrical properties, comparable to those obtained with 2D MIM structures in terms of leakage current. The denser 3D (5–5) arrays show high capacitance density and rather low leakage current even though it has to be further reduced. This shows that the process developed in this work leads to conformal and uniform deposition of TiO_2 and pave the way to further increase the capacitance density thanks to denser arrays of higher aspect hole ratios.

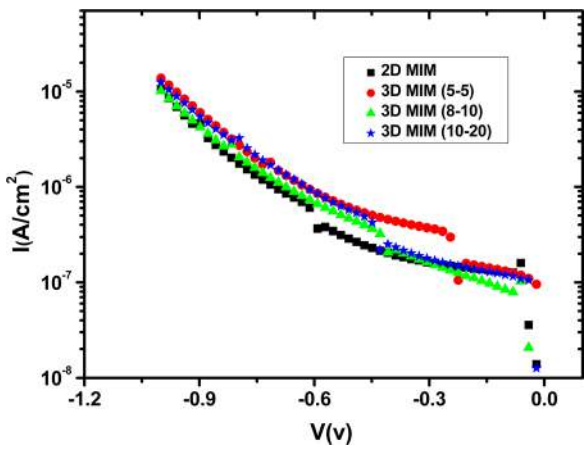

FIG. 6. Leakage current density (considering the developed area) for 2D MIM, 3D MIM (5-5), 3D MIM (8-10), and 3D MIM (10-20).

We acknowledge the financial support of LabEx Minos ANR-10-LABX-55-01 for Ph.D. funding of A.C.

[1]H. Moon, S. Yu, S. S. Song, and I. Nam, Microwave Opt. Technol. Lett. **51**, 1235 (2009).
[2]C. H. Ng, K. W. Chew, and S. F. Chu, IEEE Electron Device Lett. **24**, 506 (2003).
[3]S. B. Chen, C. H. Lai, A. Chin, J. C. Hsieh, and J. Liu, IEEE Electron Device Lett. **23**, 185 (2002).
[4]X. Yu, C. Zhu, H. Hu, A. Chin, M. F. Li, B. J. Cho, D. L. Kwong, P. D. Foo, and M. B. Yu, IEEE Electron Device Lett. **24**, 63 (2003).
[5]S. Y. Lee, H. Kim, P. C. McIntyre, K. C. Saraswat, and J. S. Byun, Appl. Phys. Lett. **82**, 2874 (2003).
[6]S.-J. Ding, H. Hu, H. F. Lim, S. J. Kim, X. F. Yu, C. Zhu, M. F. Li, B. J. Cho, D. S. H. Chan, S. C. Rustagi, M. B. Yu, A. Chin, and D.-L. Kwong, IEEE Electron Device Lett. **24**, 730 (2003).
[7]Y. H. Wu, C. K. Kao, B. Y. Chen, Y. S. Lin, M. Y. Li, and H. C. Wu, Appl. Phys. Lett. **93**, 033511 (2008).
[8]U. Diebold, Surf. Sci. Rep. **48**, 53 (2003).
[9]M. Kadoshima, M. Hiratani, Y. Shimamoto, K. Torii, H. Miki, S. Kimura, and T. Nabatame, Thin Solid Films **424**, 224 (2003).
[10]S. K. Kim, G. W. Hwang, W. D. Kim, and C. S. Hwang, Electrochem. Solid-State Lett. **9**, F5 (2006).
[11]S. K. Kim, G. J. Choi, S. Y. Lee, M. Seo, S. W. Lee, J. H. Han, H. S. Ahn, S. Han, and C. S. Hwang, Adv. Mater. **20**, 1429 (2008).
[12]M. Thomas, A. Farcy, C. Perrot, E. Deloffre, M. Gros-Jean, D. Benoit, C. Richard, P. Caubet, S. Guillaumet, R. Pantel, M. Cordeau, J. Piquet, C. Bermond, B. Flechet, B. Chenevier, and J. Torres, in *VLSI Symposium on Technical Digest* (2007), p. 58.
[13]S. Jeannot, A. Bajolet, J. P. Manceau, S. Cremer, E. Deloffre, J. P. Oddou, C. Perrot, D. Benoit, C. Richard, P. Bouillon, and S. Bruyere, in *Proceedings of the International Electron Devices Meeting* (IEEE, 2007), p. 997.
[14]J. H. Klootwijk, K. B. Jinesh, W. Dekkers, J. F. Verhoeven, F. C. van den Heuvel, H. D. Kim, D. Blin, M. A. Verheijen, R. G. R. Weemaes, M. Kaiser, J. J. M. Ruigrok, and F. Roozeboom, IEEE Electron Device Lett. **29**, 740 (2008).
[15]J. Pointet, P. Gonon, L. Latu-Romain, A. Bsiesy, and C. Vall_ee, J. Vac. Sci. Technol., A **32**, 01A120 (2014).
[16]A. Chaker, P. D. Szkutnik, J. Pointet, P. Gonon, C. Vallée, and A. Bsiesy, J. Appl. Phys. **120**, 085315 (2016).
[17]A. Chaker, C. Bermond, P. Artillan, P. Gonon, C. Vallée, and A. Bsiesy, IEEE Electron Device Lett. **38**(3), 375 (2017).
[18]N. Ranganathan, D. Y. Lee, L. Ebin, N. Balasubramanian, K. Prasad, and K. L. Pey, J. Micromech. Microeng. **18**, 115028–115021 (2008).
[19]R. Nagarajan, E. Liao, D. Lee, C. S. Soh, K. Prasad, and N. Balasubramanian, in *Electronic Components and Technology Conference*, 30 May–2 June 2006 (IEEE, San Diego, CA, USA, 2006), pp. 383–387.
[20]R. Li, Y. Lamy, W. F. A. Besling, F. Roozeboom, and P. M. Sarro, J. Micromech. Microeng. **18**, 125023–125021 (2008).
[21]P. Dixit, S. Vahanen, J. Salonen, and P. Monnoyer, ECS J. Solid State Sci. Technol. **1**, P107 (2012).
[22]R. S. Azlina, A. A. Aziz, and H. A. Hamid, in *IEEE International Conference on Semiconductor Electronics, ICSE '06 29 October–1 December 2006, Shanghai, China (*2006), pp. 851–855.