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# Spin-Transfer Torque Magnetic Memory as a Stochastic Memristive Synapse for Neuromorphic Systems

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**Abstract**—Spin-transfer torque magnetic memory (STT-MRAM) is currently under intense academic and industrial development, since it features nonvolatility, high write and read speed and high endurance. In this work, we show that when used in a non-conventional regime, it can additionally act as a stochastic memristive device, appropriate to implement a “synaptic” function. We introduce basic concepts relating to spin-transfer torque magnetic tunnel junction (STT-MTJ, the STT-MRAM cell) behavior and its possible use to implement learning-capable synapses. Three programming regimes (low, intermediate and high current) are identified and compared. System-level simulations on a task of vehicle counting highlight the potential of the technology for learning systems. Monte Carlo simulations show its robustness to device variations. The simulations also allow comparing the operation of system when the different programming regimes of STT-MTJs are used. With comparison to the high and low current regimes, the intermediate current regime allows minimization of energy consumption, while retaining a high robustness to device variations. These results open the way for unexplored applications of STT-MTJs in robust, low power, cognitive-type systems.

**Index Terms**—modeling, magnetic memories, magnetic devices, simulation.

## I. INTRODUCTION

Thanks to considerable progress in recent years, spin-transfer torque magnetic random access memory (STT-MRAM) – the second generation of magnetic memory – now appears as a breakthrough for embedded and standalone non-volatile memory, providing fast programming and high endurance [1]. However, a limitation of this technology is its stochastic switching nature [1]–[3]. The time required for programming from a memory state to another is a random quantity, which requires designing programming times with high safety margins, to ensure reliable programming. Device physicists have intensely studied this effect of intrinsic probability [4], [5], and circuit designers have proposed ideas like self-enabled programming to mitigate the issue [2]. However, an alternative approach is

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to not consider this randomness as a drawback, but as a feature of the device. In particular, here we reinterpret STT-MRAM cell’s behavior as a “stochastic memristive device”. And we show by system-level simulations how it may be used in a neuromorphic system for practical applications.

In recent years, the exploitation of nanodevices with memory effects (or memristive devices) as synapses in neuromorphic systems has stimulated a growing interest [6]–[21]. They raise the hope for a breakthrough in electronics, bringing smarter, lower power and more adaptive systems. Most of these proposals use memory devices with multi-level capability – the original memristor paradigm [8]. However, an alternative idea is to use binary devices programmed in a stochastic fashion, or even to use binary devices with intrinsic stochastic properties [20], [22]–[24]. In theoretical works, the idea of using stochastic synapses instead of deterministic ones (in a broad sense) has also been proposed with supervised neural networks [25]–[27]. We suggest that STT magnetic memory is ideal for this vision and illustrate it in the case of unsupervised learning.

In the present paper, we introduce the basic physics of STT memory and the foundations of its behavior as a stochastic memristive device. To support the idea, we perform system-level simulations incorporating an accurate model of the stochastic effects for an application of car counting. Monte Carlo simulations show the relevance and the robustness of the approach to device variations, and allow us to identify in which regime STT memory should be used.

Partial and preliminary results of this work have appeared in [28]. The present paper adds in-depth discussion on system implications of using STT memory as a synapse, comprehensive Monte Carlo simulations, and compares the operation of the STT-MTJs in different regimes in terms of energy efficiency and robustness to device variations.

## II. STOCHASTIC MEMRISTIVE BEHAVIOR OF MAGNETIC TUNNEL JUNCTIONS

A magnetic tunnel junction (MTJ, the basic structure of magnetic memory, Figure 1(a)) is composed of a fixed magnetic layer, an oxide layer and a free magnetic layer, whose magnetization can be parallel or antiparallel to the one of the fixed layer. The antiparallel state AP is high resistive and the parallel state P is low resistive. Thanks to the spin transfer torque (STT) effect, a positive current can switch the STT-MTJ from the AP to the P state, while a negative current can

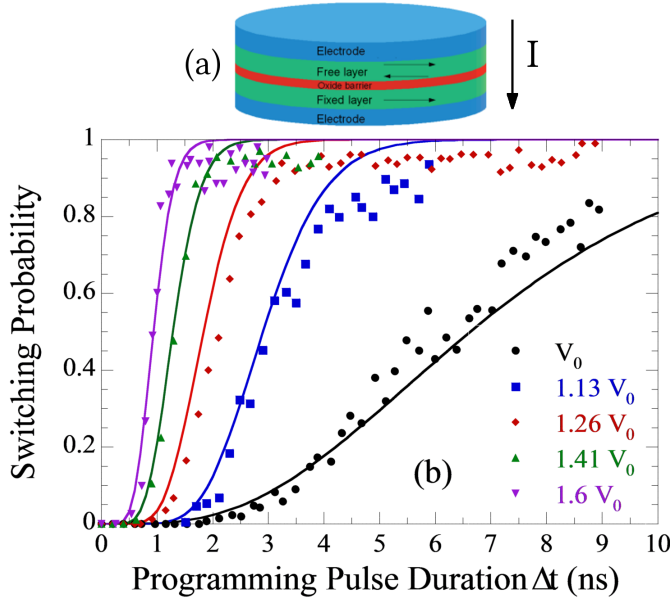


Fig. 1. (a) Schematic illustrating the basic structure of an in-plane magnetic tunnel junction. (b) Symbols: Experimental measurements of probability of switching as a function of programming time, for different programming voltages [5], [29]. Lines: our analytical model.

switch it from the P to the AP state. In this way, a STT-MTJ is extremely reminiscent of a binary bipolar memristor [8].

The switching time depends heavily on the current and is itself a stochastic quantity as observed in the measurements of Figure 1(b). We see that a programming pulse of duration  $\Delta t$  has a *probability* of switching the memory. This stochastic effect is not caused by technological imperfections or filamentary effects like in other resistive memory technologies [22], [24], but is intrinsic to the physics of magnetic switching. This has been largely clarified by magnetism studies.

#### A. Low Current Regime

In particular, at low current, memory switching is caused by thermal fluctuations. We can introduce a critical current of a STT-MTJ (in the case of a device with in-plane magnetization):

$$I_{c_0} = \frac{2|e|\hbar}{\alpha V} \frac{\alpha V(1 \pm P)}{P} \mu_0 M_s \frac{M_{\text{eff}}}{2}, \quad (1)$$

where  $\alpha$ ,  $M_s$  and  $V$  are the Gilbert damping, the saturation magnetization and the volume of the free layer,  $P$  the spin polarization of the current, and  $M_{\text{eff}}$  an effective magnetization (all the equations are written in SI units). The sign  $-$  in equation 1 is for the AP  $\rightarrow$  P transition, the sign  $+$  for P  $\rightarrow$  AP. It should thus be noted that  $I_{c_0}$  has different values for the P  $\rightarrow$  AP and AP  $\rightarrow$  P transitions. However, basic calculations confirmed by measurements show that they correspond to the same voltages. The symmetry  $-$  in voltage  $-$  between the P  $\rightarrow$  AP and AP  $\rightarrow$  P transitions is an extremely nice property of STT-MTJs used as memristive devices.

If a current  $I$  much smaller than  $I_{c_0}$  flows through a STT-MTJ, the mean switching time  $\langle \tau \rangle$  has been proven to behave as the Néel-Brown equation [1]

$$\langle \tau \rangle = f_0^{-1} \exp\left(\frac{E_0}{k_B T} \left(1 - \frac{I}{I_{c_0}}\right)\right), \quad (2)$$

where the energy barrier at zero current is  $E_0 = \mu_0 M_s H_k V/2$ ,  $k_B T$  is the thermal energy,  $H_k$  the amplitude of anisotropy field and  $f_0^{-1}$  a constant. Switching time itself is determined by an exponential random law with mean  $\langle \tau \rangle$  [1], [4]. This implies that if a programming pulse of duration  $\Delta t$  is applied to the junction, its probability of switching is

$$\mathcal{P}_{\text{sw}} = 1 - \exp\left(-\frac{\Delta t}{\langle \tau \rangle}\right). \quad (3)$$

Choosing the pulse duration  $\Delta t$  thus allows tuning the switching probability of the devices anywhere between a low ( $\mathcal{P}_{\text{sw}} \ll 1$  for  $\Delta t \ll \langle \tau \rangle$ ) and a high probability ( $\mathcal{P}_{\text{sw}} \approx 1$  for  $\Delta t \gg \langle \tau \rangle$ ). It should be noted that STT-MTJ thus possess no hard threshold. Even an extremely low current has a probability to switch the junction, but the mean switching time is exponentially dependent on the current.

#### B. High Current and Intermediate Current Regimes

By contrast, when a current much higher than  $I_{c_0}$  flows, the physics differs (precessional switching) and the switching time behaves as Sun's law [1], [5]

$$\tau = \frac{2}{\alpha \gamma \mu_0 M_s} \frac{I_{c_0}}{I - I_{c_0}} \log\left(\frac{\pi}{2|\theta|}\right), \quad (4)$$

where  $\theta$ , the initial angle of the magnetization, is given by a normal random number with mean 0 and standard deviation  $\theta_0 = \sqrt{k_B T / (\mu_0 H_k M_s V)}$  ( $\gamma$  is the electron gyromagnetic constant). This is no longer an exponential law as is seen for the measurements on Figure 1(b), which are taken in the intermediate and high current regimes.

Although the two regimes  $I \ll I_{c_0}$  and  $I \gg I_{c_0}$  have been well studied, the intermediate regime is much harder to model. For the present work we developed equations that fit STT-MTJs' behavior in all situations. The relatively complex equations are beyond the scope of the current paper and are published in a sister publication [30]. Figure 1(b) shows that our equations fit experimental measurements.

Figure 2 shows the mean switching time as a function of current (for the AP  $\rightarrow$  P transition) in all possible regimes, compared with physical simulations based on the macrospin magnetic Landau-Lifschitz-Gilbert-Slonczewski equation with thermal agitation. The low current, high current and intermediate current regimes are visible. This graph also shows how the mean switching time can be tuned over several decades by choosing current or voltage adequately, a unique feature of STT-MTJs.

#### C. Integration and Scaling Potential of STT-MTJs

Although STT-MTJ technology is complex and involves new materials, STT-MTJs are CMOS-compatible, and their integration potential has been demonstrated in several experimental realizations, which use STT-MTJs as standard memory. A standalone memory of 64 Mb, in a 90 nm process, has already reached the market [31], [32], and similar chips have been published in recent years by several groups [33]–[35]. An embedded memory of 1 Mb in a 65 nm process has been published [36].

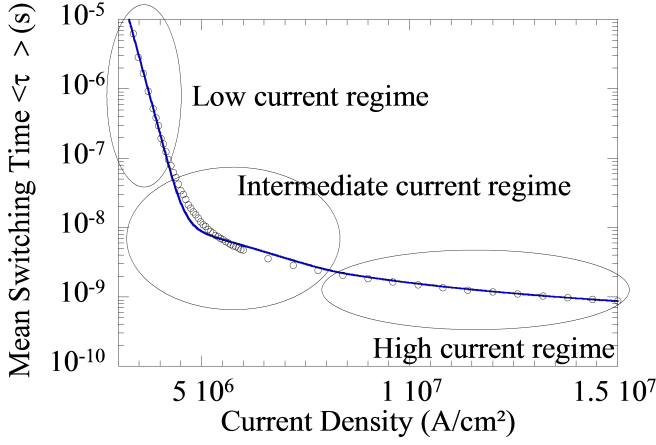


Fig. 2. Mean switching time as a function of current density in a 45 nm technology STT-MTJ, simulated with our model for the AP  $\rightarrow$  P transition. Blue line: our analytical model. Symbols: physical simulation based on Landau-Lifschitz-Gilbert-Slonczewski equation with thermal agitation.

Unlike flash memory, as well as several alternative non-volatile memory technology, STT-MTJs use programming voltages lesser or equal than logic voltages. Programming currents scale with the technology node [1] and can range from mA to 10  $\mu$ A. The most recent realization use structures where the magnetic layers magnetizations are perpendicular to the structure, which reduces programming current [37]–[39]. In Ref. [36], [37], for example, programming voltage is 0.6 V, programming current is 50  $\mu$ A and programming time only 3 ns. Read and write circuits associated with STT-MTJs have been heavily developed in recent years. Advanced read circuits are sense amplifiers specially designed for STT-MTJs [36], [40]. Advanced write circuits mitigate stochastic effects using self-enabled paradigms [2].

### III. EXAMPLE OF APPLICATION IN A NEUROMORPHIC SYSTEM

#### A. Architecture of the System

In this section, we validate by means of system-level simulation the use of stochastic STT-MTJs as synapses. For this, we adapted a scheme proposed elsewhere for Phase Change Memory [13], [41] and Conductive Bridge RAM (CBRAM) [22], [23]. The system implements a spiking neural network, capable of performing unsupervised learning through a simplified Spike Timing Dependent Plasticity (STDP) rule. Figure 3 shows the basic architecture of the system.

CMOS input neurons present the input as asynchronous spikes, which may come directly from a neuromorphic sensor (e.g. DVS retina [42]). The STT-MTJs are organized as a crossbar connecting input and output neurons. The simplest architecture is to use a passive crossbar (1R), which has also been proposed for memory applications [43]. This scheme is extremely efficient in terms of area, and allows each input neuron to be connected to each output neuron by a single STT-MTJ. Unlike for memory operation, this architecture does not suffer from the sneak path during read operations. Indeed, read operation is naturally done in parallel.

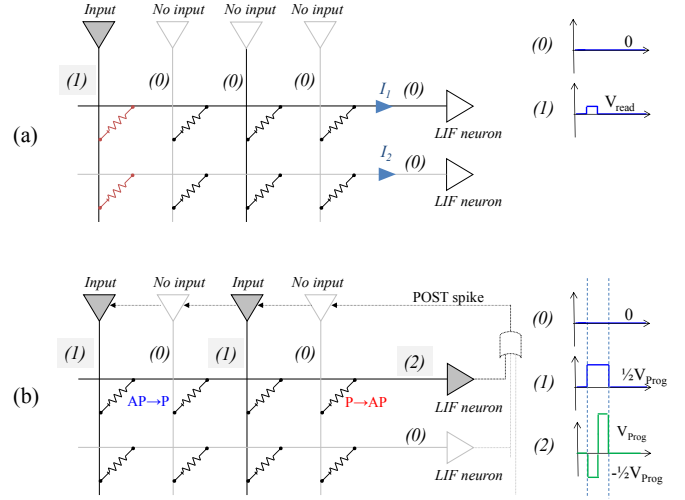


Fig. 3. Schematization of the crossbar architecture (1R case) for the learning system. (a) Read operation, which occurs whenever an input neuron spikes. (b) STDP (write) operation which occurs when an output neuron spikes. Waveforms (1) and (2) are applied concurrently. Due to the stochastic nature of switching, in the presented example, only two STT-MTJs switch states.

In contrast, passive crossbar suffers from some sneak paths during programming, which use unnecessary energy, as discussed later. For this reason, this scheme can be adapted to selector devices (1T-1R structure). This loses, unfortunately, the compactness of the scheme. Detailed comparison between 1R and 1T-1R will be the subject of future work focused on circuit implementations using STT-MTJs as synapses.

In our system, when an input neuron spikes, it applies a brief read pulse to the crossbar, as illustrated in Figure 3(a). This leads to currents that reach the different output neurons simultaneously. The output neurons, materialized as triangles ( $\triangleright$ ) in Figure 3 maintain a constant voltage at their input (avoiding sneak path on other STT-MTJs), while reading the current. This can be achieved using second-generation current conveyor designs [57]. The current received by an output neuron depends on the state (P or AP) of the synapse connecting the input to this particular output. The output neurons provide two features. First, using a sense-amplifier type circuit, adapted from the ones used for MRAM [36], [40], the output neuron can determine if an input was received from a P or AP synapse. This process would lead to error if two inputs spiked during a time smaller than the read pulse width. In the practical application that we studied (processing video data from a DVS retina), this situation does not arise. Second, the output neurons integrate the information received from their sense amplifier. Functionally, the output neurons implement leaky integrate-and-fire (LIF) spiking neurons. They may be implemented by analog or digital circuits [44]–[48]. Only the inputs coming from P synapses are integrated by the output neurons. So, MTJs in the AP state act as synapses with a synaptic weight of zero, and MTJs in the P state act as synapses with a synaptic weight of one.

When an output neuron spikes, it inhibits the other output neurons: their internal variable is reset to zero. In practice, this can be implemented by nearest-neighbor schemes like diffusor

network [49]. With this lateral inhibition, our architecture is reminiscent of a winner-takes-all neural network.

### B. Simplified STDP Rule

Additionally, when an output neuron spikes it applies a voltage pulse on the crossbar, that implements our learning rule inspired by STDP. STDP is a model for synaptic learning in the brain [50], [51]. Many works have proposed to use memory devices to implement STDP [9], [11]–[14], [52]–[57], usually involving sophisticated schemes. Here we use an extremely simplified version adapted to stochastic STT-MTJs.

This simplified STDP rule **deviates from biological models**, and includes two significant simplifications. First, STDP occurs only when an output neuron spikes, which differs from most STDP models, but is easier to implement with nanodevices as seen in [12], [13], [23], [58]. In the field of neuroscience, a similar choice has been taken by Nessler et al. [59]. They showed that in this condition, STDP can approximate the powerful machine learning algorithm of Expectation-Maximization. Second, our STDP rule is stochastic instead of deterministic: a STDP event has a probability to switch a nanodevice.

In practice, STDP steps act as the programming operations of the network and are presented in Figure 3(b). When an output neuron spikes, the whole system enters a “programming” phase. The output neuron that spiked applies the voltage waveform (2) to its row of the crossbar, while the inputs that were active in a recent time window apply an input pulse (1). The combination of these voltage pulses implements a simplified STDP rule: when an output neuron spikes, a STT-MTJ connected to it

- has a given probability of switching to the P state if its input neuron was active in a recent time window;
- has a given probability of switching to the AP state if its input neuron was not active in the same time window.

At the same time, the STT-MTJs connected to the other output neurons are either non-selected, or half-selected (*i.e.* the voltage applied to these devices is either 0 or  $V_{Prog}/2$ ). According to the model of section II, the switching probability of these devices is negligible.

This probabilistic rule is similar to the one that we proposed for CBRAM [22], [23]. However, the voltage waveforms are simpler because of the symmetry in voltage between  $P \rightarrow AP$  and  $AP \rightarrow P$  switching in MTJs. The learning rule is also reminiscent of the simplified STDP proposed for computational neuroscience studies in [59], but in a binary and probabilistic version. As shown further, our simplified STDP allows a form of powerful unsupervised learning.

### C. Methodology for System-Level Simulation

To validate the use of STT-MTJs as synapses, we performed system-level simulations where STT-MTJs are modeled accurately according to the model of section II. We used a specialized neuromorphic spiking neural network simulator developed in our lab. The simulation is time-step based and simulates CMOS circuits functionally. The simulator is designed for the possibility of including comprehensive physical models for the nanodevices and for their imperfections. This

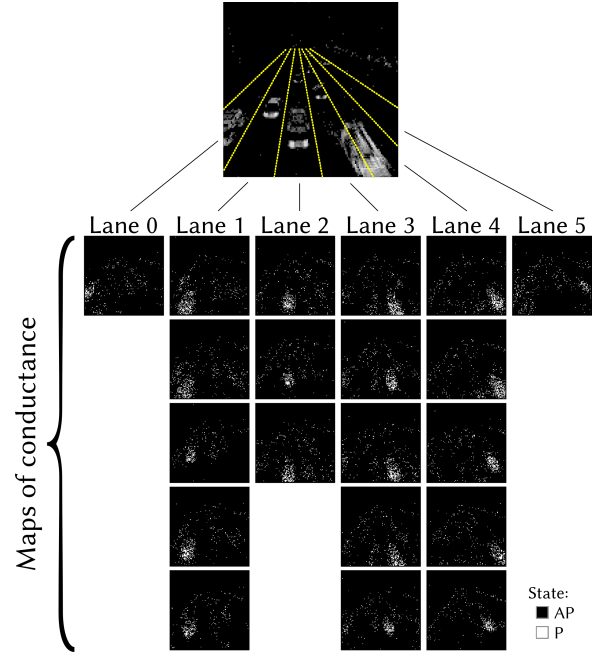


Fig. 4. Representation of the final state of the MTJs. Every subimage represents one output neuron. The state of the MTJs is organized as the input pixels in the image. White is P, black is AP state.

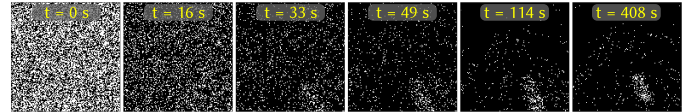


Fig. 5. Evolution of the states of the MTJs connected to one of the output neurons during the learning process, and plotted as in Figure 4.

kind of simulation is much faster than SPICE simulation; for our test application, the simulation time was between 25 and 40 times the real time on a Xeon E5620 processor. This allows us to simulate practical applications, and to perform statistical studies (Monte Carlo simulations).

We based our simulations on a STT-MTJ device representative of a 45 nm technology. The STT-MTJs are ellipses with a width of 40 nm, a length of 100 nm and a free layer thickness of 2 nm. The tunnel magnetoresistance is 150 % (*i.e.*  $R_{AP}/R_P = 2.5$ ).

The programming voltage  $V_{Prog}$  in Figure 3(b) is varied between 0.3 V and 0.6 V, in order to study its impact of the system. Under the constraint of fixed switching probability, the programming pulses duration heavily depends on their amplitude  $V_{Prog}$ . Thus, with the presented geometry and a switching probability of 10%, it ranges from 32.3  $\mu$ s (with  $V_{Prog} = 0.3$  V) to 3.9 ns (with  $V_{Prog} = 0.6$  V). Concerning the reading pulses, they are 1 ns long and 0.1 V high, resulting in an insignificant probability of parasitic switching.

### D. Task Results for Car Detection

For our test application, we presented an 80 seconds video of cars passing on a freeway recorded with a neuromorphic retina [42] (the video is freely available online [60]). This retina, directly inspired by the human retina, works asynchronously



and without frames, and generates spikes when the intensity of a pixel changes. Each pixel of the retina comes in two versions, sensitive to increase and decrease of pixel intensity, respectively.

Each input neuron of our system corresponds to one of the 32,768 pixels of the retina. The system has 20 output neurons and each of them is connected to every input pixel through a synapse made of a single STT-MTJ. We presented the video five times and observed that due to the simplified STDP learning rule, the output neurons naturally specialize on particular lanes and the system effectively becomes a vehicle counter.

The specialization of the output neurons is evident in Figure 4, which shows the final states of the STT-MTJs. The top image represents sample input: we plotted as white every input that spiked during a 30 ms period. The yellow dotted lines materialize the different lanes of the freeway. Every other image represents the final states of the STT-MTJs connected to one of the output neurons (white is P, black is AP). The output neurons are listed according to the lane to which they specialized. The number of output neurons specialized in a given lane is not uniform (lanes 1, 3 and 5 have five specialized output neurons, lane 2 three output neurons, and lanes 0 and 5 only one). This is determined by the number of cars passing on each lane, and the number of pixels activated by a car passing on each lane. In particular, fewer vehicles are passing on lanes 0 and 5 than on other lanes.

Figure 5 shows how a pattern emerges and stabilizes starting from uniform random distribution of synaptic states, in one of the output neurons. Originally, the STT-MTJ states are random. After 33 s, the neuron has started to specialize in lane 4. After 114 s, the states of the STT-MTJs are stabilized.

Once the learning has been achieved, we can deactivate both lateral inhibition and the learning steps, causing the operation of the system to become very low power. Disabling lateral inhibition and learning **is not inspired by biology**, but motivated by engineering purpose. Disabling lateral inhibition slightly increases the detection rate of the system, allowing the system to react to two vehicles passing at the exact same time. Disabling learning decreases the power consumption of the system. Once the system has learnt, it can also be switched OFF and ON without losing its function, since the state of STT-MTJs is nonvolatile.

To estimate the performance of the system on the car detection task, for each line, we chose the output neuron with the best detection rate. This operation can be done automatically by adding a second layer to the network as proposed in [61].

We first consider a situation where the devices are programmed in the intermediate current regime with a voltage  $V_{Prog} = 0.46 V$ , and where device variation is neglected. The STDP programming pulse width is adjusted such that transitions from AP to P and P to the AP both have a probability of 10%.

If we interpret the system as a vehicle counter, the detection rate is 97.3% for the four inward lanes. Detection rate is 62% and 28% for the two outward lanes. The proportion of false positives among the output spikes is 4.7%.

If we do not stop learning and inhibition once the system is stable, the detection rate for the four inward lanes is slightly reduced to 94.6 %, while the proportion of false positives is

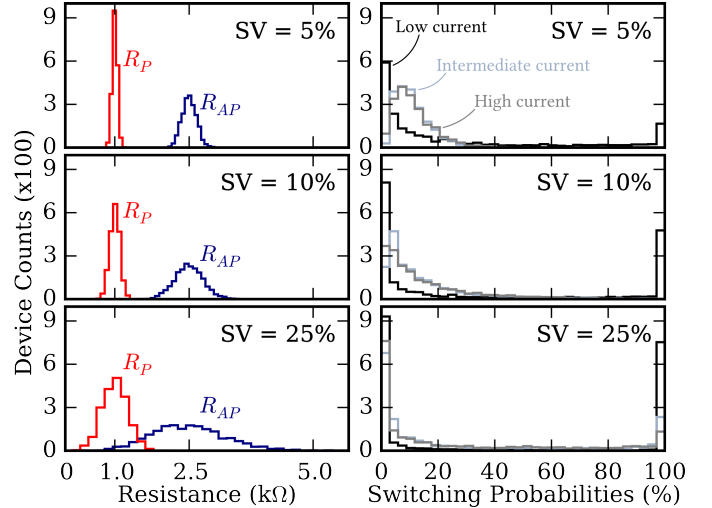


Fig. 6. Histograms representing the values of P and AP states resistance (left subfigures) and switching probabilities (right subfigures) when synaptic variability is introduced. The switching probabilities are represented in the low, intermediate and high programming current regimes (obtained with  $V_{Prog} = 0.3V, 0.4V$  and  $0.6V$  respectively). Switching probability is 10% in all cases for SV=0. From top to bottom, synaptic variability SV is 5%, 10% and 25% of relative standard deviation (one-sigma) on resistance of the P state and TMR.

5.0 %.

The best result on the same dataset, using a neural network with double precision analog weight reports a detection rate of 98.1% and a proportion of false positives of 4.3% [61].

During the learning process, the power consumption for programming the STT-MTJs (excluding the power consumption of the CMOS neurons and of the rest of the system) is only 180 nW, therefore making low power operation possible. We show further that this figure depends tremendously on the chosen programming regime.

Sneak paths represent only a small fraction of the power consumption (8.4%). This is caused by the high parallelism of the STDP operation. However, the proportion of sneak path energy increases linearly with the number of output neurons. The overall power consumption is smaller than in the case of CBRAMs used for solving a similar task [23] due to the low voltage operation and high speed of STT-MTJs in the probabilistic regime.

Interestingly, the performance of the system is only weakly dependent on the actual switching probability of STT-MTJs during learning. If we adjust the programming pulse so that P to AP transitions have a probability of 5% (P to AP remaining 10%), the system detection rate for the four inward lanes drops to 86%.

#### IV. IMPACT OF DEVICE PROPERTIES ON THE NEUROMORPHIC SYSTEM

##### A. Impact of Device Variations

In reality, device variations cause different STT-MTJs to have different probabilities of switching when being applied the same programming pulses. To evaluate the robustness of our approach to this issue, we performed Monte Carlo simulations.

Variations of the minimum and maximum resistances of the MTJs are considered. Since they affect the current that flow through the devices, this kind of variation has a dramatic effect on the probabilities of switching STT-MTJs when programming pulses are applied. This is illustrated in Figure 6. We introduce several levels of Gaussian variability on the resistance of the P state and on the TMR of 2000 STT-MTJs. The synaptic variability SV parameters, 5%, 10% or 25%, represent the relative standard deviation ( $\sigma/\mu$ , one-sigma) of resistance of the P state and TMR. This way of introducing variability is motivated by experimental realizations, which suggest that variations on the resistance of the P state and on the TMR are uncorrelated and have equivalent relative standard deviation [33], [34]. In Refs. [33], [34], the SV parameter was found to be approximately 5%. The degree of variability that we are considering therefore corresponds to extremely high level of variability, in terms of realistic technology. The left subfigures of Figure 6 represent histograms on the values of the resistances of the parallel and antiparallel states. The right subfigures are computed with the model of section II and represent histograms of the switching probabilities of STT-MTJs, for programming pulses whose probability to program STT-MTJs when SV=0 is 10%. Three histograms are superimposed in the low, intermediate and high current regimes. We see that the variability on the switching probabilities is exacerbated with regards to the variability on the resistance states. The variability on the switching probabilities is also considerably higher in the low programming current regime than in the intermediate and high current regimes.

When simulating the whole system, we observed spectacular tolerance of the system to device variation. We first consider the case where the STT-MTJs are programmed in the intermediate current regime. In Figure 7(a), we plotted detection rate and proportion of false positives as a function of synaptic variability in two situations: a situation where we did not stop STDP at the end of learning, and a situation where we stopped it. Without variability, the situation where learning is not stopped has a significantly reduced detection rate compared to when it is disabled. Up to 17% of synaptic variability, no impact is seen on the detection rate in both situations, while as seen in Figure 6, the variability of switching probability is considerable. The degree of robustness is astonishing. When synaptic plasticity is increased above 17%, the detection rate drops sharply in the cases where learning and inhibition are disabled, and more gently in the case where they are not. The case where inhibition is not disabled is more robust, because in the presence of high device variation, some output neurons react preferentially. Inhibition limits their activity.

Figure 7(b) shows the proportion of false positives in the same conditions as Figure 7(a). Similar trends are seen, although the number of false positives starts to increase at a lower synaptic variability (13%) than the detection rate.

Finally, we have also considered transient variations of the properties of the STT-MTJs. We performed simulations where, every time a STT-MTJ is programmed, its device properties ( $R_P$  and TMR) are redrawn randomly with a synaptic variability of 10%. This constitutes an artificially high degree of variations since MTJs properties are experimentally stable from

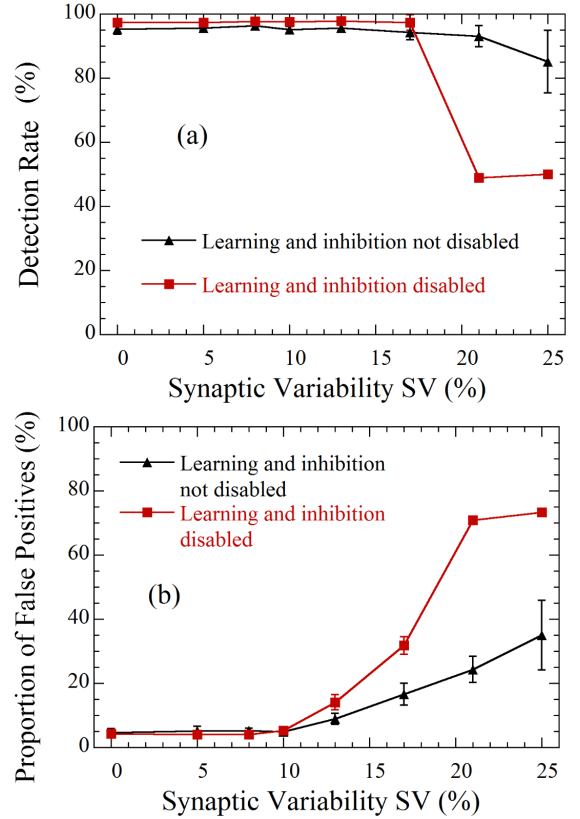


Fig. 7. Detection rate (a) and proportion of false positives (b) as a function of synaptic variability in a situation where learning is disabled at the end of the learning process (squares) or not (triangles). Every simulation was repeated ten times, the error bars represent one standard deviation.

cycle to cycle. Nevertheless, in these conditions our system achieved the same detection rate and number of false positives as in the situation where the MTJs properties are stable.

### B. Impact of the Programming Regime

We have seen in section II that STT-MTJs can be operated in different regimes (low, intermediate and high current). In this part, system level simulations allow us to understand the benefits and drawbacks of the different regimes when using STT-MTJs as synapses.

Without device variations, all regimes allow implementing the same switching probability, and thus lead to the same detection rate and proportion of false positives. However, the energy required to program the STT-MTJs differs significantly. In the intermediate current regime, with a programming voltage of 0.46 V, programming power is 180 nW. In the high current regime, with a programming voltage of 0.6 V, it reaches 220 nW. In the low current regime, with a programming voltage of 0.3 V, it reaches a higher 0.42 mW.

In the presence of device variation, the programming regimes are nonequivalent. This is seen in the Monte Carlo simulations of Figure 8. In the intermediate and high current regimes, the detection rate is robust until a synaptic variability of 17%; it is robust until only 10% in the low current regimes. The number of false positives is robust up to 10% of device variability in

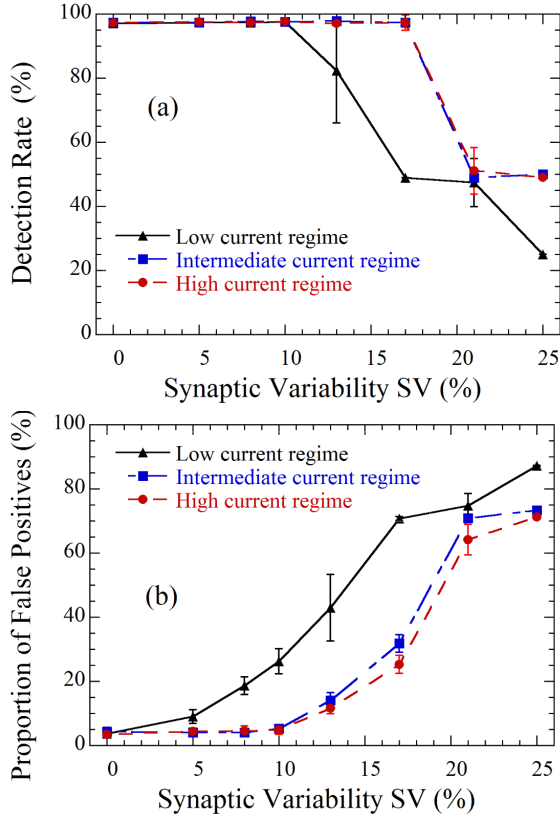


Fig. 8. Detection rate (a) and proportion of false positives (b) as a function of synaptic variability with STT-MTJs programmed in the low (triangles), intermediate (squares) or high (circles) programming regimes. Learning was disabled at the end of the learning process. Every simulation was repeated ten times, the error bars represent one standard deviation.

the cases of intermediate and high programming current, while it increases as soon as there are device variations in the low programming current.

This contrast can be explained by the device physics of STT-MTJs. As seen in section II, in the low current regime, the mean switching time of STT-MTJs has an exponential dependence on the current. In the presence of device variations, each STT-MTJ is programmed with a different current, and therefore has an extremely disparate switching probability. For intermediate and high programming currents, the mean switching time of STT-MTJs has a softer dependence on current than in the low programming current regime.

In summary, intermediate and high programming currents require much smaller programming power than the low programming current and have a better robustness to device variations. Since the intermediate programming current uses smaller voltages than the high programming current regime, STT-MTJs have a better reliability in this regime. The intermediate programming therefore appears as the ideal regime for synaptic use of STT-MTJs. This differs from traditional memory applications of STT-MTJs, where programming speed is the major concern and where the high programming current may be a better choice.

## V. CONCLUSION

In this work, we interpreted magnetic tunnel junctions' behavior as a stochastic memristive synapse. The stochastic effects were modeled accurately using analytical physical equations. The mean switching time can be tuned over many decades, and STT-MTJs can be programmed in three different regimes. Low voltages are used for programming and are symmetric between positive and negative polarizations. We introduced a neural network-inspired system that can exploit this stochastic effect to perform unsupervised learning. The switching probabilities of the nanodevices do not need to be controlled perfectly, as the system is robust to device mismatch, which is evidenced by Monte Carlo simulations. The intermediate programming current regime minimizes energy consumption and leads to high robustness to device variations. This regime appears to be ideal for the use of STT-MTJs as synapses.

Future works address the optimized circuits for using STT-MTJs as synapses, which might differ from the circuits used for using STT-MTJs as memory [62], and the physical realization of hybrid CMOS/stochastic synapse circuits. From a system point of view, the architecture should be advanced for demonstrating more complex applications.

This work also gives insight into a new way to use memristive nanodevices. Unpredictability caused by nanoscale physics is not necessarily an enemy but can become the foundation for efficient processing using novel computing paradigms.

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TOPEN BAMBI project, which explore the new paradigms for nanoelectronics based on Bayesian inference.