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A MINIATURIZED THREE-PORT DIVIDER/COMBINER

A.-L. Perrier,¹ J.-M. Duchamp,² and P. Ferrari²

¹ LAHC, University of Savoie, 73376 Le Bourget-du-Lac, France;

Corresponding author: anne-laure.perrier@grenoble.cnrs.fr

² IMEP, INP of Grenoble, BP 257, 38016 Grenoble cedex 1, France

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ABSTRACT: We propose a new topology based on a semi-lumped complex impedance transformer for the design of miniaturized power dividers. Our design is based on an impedance transformer in the input branch and a loop in the output branches. The input impedance transformer is constituted by a transmission line loaded with a capacitor. A prototype has been realized using hybrid technology for a 1 GHz operating frequency. The electrical length of the device is 26.4°. This leads to a miniaturized device, more than three times shorter than a typical Wilkinson power divider. This divider exhibits insertion loss lower than 0.3 dB, return loss better than 20 dB and the isolation between the two output ports above 20 dB. Moreover, the low-pass behavior of the input impedance transformer leads to a good rejection of the third harmonic. © 2007 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 50: 72–75, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23008

Key words: output isolation; harmonic rejection; miniaturized device; power divider

1. INTRODUCTION

The technical maturity of power dividers dates from the sixties when Wilkinson published a paper on a N -port divider (with N even or odd) [1]. The main aim of this kind of divider is to uniformly spread the input power P into N output ports. All outputs are in phase and have a P/N power. Another significant property is the good isolation between output ports. Wilkinson's dividers are designed with quarter-wave transmission lines.

In general, power dividers can be classified in two groups: three-port and four-port dividers. Since 1960, several researches on the three-port dividers have been carried out, with main objectives to increase the bandwidth by increasing the number of sections [2], to distribute a nonuniform power to each output [3], to decrease the size of the devices using lumped elements [4–6] and to eliminate the spurious harmonics [7]. All these researches are based on real or artificial quarter-wave transmission lines, used as impedance transformers to change a resistive load into another one. In parallel, researches were performed on complex impedance transformers, not based on quarter-wave transmission lines. A principle was shown in 1967 [8].

In this paper, we show a compact topology of power dividers having the same properties as the Wilkinson power dividers. They are based on a complex impedance transformation. From the output to the input: the output branches transform a resistive load into a complex load using a small-length transmission line; this complex load is then transformed to a resistive load thanks to a small-length complex impedance transformer. This topology, proposed for a tunable power divider in 2006, leads to miniaturized and fixed power dividers with a harmonic rejection [9]. The complex impedance transformer is realized by a transmission line loaded by a capacitor, leading to a slow-wave and low-pass behavior.

The miniaturized power divider is described in Section 2, design equations are developed in Section 3 and design charts are carried in Section 4, whilst Section 5 shows simulated and mea-

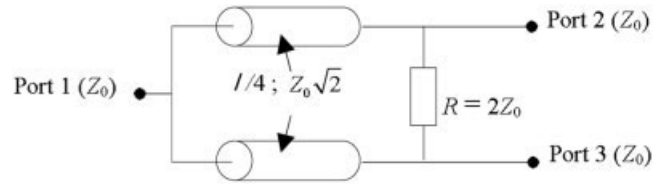


Figure 1 Wilkinson power divider

sured results carried out on a hybrid prototype. Conclusion draws out the agreement between simulated and measured results.

2. PRINCIPLE

A classical three-port Wilkinson power divider is constituted by a T junction and two output impedance transformers (see Fig. 1). A resistor between the output ports is necessary to achieve output ports isolation.

Figure 2 shows the topology of the power divider proposed in this article. As shown in [9], this topology can be divided in two blocs: an “input transformer” and an “output loop.” This loop is necessary to achieve isolation between the two output ports (ports 2 and 3). θ_i is the electrical length and Z_i the characteristic impedance of the transmission line “ i .” Contrary to the Wilkinson power divider, the impedance transformer is split between the input port and the output loop. The input impedance at the junction point (J), seen from ports 2 and 3, is not necessarily equal to the matching input impedance (usually 50 Ω). The input transformer differs from [9], it is just composed by one capacitor and one transmission line.

3. DESIGN EQUATIONS

To extract design equations, the even and odd mode approach has been used.

3.1. Even Mode

In the even mode, the symmetrical axis of the divider can be replaced by a magnetic wall, i.e., an open circuit. In this case, the capacitor and the resistor of the output loop can be removed. The input impedance Z_{in} seen at the input of the output loop (J) can be calculated:

$$Z_{in} = \frac{\left(\frac{Z_0 + jZ_2 \tan(\theta_2)}{Z_2 Z_2 + jZ_0 \tan(\theta_2)} \right)^2}{2Z_2 \frac{Z_0 + jZ_2 \tan(\theta_2)}{Z_2 Z_2 + jZ_0 \tan(\theta_2)}} \quad (1)$$

$$Z_{in} = \frac{\frac{Z_0}{2} + j\frac{Z_2}{2} \tan(\theta_2)}{\frac{2}{Z_2} \frac{Z_0}{2} + j\frac{Z_0}{2} \tan(\theta_2)} \quad (2)$$

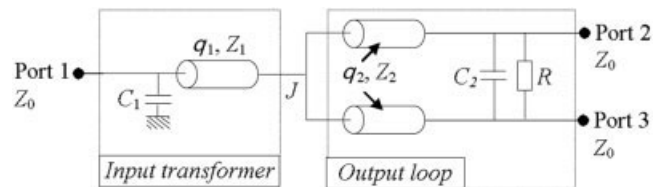


Figure 2 Topology of the proposed power divider

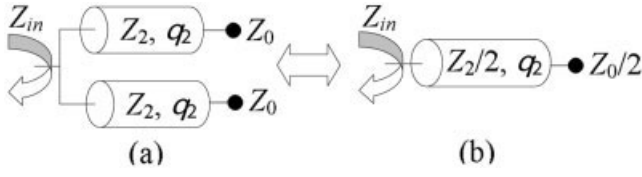


Figure 3 Output loop equivalent electrical circuit for the even mode

Relation (2) shows that the Z_{in} impedance can resume itself as the transformation of $Z_0/2$ through a transmission line with $Z_2/2$ characteristic impedance and θ_2 electrical length. Hence the two transmission lines and the two output ports of the output loop can be replaced by one transmission line and one port as described in Figure 3.

Figure 4 shows the equivalent electrical circuit of the power divider for the even mode.

The impedances Z_e , Z'_e and Z''_e seen along the divider are given by:

$$Z''_e = \frac{Z_0}{1 + jZ_0 C_1 \omega}, \quad (3)$$

$$Z'_e = Z_1 \frac{Z''_e + jZ_1 \tan(\theta_1)}{Z_1 + jZ''_e \tan(\theta_1)}, \quad (4)$$

$$Z_e = \frac{Z_2 Z'_e + j \frac{Z_2}{2} \tan(\theta_2)}{\frac{2Z_2}{2} + jZ'_e \tan(\theta_2)}. \quad (5)$$

When the port impedances are purely real, two equations can be defined to realize the power divider output matching:

$$\text{Re}[Z_e(Z_1, Z_2, \theta_1, \theta_2, C_1 \omega)] = \frac{Z_0}{2} \quad (6)$$

$$\text{Im}[Z_e(Z_1, Z_2, \theta_1, \theta_2, C_1 \omega)] = 0 \quad (7)$$

These two equations with five unknowns lead to an infinity of solutions. They will be displayed on several charts in Section 4.

3.2. Odd Mode

Whilst using the odd mode, the symmetrical axis of the power divider can be replaced by an electrical wall, i.e., a short circuit. In that case, the input transmission line and the first capacitor are short circuited. The equivalent electrical circuit of a half power divider is given in Figure 5 for the odd mode.

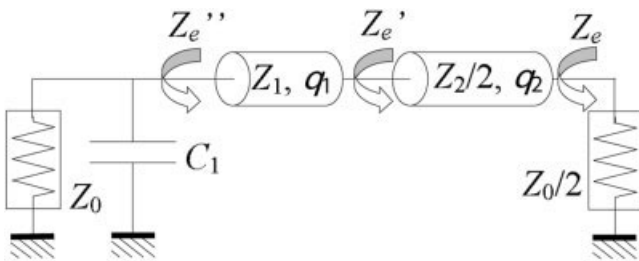


Figure 4 Equationivalent electrical circuit of the power divider for the even mode

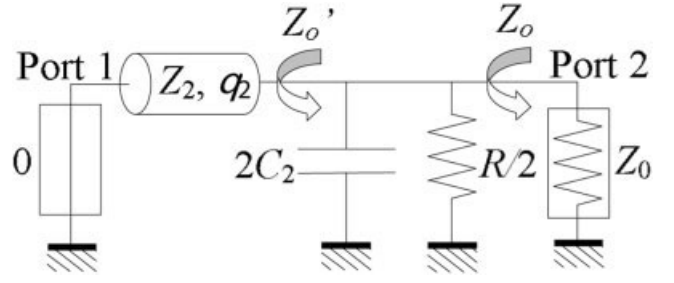


Figure 5 Equationivalent electrical circuit of a half divider for the odd mode

The impedances Z_o and Z'_o seen along the half power divider can be calculated as:

$$Z'_o = jZ_2 \tan(\theta_2), \quad (8)$$

$$\frac{1}{Z_o} = \frac{2}{R} + j2C_2 \omega + \frac{1}{Z'_o}. \quad (9)$$

When the port impedances are purely real, like for the even-mode, two other equations should be verified to realize the power divider output matching:

$$\text{Re}[Z_o] = \frac{2RZ_2^2 \tan^2(\theta_2)}{(R - 2RC_2 \omega Z_2 \tan(\theta_2))^2 + (2Z_2 \tan(\theta_2))^2} = Z_o \quad (10)$$

$$\text{Im}[Z_o] = -j \frac{RZ_2 \tan(\theta_2)[R - 2RC_2 \omega Z_2 \tan(\theta_2)]}{(R - 2RC_2 \omega Z_2 \tan(\theta_2))^2 + (2Z_2 \tan(\theta_2))^2} = 0 \quad (11)$$

Considering only the physical solution $[R - 2RC_2 \omega Z_2 \tan(\theta_2)] = 0$, R and $C_2 \omega$ can be extracted from the two Eqs. (10) and (11), leading to:

$$R = 2Z_o \quad (12)$$

$$C_2 \omega = \frac{1}{2Z_2 \tan(\theta_2)} \quad (13)$$

4. DESIGN CHARTS

Design charts have been derived from the design Eqs. (6), (7), (12), and (13) obtained from the even-odd mode theory.

The design charts of Figure 6 give the characteristic impedances Z_1 and Z_2 and the reactances $1/C_1 \omega$ and $1/C_2 \omega$ versus the total electrical length $\theta_{tot} = \theta_1 + \theta_2$. The ratios $x = Z_1/Z_2$ and $y = \theta_1/\theta_2$ are used as design parameters.

These charts allow synthesizing various power dividers. In practice, the technology and the substrate used limit the choice of the characteristic impedances and capacitors values.

5. REALIZATION AND RESULTS

To illustrate the new concept developed for the design of miniaturized power dividers, a prototype has been realized in a hybrid technology using surface mounted capacitors. For simplicity, the design has been done for a 1 GHz operating frequency. We choose $x = 1$ and $y = 1$ and the characteristic impedance of the transmission lines is fixed to 85Ω . These choices lead to $\theta_{tot} = 26.4^\circ$ as shown in Figure 6, so $\theta_1 = \theta_2 = 13.2^\circ$.

The device was designed in microstrip technology on a Rogers™ RO4003 substrate (relative permittivity $\epsilon_r = 3.36$,

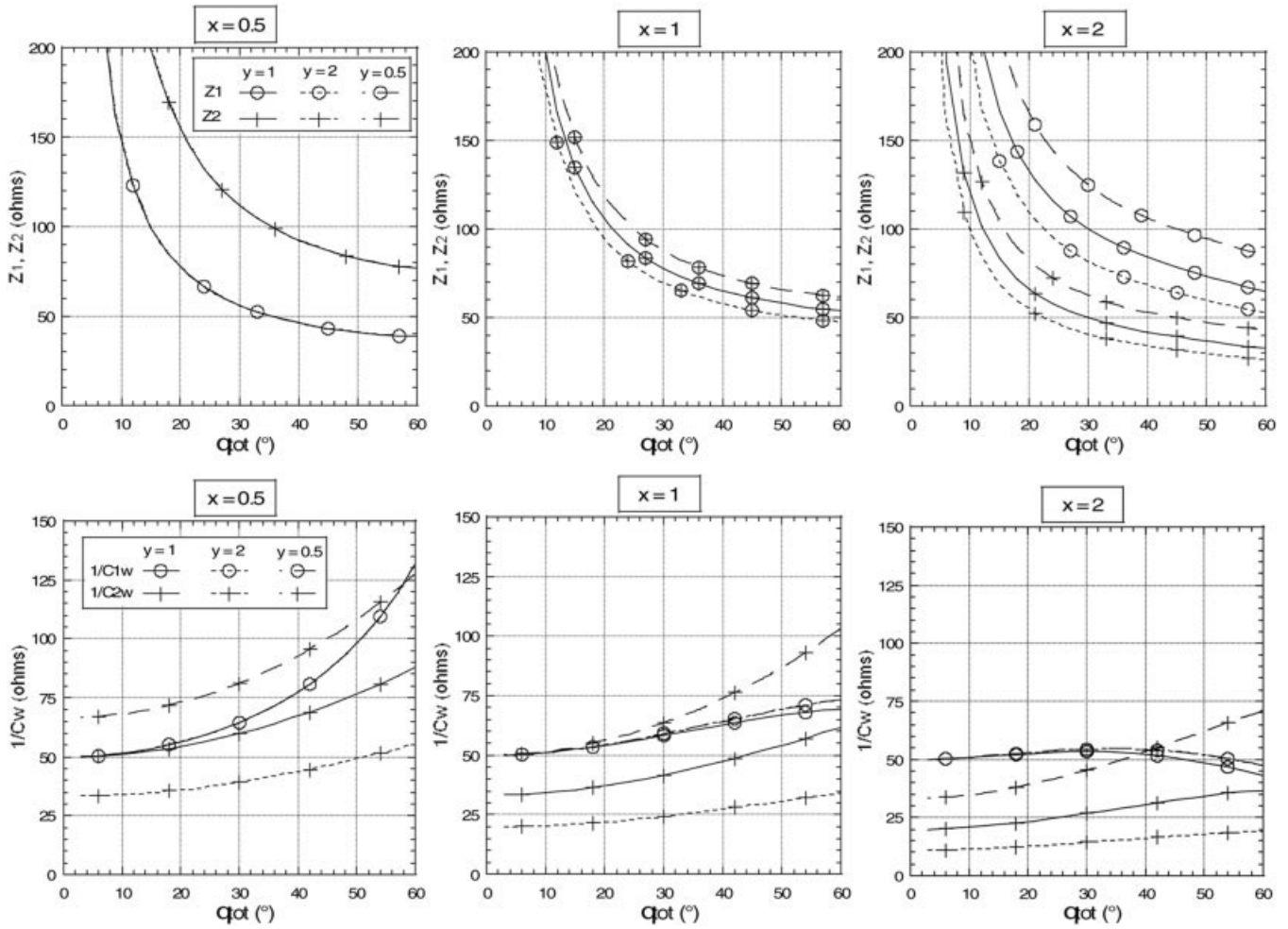


Figure 6 Z_1 , Z_2 , and $1/C_1\omega$, $1/C_2\omega$ versus x , y , and θ_{tot}

dielectric loss $\tan \delta = 0.0035$, height $h = 813 \mu\text{m}$, and copper thickness $t = 35 \mu\text{m}$). The width of the two transmission lines has been set to $667 \mu\text{m}$ (characteristic impedance = 85Ω). The transmission lines lengths are 7 mm to reach the 13.2° electrical length, for each transmission line. We noted that the total electrical length is 39.6° (3×13.2), leading to a miniaturized power divider compared to the 180° ($2 \times 90^\circ$) of the Wilkinson power divider. The total length is divided by 4.5.

The values $C_1 = 2.8 \text{ pF}$ and $C_2 = 4 \text{ pF}$ given by the charts (see Fig. 6) are not normalized surface mounted capacitors, they have been replaced by $C_1 = 3 \text{ pF}$ and $C_2 = 3.9 \text{ pF}$. The photography of the power divider is shown in Figure 7. The first capacitor is connected to the ground plane with a via and the second capacitor is connected between the two output ports.

Simulated and measured results are shown in Figure 8. Simulations were carried out with ADS [10]. Measurements were carried out with a WILTRON™ 360 Vector Network Analyzer and a standard Short-Open-Load-Thru (SOLT) calibration procedure.

The agreement between these results is correct at the operating frequency. S_{11} , S_{22} , and S_{32} minima are centered on 1 GHz as predicted in simulation. The measured bandwidth at -20 dB is 20% for S_{11} , 10% for S_{22} , and 10% for S_{32} . On the whole bandwidth, S_{21} varies between -3.1 dB and -3.4 dB , leading to less than 0.4 dB insertion loss. Insertion loss is minimum (0.1 dB) at 1 GHz .

However, variations are important, especially on S_{21} , for frequencies higher than 2 GHz . Measured results show a transmission

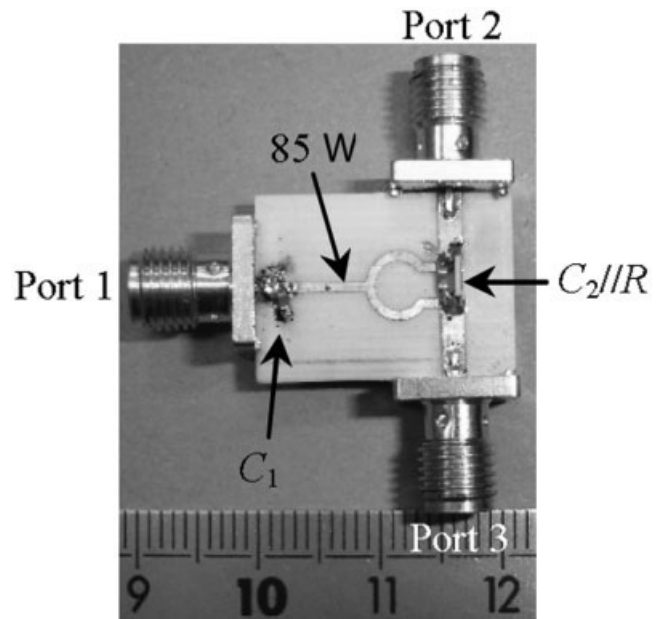


Figure 7 Photography of the power divider

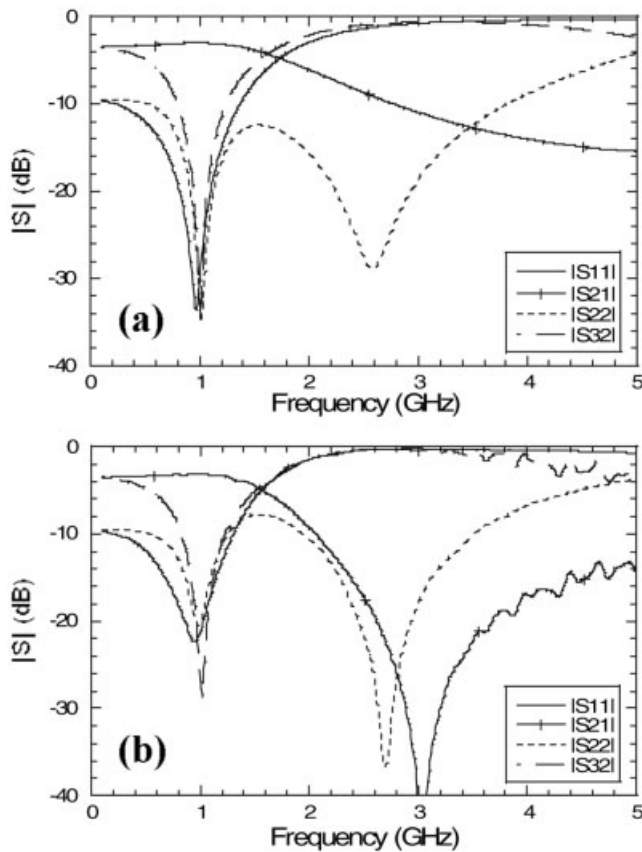


Figure 8 (a) Simulated and (b) measured results of the miniaturized power divider with $C_1 = 3$ pF and $C_2 = 3.9$ pF

zero around 3 GHz. These differences are firstly because of the surface mounted capacitors parasitic elements, and secondly to the finite width of the transmission lines, leading to uncertainties in the electrical lengths because of the junction (J) and the capacitors position. The transmission zero is due to the parasitic series inductance leading to the behavior of an elliptic filter with a transmission zero frequency equal to:

$$\omega_0 = \frac{1}{\sqrt{L_s C_1}} \quad (14)$$

This transmission zero can be very useful in the case of the use of the power divider for small bandwidth applications where the third harmonic ($3f_0$) is undesirable [7]. An additional inductance can be added in practice to adjust the frequency of the transmission zero.

This new topology allows realization of power divider more compact than device presented by Ahn and Wolff [6] with the same transmission line characteristic impedance. In their publication [6], a power divider constituted by two 15.3° electrical length transmission lines is proposed with characteristic impedance of 195.9Ω . For the same characteristic impedance, our topology, with $x = 1$ and $y = 1$ (see Fig. 6), allows to conceive a power divider constituted by three 5° electrical length transmission lines with $\theta_{\text{tot}} = 10^\circ$. So our new topology is more compact in term of length and in term of surface.

6. CONCLUSION

A new topology of miniaturized equal three-port power dividers has been proposed. Based on an input impedance transformer and

a small length output loop, it is not based on the classical quarter wave length transmission lines.

Design equations and charts have been carried out with the even-odd mode theory. A prototype has been realized in a hybrid technology with surface mounted capacitors, to validate the approach. The prototype was realized to operate at 1 GHz. The total electrical length of the device is only 39.6° compared with 180° for a classical Wilkinson power divider. A 10% bandwidth, sufficient for small bandwidth applications, is obtained at -20 dB on S_{11} , S_{22} , and S_{32} parameters. The insertion loss is low as 0.1 dB at the center frequency and limited to 0.4 dB for the whole bandwidth.

An additional inductance can be added in series with the capacitor of the input impedance transformer to reject an undesired harmonic.

These performances lead to a possible integration for a device in a monolithic microwave integrated circuit (MMIC) technology.

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