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# 40 Gop/s/mm<sup>2</sup> fixed-point operators for Brain Computer Interface in 65 nm CMOS

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**Abstract**—The performance of non-invasive Brain-Computer Interface (BCI) depends on the computing performance of the system which solves the inverse problem. So the number of basic operations computed per second determines the BCI's resolution. Architecture with pipelined and parallelized flow is then required, and each operator in this architecture must be optimised to reach the highest possible computing performance. This paper presents the implementation of a fixed-point reciprocal and an inverse square root operators for the STMicroelectronics 65 nm CMOS technology. This paper follows previous works that optimise these operators on FPGA target. Each operator reaches a computing performance of about 40 Gop/s/mm<sup>2</sup>, which improves the literature results by a factor of four. Thus, this works fits well for portable and high performance BCI applications.

## I. INTRODUCTION

A Brain Computer Interface (BCI) is a hardware and software system that allows controlling computer or other devices with cerebral activity. The invasive BCI has direct access to the brain signals but is expensive and requires a surgical operation. So, this method is not appropriate to equip many people with this technology. Electroencephalogram (EEG) permits to perform a non-invasive BCI but this method has low resolution if the measured signals are directly used to control a computer. The EEG inverse problem can then be solved in order to determine, from these signals, which dipoles are active in the brain. The larger the number of considered dipoles is, the better the accuracy is, but also the larger the computation time is. For real-time, portable and accurate BCI applications, dedicated circuits have to be designed in a parallelized and pipelined way, so that they provide high computing performance, while minimizing the silicon area. Moreover this requires to process data not with the too complex floating-point format but with the fixed-point format.

Field-Programmable Gate Array (FPGA) devices are great for prototyping proof of concepts and validating algorithm implementations on hardware. Nevertheless, Application-Specific Integrated Circuits (ASICs) reach higher computing frequency and provide a better area integration. Any operator implementation may be optimised in different ways when

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compared to the original FPGA implementation. Indeed, ASICs provide access to custom designs, which offer different implementation strategies and foster more adequate operator architectures.

The EEG inverse problem algorithm contains operations such as division or square root [1]. In the case of a pipelined architecture, each operator must be optimised to provide the best possible computing frequency. Reciprocal and inverse square root are intermediate steps to compute division and square root. The implementation of these operators is not straightforward and requires special care due to application's constraints, for both FPGA and ASIC implementations. Several methods to compute reciprocal and inverse square root can be pipelined, for example Look-Up Tables (LUTs) or the CORDIC algorithm [2]. These solutions may have some issues like necessary resources, latency or computing frequency when the size of the input increases. The iterative Newton-Raphson method is favored for floating-point implementations since it takes advantage of the mantissa value being in the interval  $[1, 2[$ . Indeed, this knowledge on the input allows the initial value to be easily computed and then to roughly double the number of bits of accuracy in each iteration. Newton-Raphson method can be used for both reciprocal and inverse square root [3], [4]. Its implementation usually relies on a memory block used to store coefficients required for the first step of the algorithm. In fixed point format, these operators require special attention, since the input values do not benefit from the mantissa property and thus require a specific computation for the first approximation. Previous work presented Scaling-Less Newton-Raphson (SLNR) architectures [5], [6] designed to maximise the computing frequency on Xilinx FPGAs but which are not optimised for an ASIC implementation.

In this paper, ASIC implementations of high computing performance fixed-point reciprocal and inverse square root operators for the STMicroelectronics 65 nm CMOS are presented. These operators reach the frequency of 1.587 GHz and occupy less than 40 000  $\mu\text{m}^2$ , which corresponds to a computing performance of 41 Giga operations per second and per  $\text{mm}^2$  (Gop/s/mm<sup>2</sup>). So the proposed architecture is a good answer to

the high-performance BCI constraints. This paper is organized as follows. Section II presents the Newton-Raphson method for both operators and its possible implementations with the impact on the maximum clock frequency on Xilinx FPGA. Different Newton-Raphson solutions for the STMicroelectronics 65 nm CMOS target are described in Section III. Then, a comparison with another 65 nm CMOS reciprocal architecture is done in Section IV. Finally, Section V concludes the paper.

## II. RELATED WORK

The Newton-Raphson algorithm can be used to compute the reciprocal or the inverse square root of a number  $a$ . This iterative algorithm doubles the number of bits of accuracy during each iteration. The final result  $x_n$  is obtained after  $n$  iterations of these equations:

$$\text{Reciprocal: } x_{i+1} = x_i(2 - ax_i) \quad (1)$$

$$\text{Inverse square root: } x_{i+1} = \frac{x_i}{2}(3 - ax_i^2) \quad (2)$$

The value  $x_0$  is the first approximation of the desired result and is provided as input with  $a$ . Thus,  $x_0$  has to be determined before computing the iteration equation. The usual method involves scaling the input  $a$  in a predetermined interval as  $[1, 2[$ , or  $[0.5, 1[$  [3], [7]. Then,  $x_0$  can be calculated by using coefficients stored in a memory block. This yields a good accuracy for the first approximation and then decreases the number of required Newton-Raphson iterations. In previous work, it was showed that this strategy is not the best to maximise the operating frequency on Xilinx FPGAs [5], [6]. These Scaling-Less Newton-Raphson (SLNR) architectures do not need any coefficients, so memory block is not required. This lack of memory block allows increasing the computing frequency because of hardware target features. In fact, on Xilinx FPGAs, the maximum frequency of BRAMs is lower than one of DSP cells, used for the multiplications. Table I shows the difference on Virtex-7 FPGAs, which rely on the 28 nm technology [8]. Therefore coefficients must be avoided

TABLE I  
MAXIMAL FREQUENCY COMPARISON BETWEEN DSP CELL AND BRAM  
ON VIRTEX-7 FAMILY FPGAS

|         | Max frequency |
|---------|---------------|
| DSP48E1 | 740 MHz       |
| BRAM    | 601 MHz       |

to generate the first approximation  $x_0$ . The method proposed in [5], [6] is based on the Leading One Detector (LOD) of  $a$ . A simple combinatory circuit can then be used to determined a first approximation that respects the conditions of convergence :

$$\text{Reciprocal: } 0 < a \times x_0 < 2. \quad (3)$$

$$\text{Inverse square root: } 0 < a \times x_0^2 < 3. \quad (4)$$

The accuracy of the first approximation determines the number of required Newton-Raphson iterations. So the products in the conditions of convergence have to be as close as possible to the numerical value 1. Finally, the SLNR architectures ensure this accuracy for the first approximation:

$$\text{Reciprocal: } 0.875 < a \times x_0 < 1.125. \quad (5)$$

$$\text{Inverse square root: } 0.5 < a \times x_0^2 < 1.125. \quad (6)$$

FPGA implementation results for both operators are presented in Table II. The critical path in these architectures is located in the DSP cells for multiplication and gives a 740 MHz computing frequency on a Virtex7-690T. So the SLNR designs fit with high throughput applications on Xilinx FPGAs. This maximum value of 740 MHz is due to the physical structure of the FPGA. Higher computing frequency could be profitable to BCI applications. This explains the desire to adapt SLNR architectures to the ASIC technology.

TABLE II  
IMPLEMENTATION RESULTS: 16-BIT RECIPROCAL AND INVERSE SQUARE  
ROOT ON VIRTEX-7 690T

| Operator            | Reciprocal | Inverse square root |
|---------------------|------------|---------------------|
| LUT                 | 111        | 306                 |
| Flip-Flop           | 240        | 262                 |
| DSP                 | 6          | 9                   |
| Clock cycles        | 20         | 34                  |
| Max frequency (MHz) | 740        | 740                 |

## III. FIXED-POINT NEWTON-RAPHSON ARCHITECTURES FOR A 65 NM CMOS ASIC

The SLNR architectures introduced in Section II offer the maximum computing frequency on Xilinx FPGAs. Since every hardware target is different, it must be verified that the SLNR architectures yield the highest computing frequency for 65 nm CMOS ASIC. The goal here is to minimise the critical path and the silicon area. A memory-based Newton-Raphson alternative to SLNR can be considered to improve the first approximation and reduce the number of iterations while providing the same accuracy as shown in Fig. 1. Both architectures are proposed for a 16-bit input named  $a$ , resented with 8 bits for integer and fractional parts. So, for the memory-based solution, the input must be scaled in order to have  $a_s$  in the interval  $[1, 2[$ . The 10 most significant bits of  $a_s$  are used as the address of the RAM. In this way,  $x_0$  is the approximation of the desired value with 10 bits of accuracy. The following Newton-Raphson iteration block ensures the 16-bit accuracy. The output must then be similarly scaled to have the desired value. A synthesis with Encounter RTL Compiler states that the multiplier is the most impactful element on the critical path for the SLNR architecture. The delay can not be reduced, because the multipliers are already between two registers, so that multiplier's propagation delay of 593 ps becomes the comparison reference.



non-pipelined and generic architecture in [9] is not specific to reciprocal or inverse square root computation but is the most effective ASIC implementation in the latest literature. [9] uses a cubic Chebyshev interpolator, which relies on 4 coefficients sets stored in a Lookup-table, as presented in Fig. 4. The Lookup table is composed of 4 memory blocks. The coefficients can be changed in order to compute different functions. The architecture contains 5 multipliers (Multiplier #1 to 3, squarer and cuber). The value  $x$  is the input of the architecture and, for the reciprocal computation, must belong to the interval  $[1, 2]$ . The reciprocal operator synthesis for the IBM 65 nm CMOS technology is done. Table V compares [9] and the memory-based Newton-Raphson reciprocal operator.

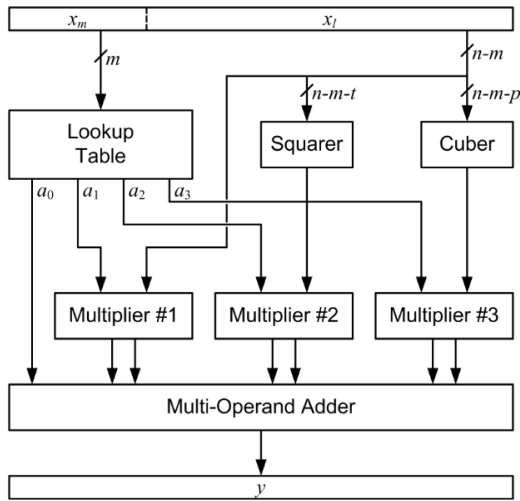


Fig. 4. Cubic Chebyshev interpolator architecture [9]

If [9]’s solution is changed in order to be pipelined, the critical path would be at least equal to the memory delay and then the maximum frequency would be equal to 0.820 GHz. Then, the use of memory blocks has an impact on the occupied area by this architecture. Indeed, the surface required by the memory-based Newton-Raphson solution is twice as small. Finally, the memory-based Newton-Raphson provides 4 times better computing performance than [9]. Table VI presents the results for memory-based Newton-Raphson architectures. Each operator has a similar computing performance and then is a good implementation to save area. So the proposed ASIC implementation improves both the computing frequency and the occupied silicon surface.

## V. CONCLUSION

In this paper, the fixed-point SLNR architecture presented in previous work is investigated on the 65 nm CMOS technology and compared with a memory-based Newton-Raphson solution. These solutions have similar computing performance and their use depends on the rest of the algorithm. The computing performance can be increased up to 41 Gop/s/mm<sup>2</sup>, which is a literature improvement by a factor of 4. Thus, this solution

TABLE V  
65 NM COMPARISON BETWEEN 16-BIT RECIPROCAL SLNR AND CUBIC CHEBYSHEV ARCHITECTURES

| Architecture             | Memory-based NR | [9]      |
|--------------------------|-----------------|----------|
| Memory                   | 1024 x 16       | 512 x 20 |
|                          |                 | 512 x 12 |
|                          |                 | 512 x 12 |
|                          |                 | 512 x 10 |
| Memory delay (ns)        | 0.630           | 1.22     |
| Multipliers              | 2               | 5        |
| Maximum frequency (GHz)  | 1.587           | 0.360    |
| Area ( $\mu\text{m}^2$ ) | 38 527          | 95 700   |
| Gop/s/mm <sup>2</sup>    | 41              | 9        |

TABLE VI  
STMICROELECTRONICS 65 NM CMOS RESULTS FOR MEMORY-BASED NEWTON-RAPHSON RECIPROCAL AND INVERSE SQUARE ROOT

| Operator                 | Reciprocal | Inverse Square Root |
|--------------------------|------------|---------------------|
| Multipliers              | 2          | 3                   |
| Maximum frequency (GHz)  | 1.587      | 1.587               |
| Area ( $\mu\text{m}^2$ ) | 38 527     | 39 683              |
| Gop/s/mm <sup>2</sup>    | 41         | 40                  |

fits the BCI requirements and offers a good trade-off between operating frequency and silicon area.

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