



Semi-Iterative Analogue Turbo Decoding

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■ Introduction

- Analogue decoding has many advantages
 - high speed,
 - low power consumption,
 - small elementary operator area,
- and traditionally two main drawbacks
 - a huge **area** for a full parallelized implementation,
 - a circuit is **dedicated** to a single frame length.
- Solution: **reduce parallelism and propose reconfigurability**
 - mixed signal sliding window decoding [M. Mörz: *Analog Sliding Window Decoder Core for Mixed Signal Turbo Decoder*. - In: Proc. Int. ITG Conference on Source and Channel Coding, Erlangen, Germany, January 2004, p. 63-70],
 - **semi-iterative analogue turbo** decoding, applied to the **DVB-RCS** standard.

■ Outline

- **Analogue slice turbo decoder**
 - Slice principle
 - Architecture
 - Limitations
- **Semi-iterative turbo decoder**
 - Motivations
 - Architecture
 - Area
 - Simulations
- **Reconfigurability**
 - MAP decoder
 - Turbo decoder
 - Analogue vs. digital

Outline

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- **Analogue**
 - **slice turbo**
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- Conclusion

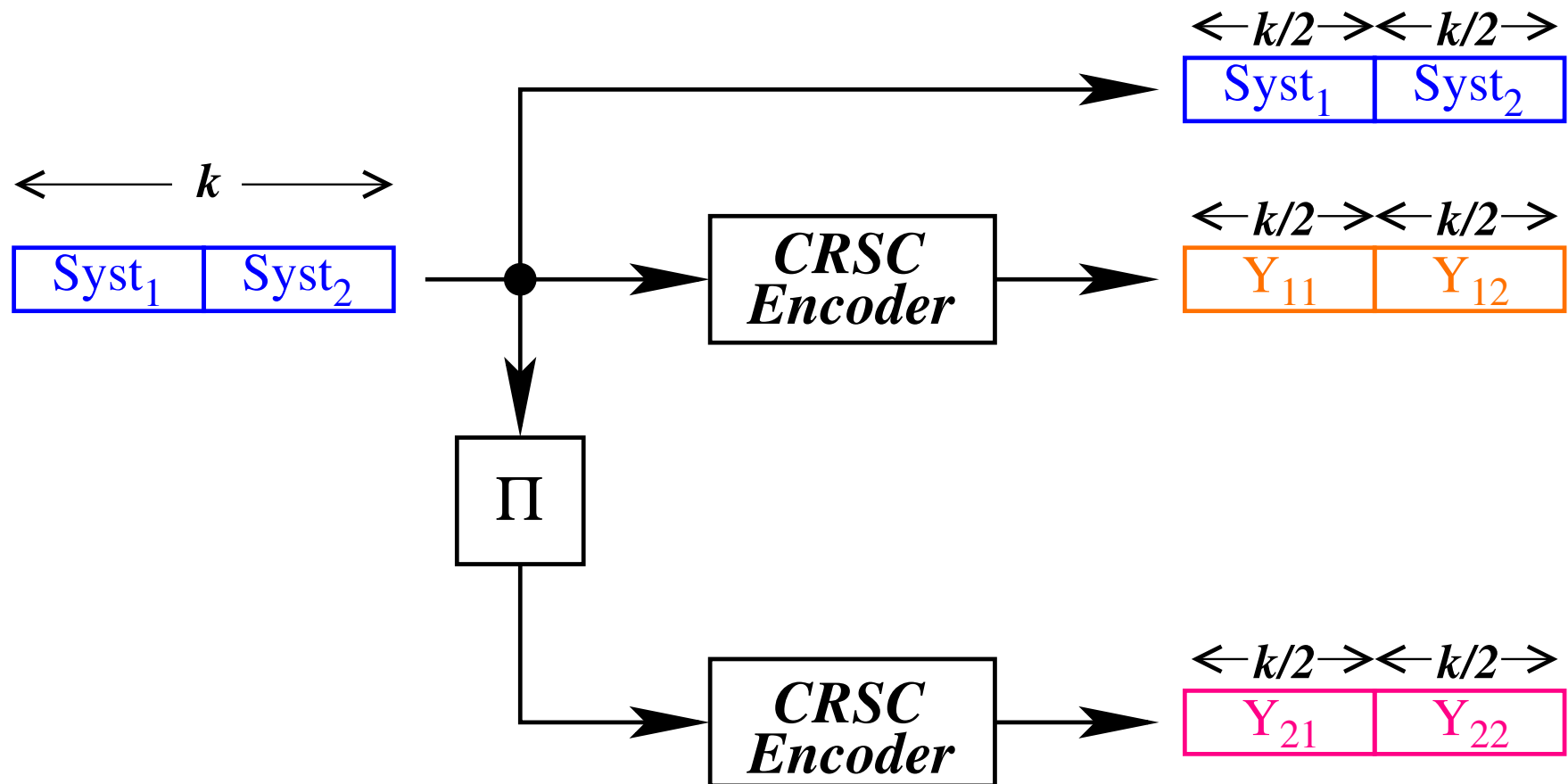
Analogue slice turbo decoder

■ Slice turbo encoding

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p -slice turbo code

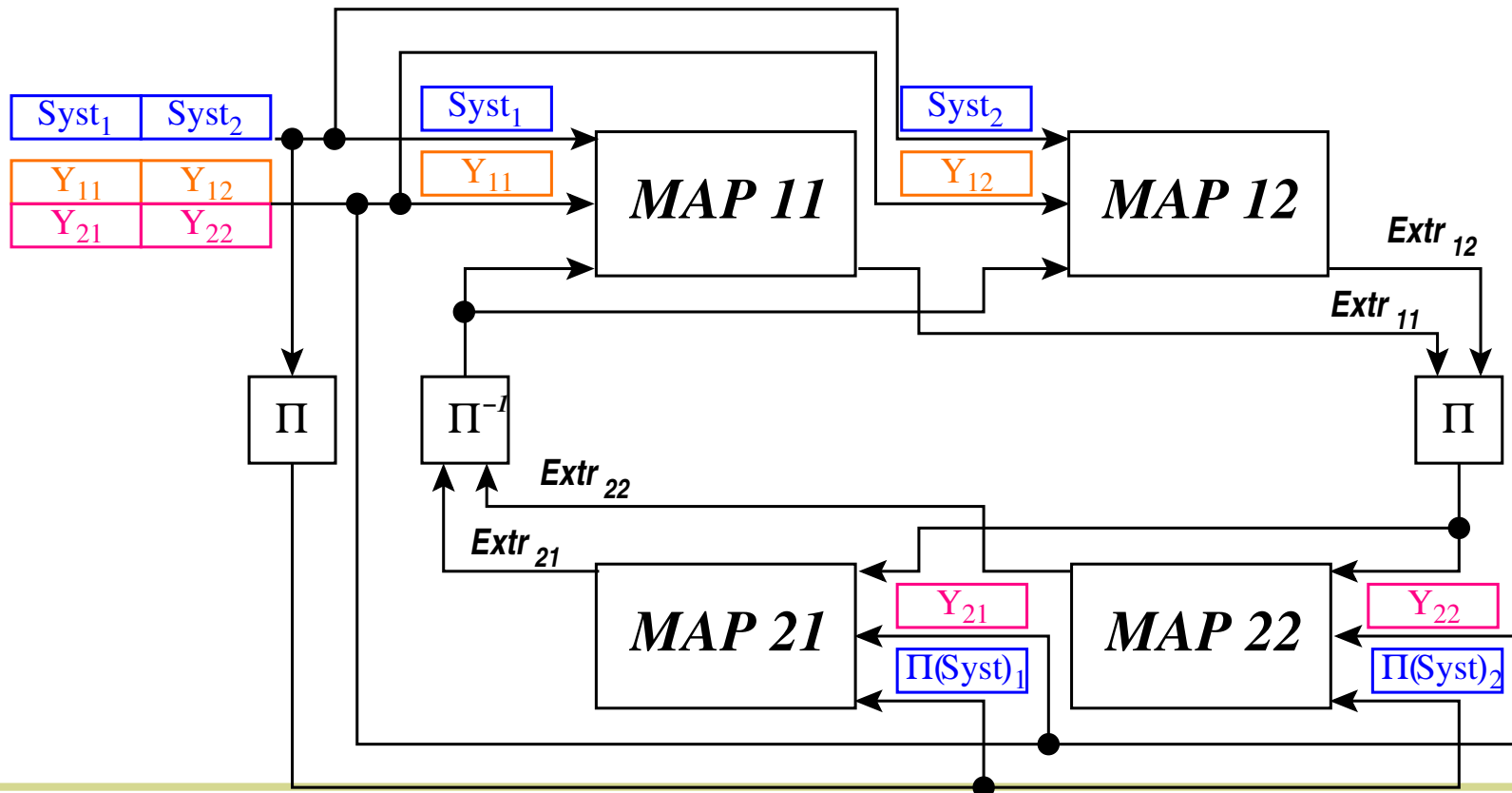
- Frame divided into p parts of same length m .
- **Circular** Recursive Systematic Convolutional code.
- Interleaving on the $k = p \cdot m$ systematic symbols.

Decoder architecture

- MAP on 24 double-binary symbols \rightarrow slice turbo on 48 symbols (shortest frame of the DVB-RCS standard):
 - Easier to characterize and more reliable.
 - Reusable: 5 short slice lengths (20, 24, 28, 32, 36) to cover the 12 frame lengths (up to 864) of the standard.

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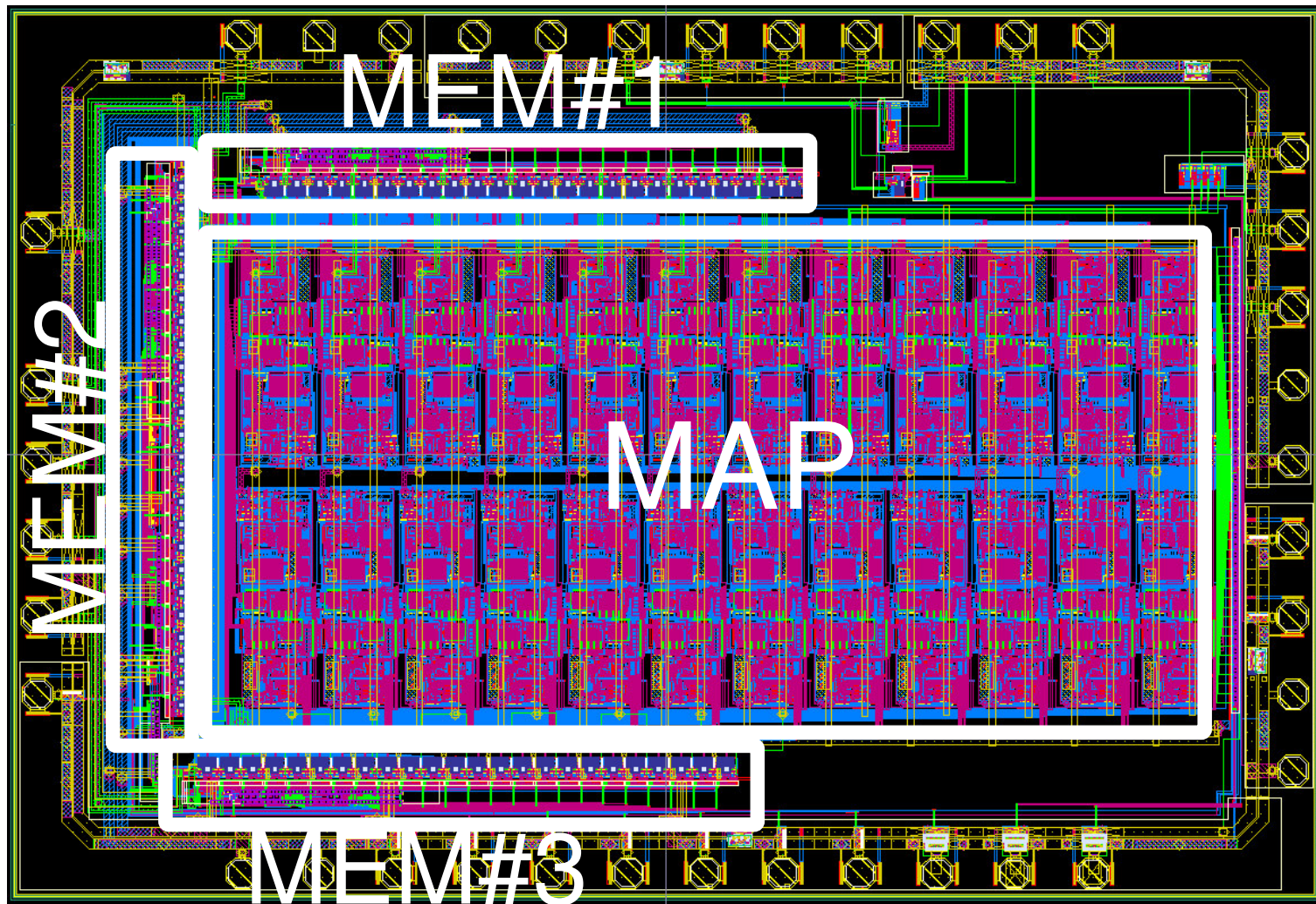


MAP decoder layout

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Philips QUBIC4: $0.25\mu m$ BiCMOS.

- MAP area: $3.03mm^2$ / with analogue S/Hs: $4.31mm^2$.

■ But...

- 24-symbol MAP decoder = 3mm^2
- 864-symbol turbo decoder $\approx 250\text{mm}^2$



- No industrial viability!??

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Semi-iterative analogue turbo decoder

■ Motivations

- **Conventional** analogue turbo decoder
 - 😞 **Area** grows dramatically with frame length.
 - 😞 A chip is dedicated to **one frame length**.
 - 😊 The **extrinsic information** can be more powerful than the path metrics to initialize the convergence process.

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■ Semi-iterative algorithm

Outline

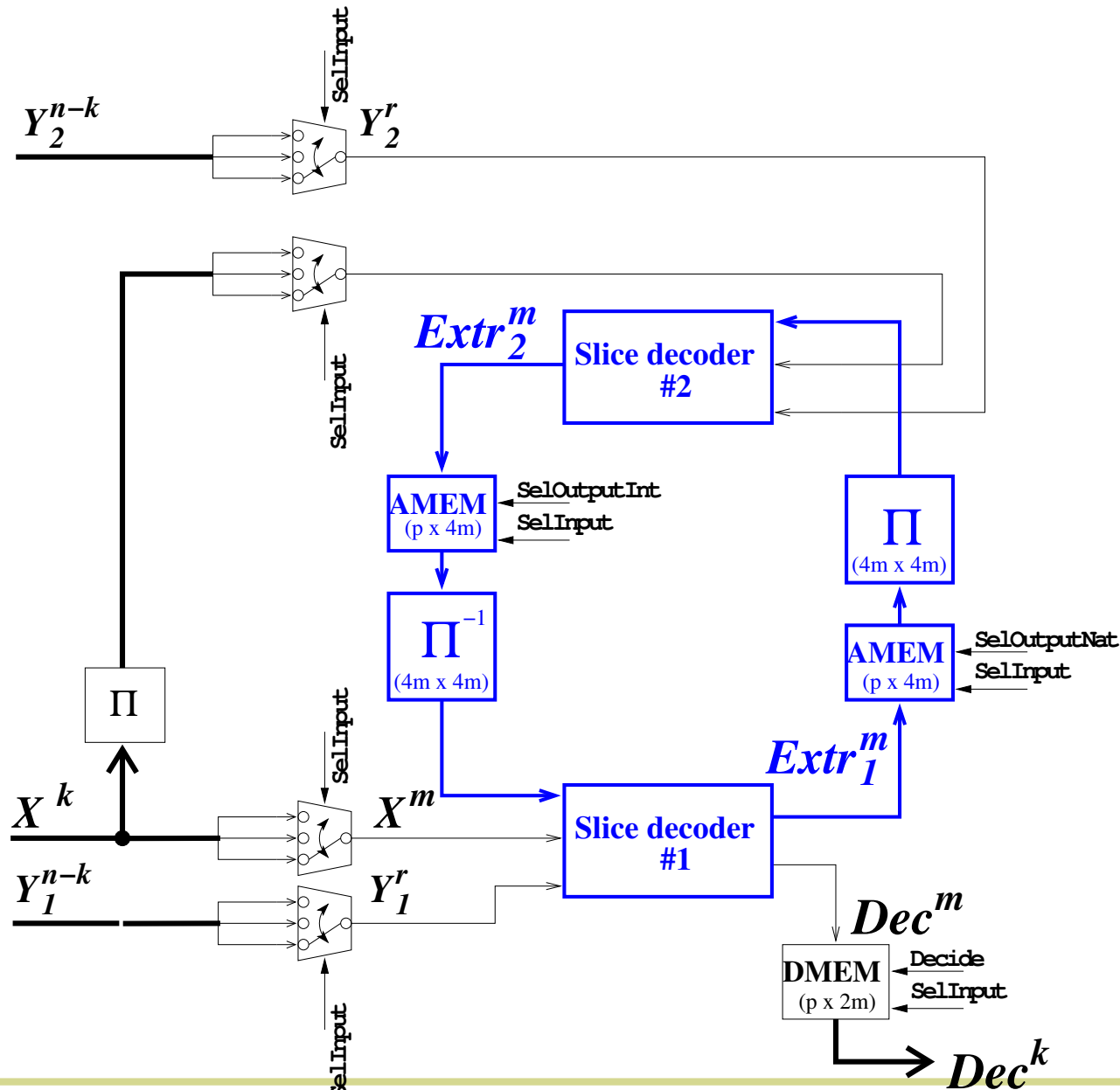
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How to reduce the area without breaking the
continuous exchange of **extrinsic**
information?

Semi-iterative architecture

Outline

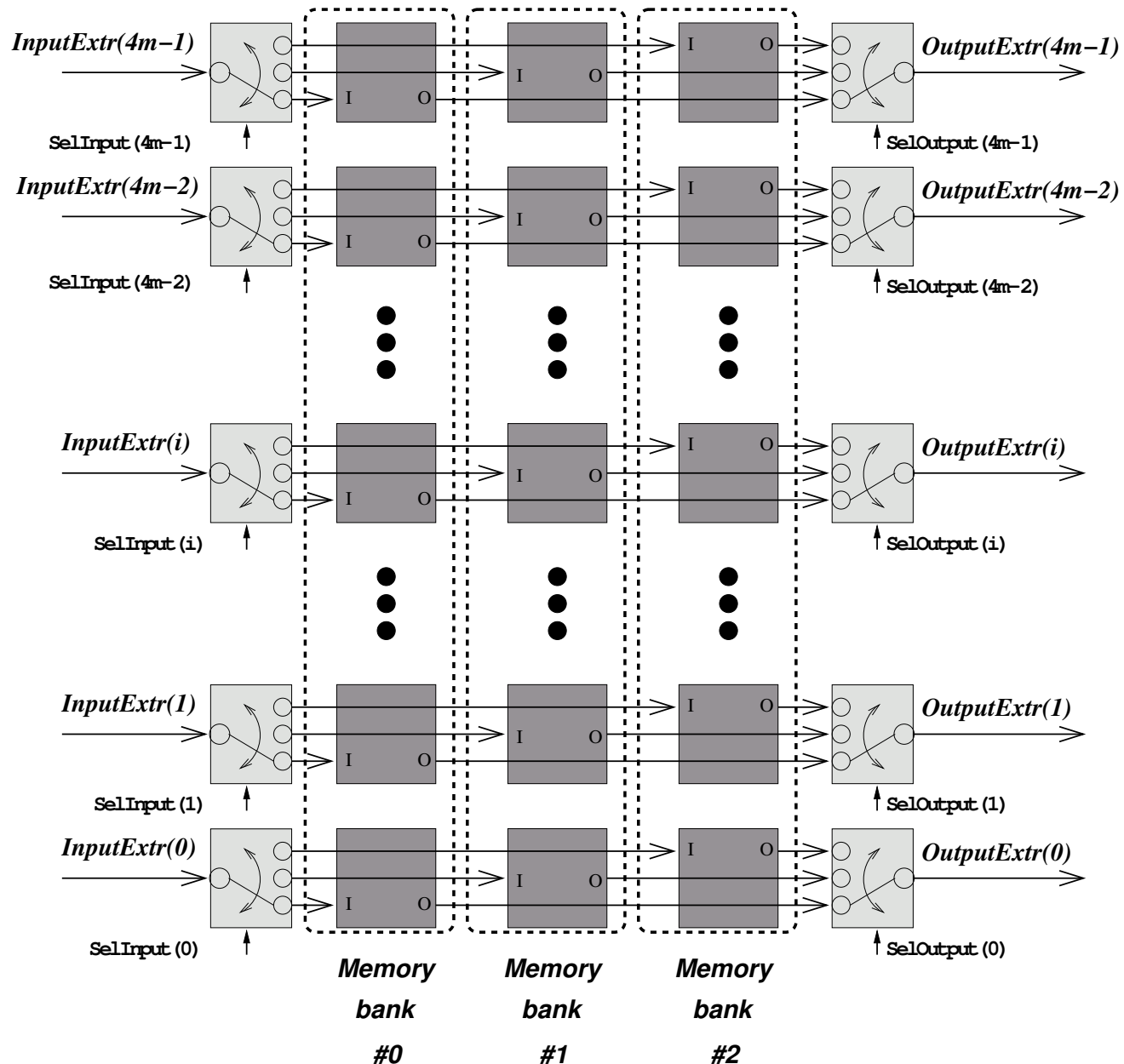
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■ Multiplexed analogue memories

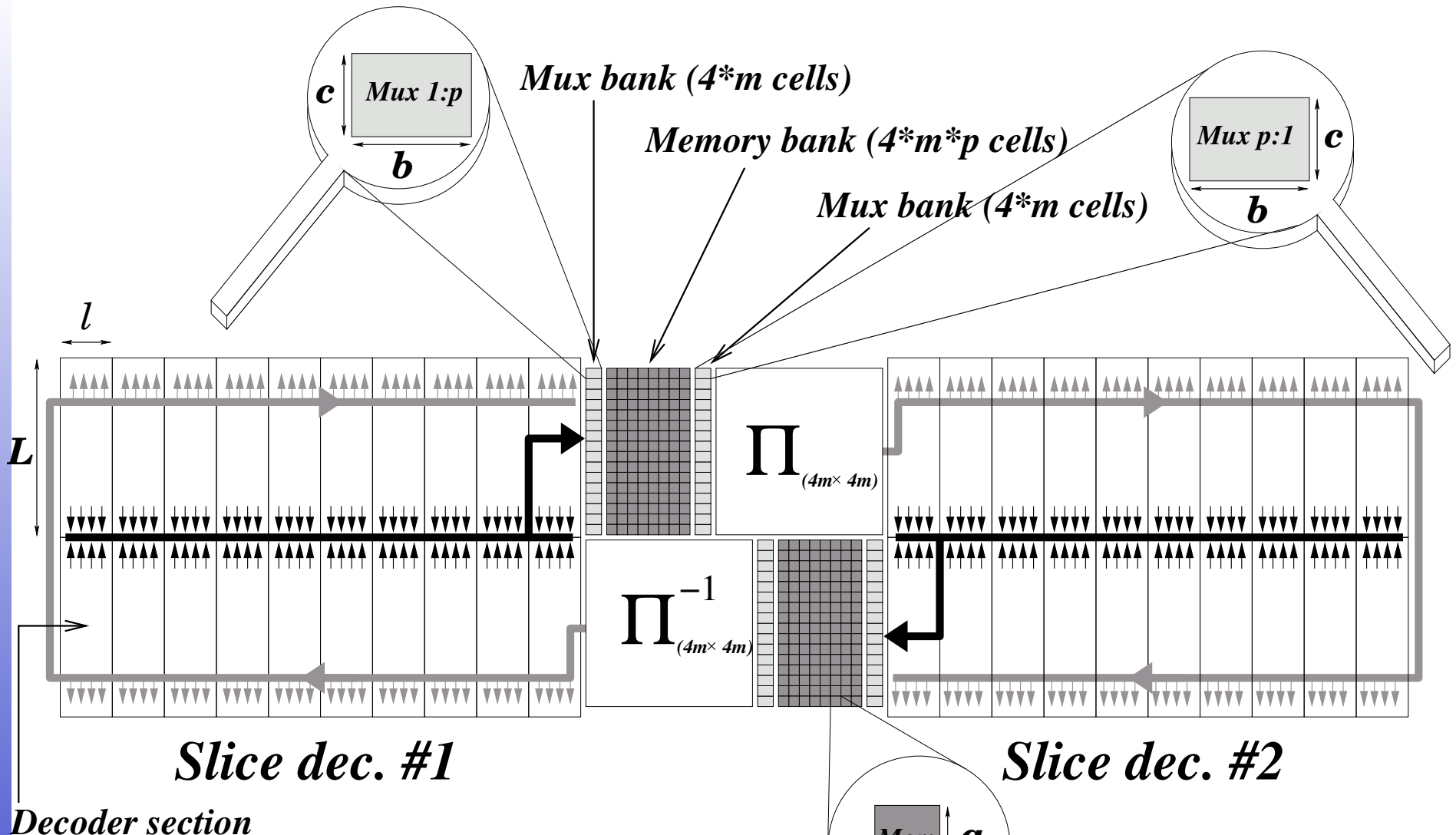
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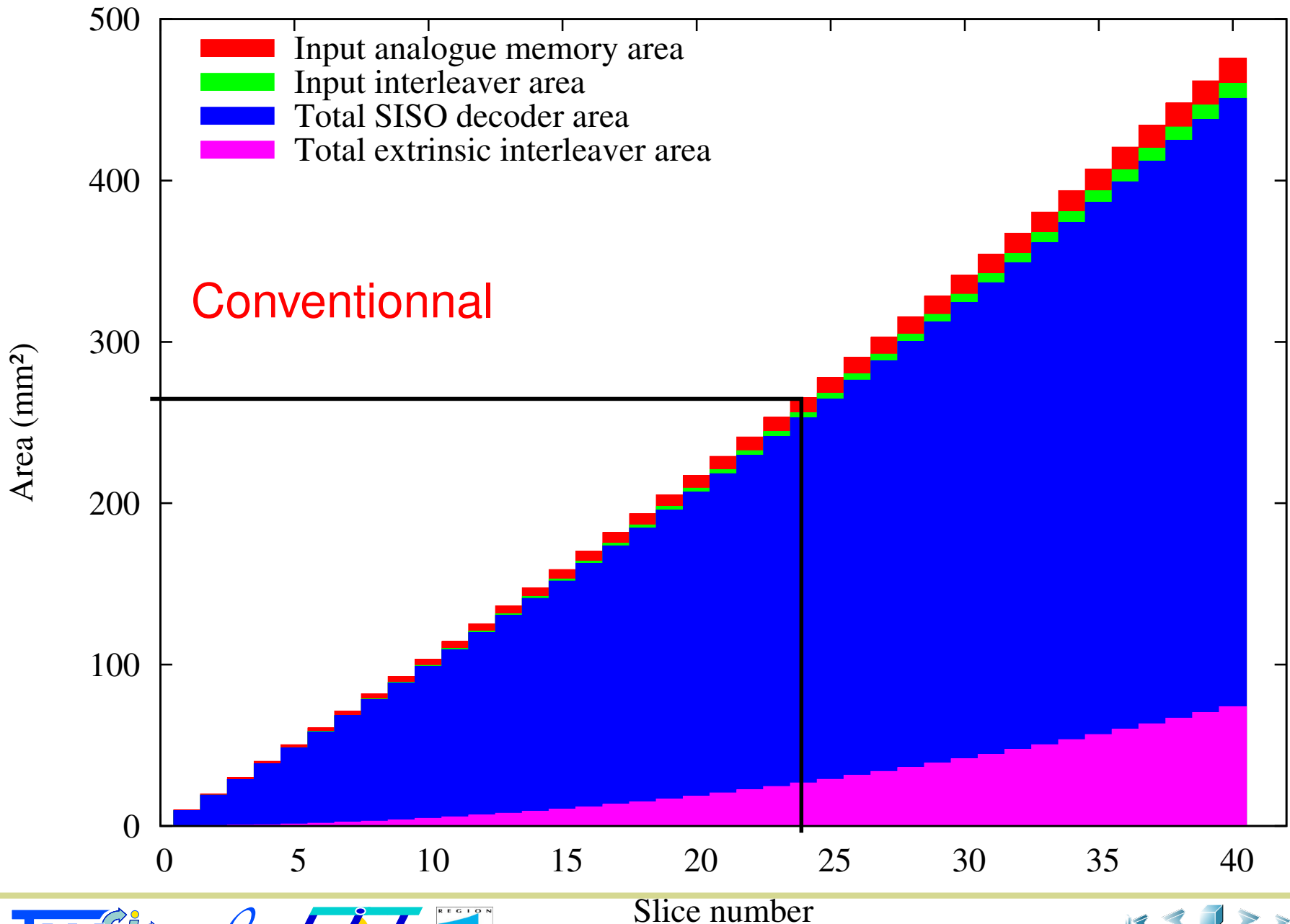
Geometrical considerations

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Semi-iterative turbo decoder area

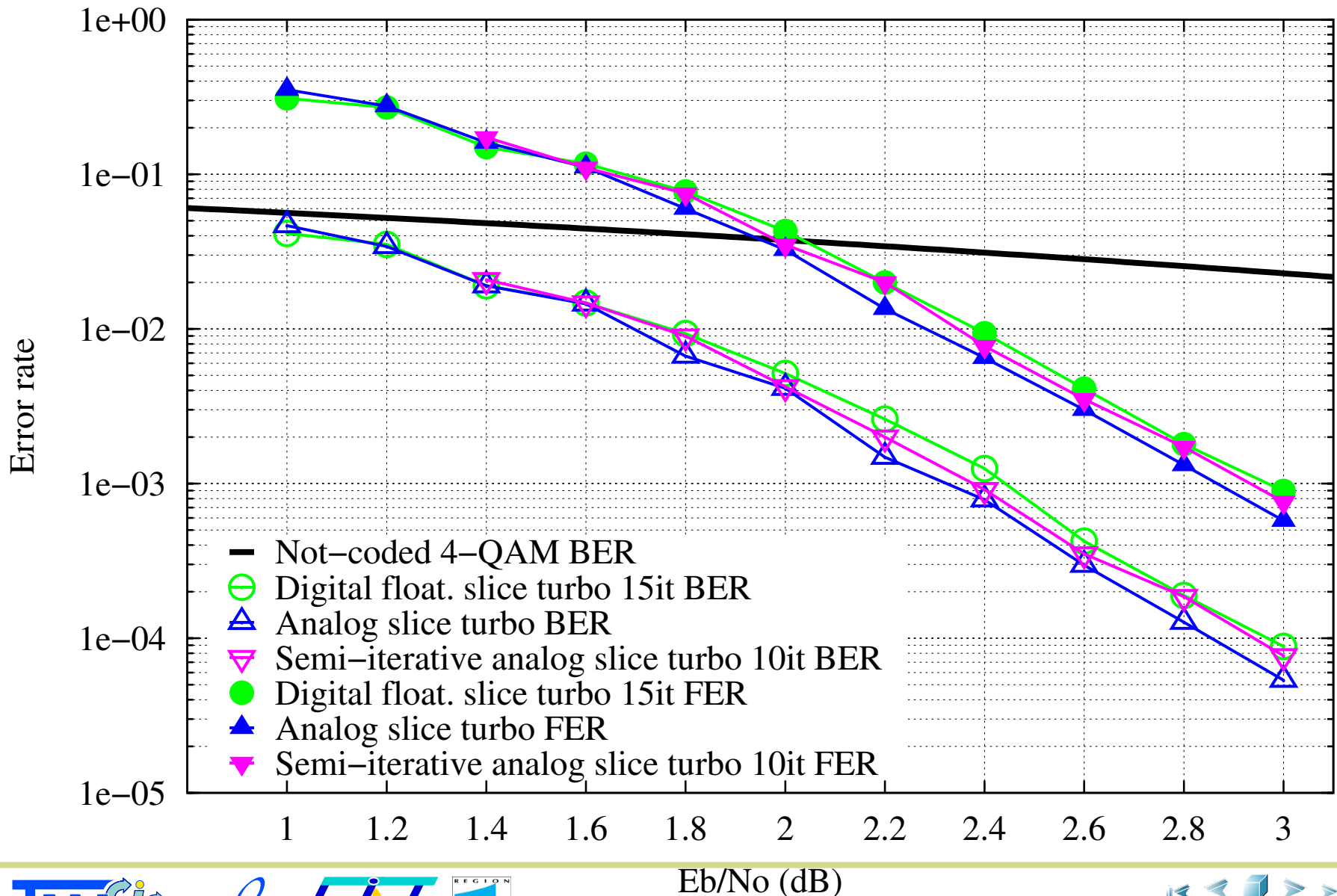
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Behavioural simulations

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Decoding of DVB-RCS frames (48 symbols, R=1/2)



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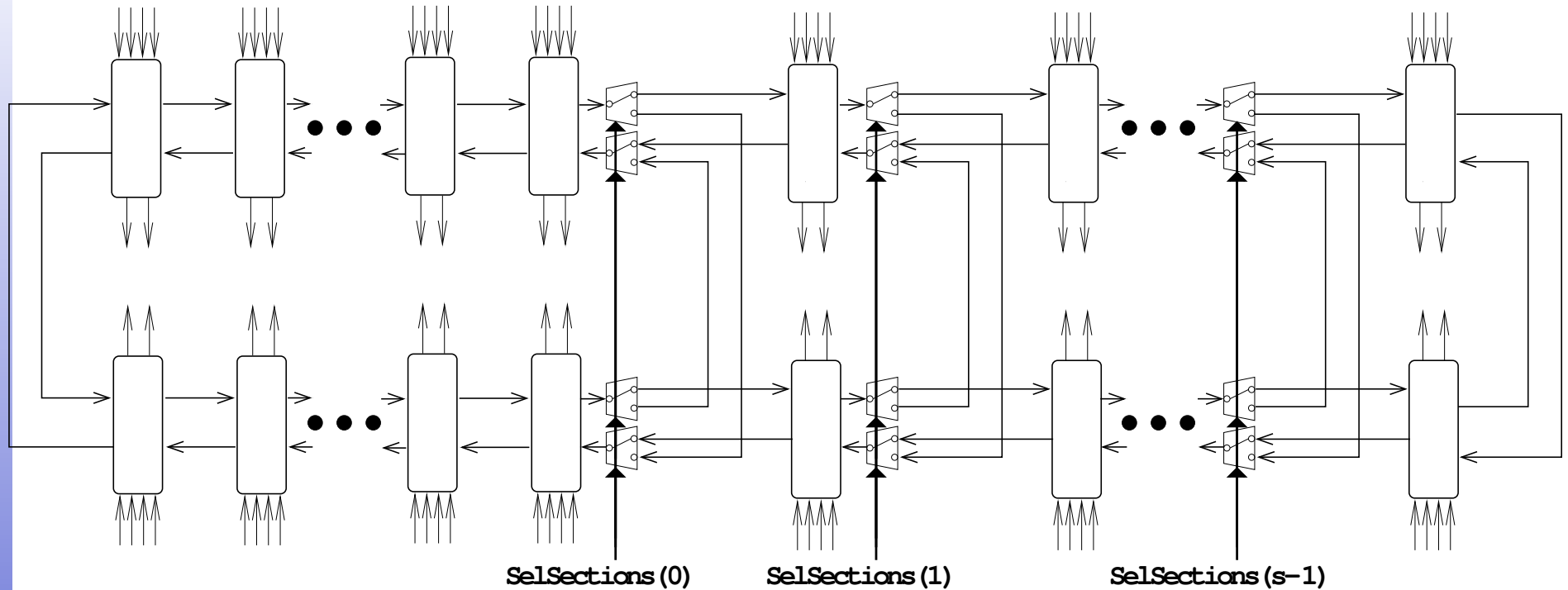
Reconfigurable semi-iterative turbo decoder

■ Reconfigurable MAP decoder

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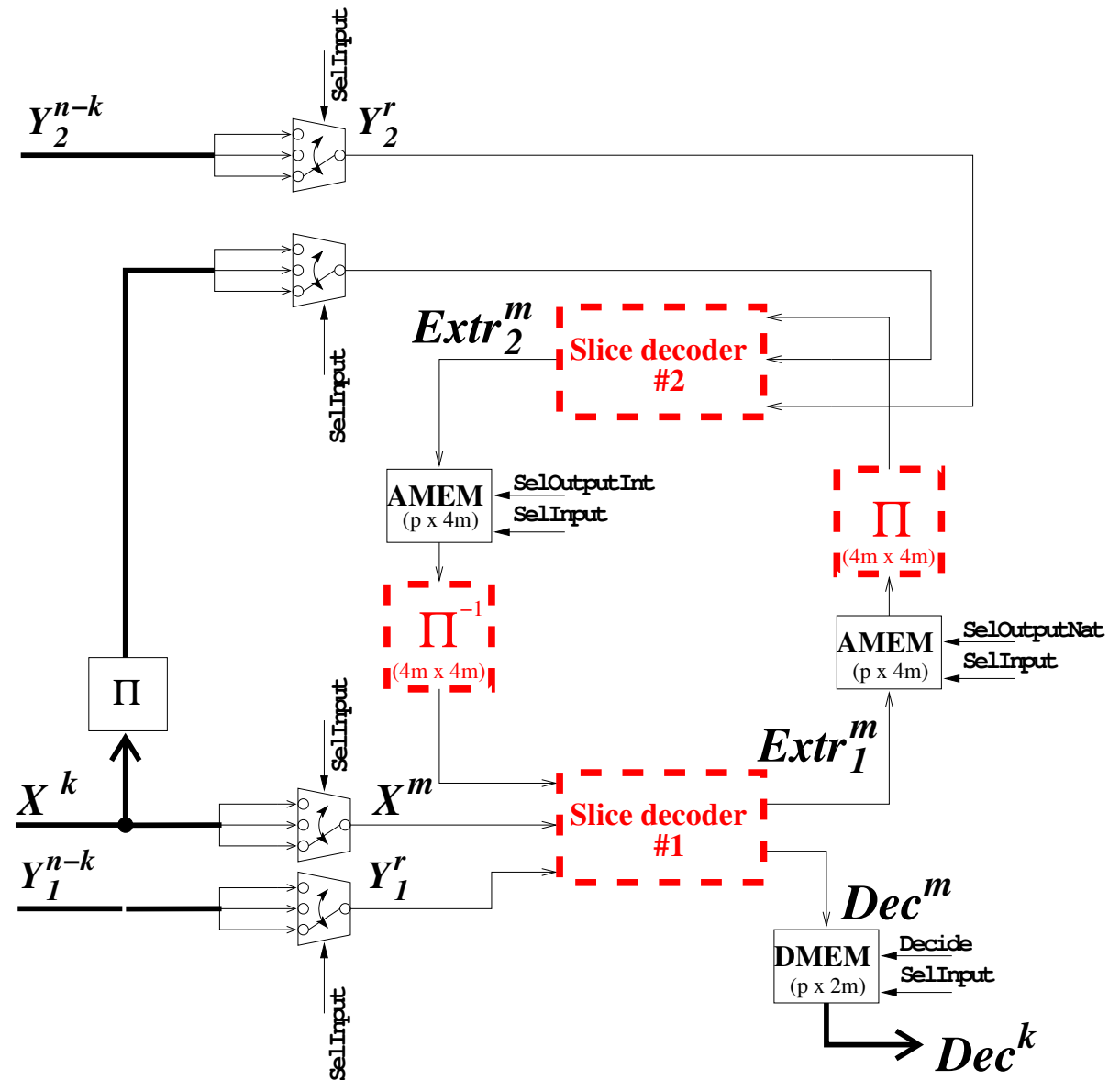
- Min slice length: 20 symbols.
- Max slice length: 38 symbols.
- Slice decoder area: 4.7mm².

Reconfigurable turbo decoder

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A reconfigurable MAP
 +
 A reconfigurable interleaver
 [Gaudet] P=19,
 Q=8
 =
 A single 25mm²
 chip for frames of
 40 up to 1824 bits!



■ Analogue vs. digital

- Multiple slice turbo decoder for DVB-RCS-like frames made up of 1824 bits (max).

	Analogue	Digital
Process	BiCMOS 0.25 μ m	CMOS 0.13 μ m
Data rate	1.5 GBits/s ?	100Mbits/s
On-chip area	25mm ²	2.7mm ²
SISO area	9.4mm ²	2.4mm ²
Mem area	9.4mm ²	0.3mm ²

- Our SISO decoder and analogue memories are not optimized at all: **room for improvement!**

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■ Conclusion

- Slicing technique
 - presents NO performance degradation,
 - enhances **reliability** and **reusability** of analogue elementary MAP decoders.
- **Semi-iterative** analogue turbo slice decoder
 - has an area divided by **10** when compared to a conventional analogue decoder,
 - enables the **continuous** exchange of extrinsic information,
 - requires an effort to design optimized analogue memories.
- A **single** 25mm² turbo circuit
 - can treat **all the frame lengths** of the DVB-RCS standard with **reconfigurable** MAP decoders and interleavers.

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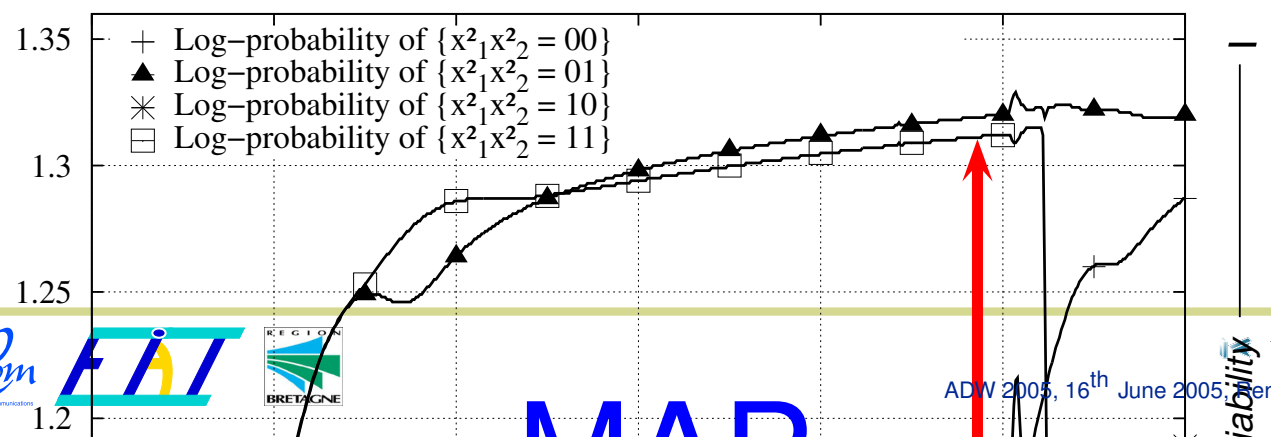
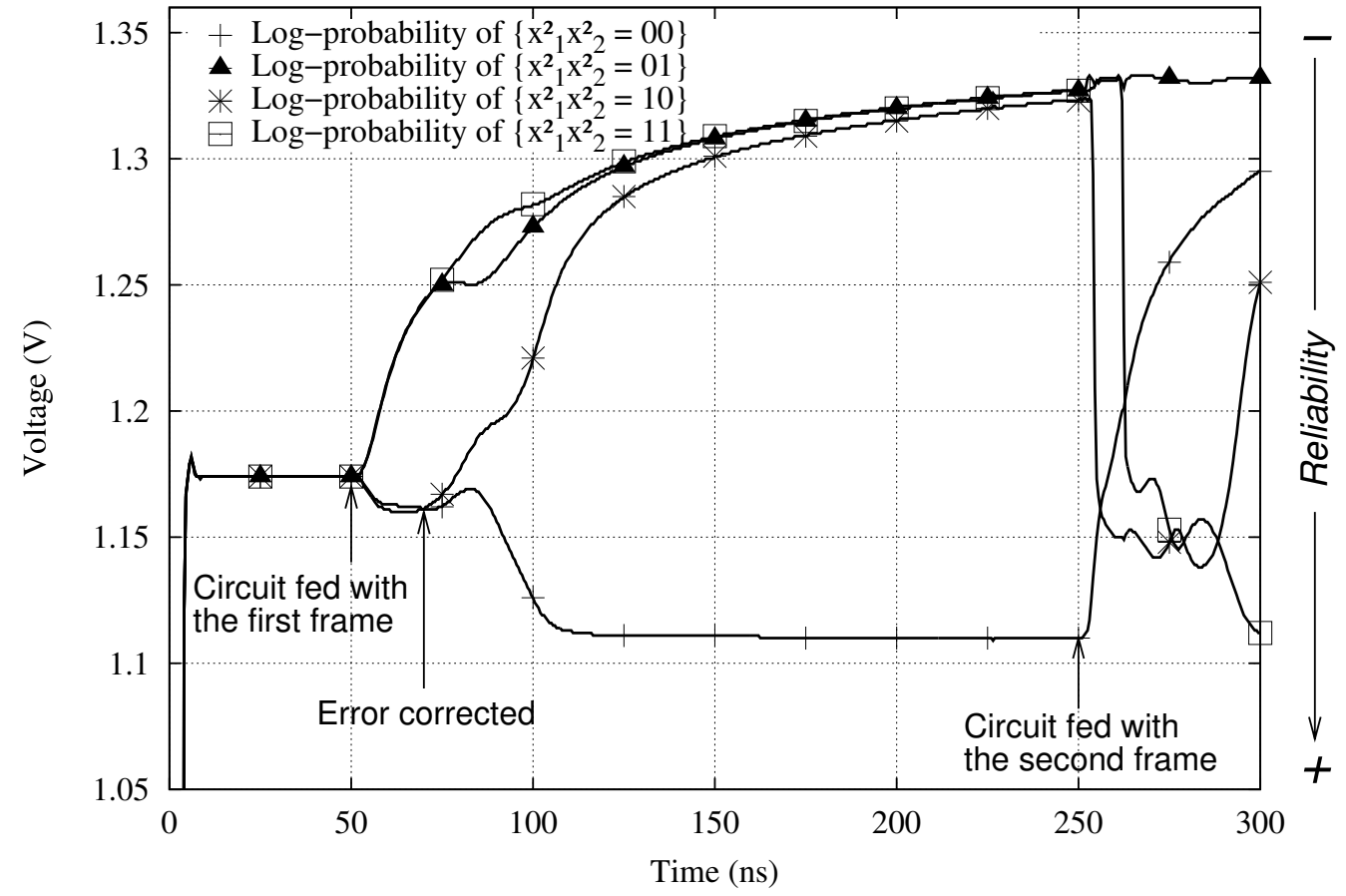
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Thanks for your attention.

Any questions?

Transistor-level simulation results

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Behavioural simulations

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