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Analogue Decoding of Duo-Binary Codes

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Abstract

This paper presents the design of an analogue decoder for convolutional duo-binary codes targeting an industrial application for the DVB-RCS standard. The decoder implements the MAP algorithm and is designed for a $0.25\mu m$ BiCMOS SiGe process. Simulations at transistor level validate the decoding of frames made up of 24 duo-binary symbols. Its power consumption per information bit and per state is simulated at $1.4mW$ which is comparable to what was obtained in a previous work for simpler and shorter codes. The decoding speed is estimated at 600Mbit/s. This elementary decoder is then used in a turbo scheme in order to implement the complete DVB-RCS decoder. Behavioural simulations show that the analogue MAP decoding enhances the error correcting performance by 0.1dB (at a BER of 10^{-4}) compared to its optimal digital equivalent.

1. INTRODUCTION

In telecommunication receivers many tasks which were performed by analogue circuits are now mostly being performed by digital ones. However, powerful error correcting techniques such as turbo decoding use continuous values which suggests that analogue circuits have yet to offer many advantages for such a type of integrated function. The first analogue solutions for this particular application were proposed by European laboratories [1–3] and were implemented using either BiCMOS or CMOS processes. These works have not only proved the validity of the concepts but have also shown significant gains in terms of speed, power consumption and silicon area over digital solutions [2–4]. However, none of the decoders presented in [2–4] were developed for an industrial application, only simple short codes were used. A first design for an industrial standard — the Universal Mobile Telecommunication System (UMTS) — is presented in [5]. This paper points out the fact that it is now crucial to apply the analogue technique to other standards to certify the industrial viability of analogue decoding. This is what this work aims to do. This article highlights the principles and results of the analogue decoding simulations of the duo-binary codes that were chosen for the recent standard Digital Video Broadcasting - Return Channel via Satellite (DVB-RCS) of the European Telecommunications Standard Institute (ETSI) [6]. In the first section, the principles of duo-binary convolutional codes are outlined. The BiCMOS design of an analogue decoder and simulation results are then presented. Finally, the design of a complete analogue DVB-RCS turbo decoder is raised.

2. PRINCIPLES AND ADVANTAGES OF DUO-BINARY CONVOLUTIONAL CODES

The DVB-RCS standard has adopted a duo-binary Convolutional Recursive Systematic Circular turbo code. This type of code does not treat bits individually but in couples. The elementary DVB-RCS convolutional encoder (Fig. 1) produces two parity bits for each duo-binary input symbol. A trellis section of

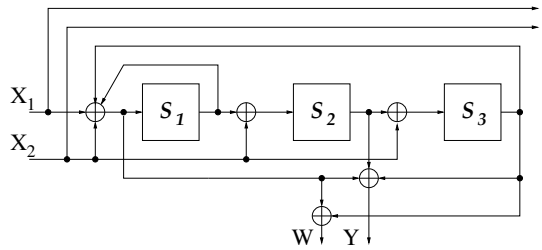

Figure 1: 8-state duo-binary encoder for DVB-RCS standard. Depending on the code rate, each two-bit symbol X_1X_2 is associated with either one or two redundant bits, Y and W.

this code is illustrated in Fig. 2. Compared to a trellis section of a binary code, the number of branches is doubled but the length is halved since a section treats a two-bit symbol rather than a one-bit symbol. Such

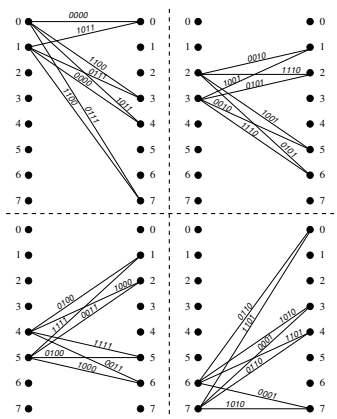

Figure 2: Trellis associated with the encoder of Fig. 1. The branches are labelled with the encoded symbol X_1X_2YW. Y and W are transmitted for a coding rate of 1/2 whereas only Y is used for a coding rate of 2/3 .

a code has major advantages compared to its binary counterparts. Berrou *et al.* [7] showed that the convergence of m-ary turbo codes is better but the gain is less noticeable for $m > 2$. Their minimal distances and their asymptotic gains are larger. They are also less sensitive to puncturing. These advantages make duo-binary turbo codes key candidates for many other telecommunications standards.

3. DESIGN OF AN ANALOGUE DECODER IN A BICMOS TECHNOLOGY

A convolutional circular binary code can be decoded with the Maximum A Posteriori (MAP) algorithm [8]. It uses only two mathematical operators (addition and multiplication) and two functions (logarithm and exponential). The last two are necessary for converting log-likelihood ratios (LLR) to probabilities and vice-versa. If X is a binary random variable and x its outcome, the LLR of X, $L(X)$, is defined by:

$$L(X) = \ln\left(\frac{P_X(x=1)}{P_X(x=0)}\right) \tag{1}$$

The exponential and the natural logarithm functions are readily available from a bipolar junction transistor (BJT) working in the forward active region. The collector current I_C depends on the base-emitter voltage V_{BE}:

$$I_C \approx I_S e^{\frac{V_{BE}}{V_T}} \tag{2}$$

where I_S is the saturation current and V_T is the thermal voltage. When diode connected, the BJT produces

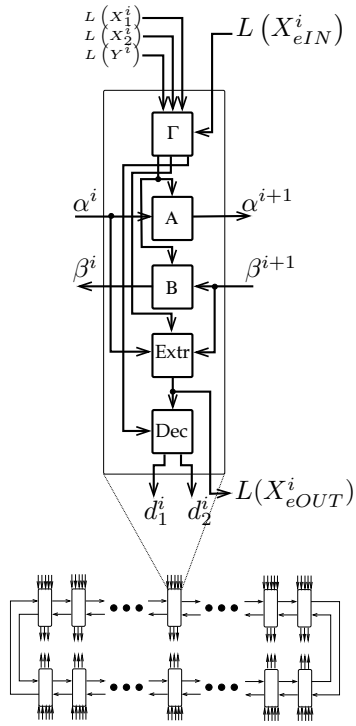

Figure 3: Analogue circular MAP decoder. Each section is made up of modules defined by the MAP algorithm. There are as many sections as symbols to decode.

a voltage V which depends on the current I flowing through it:

$$V \approx V_T \ln\left(\frac{I}{I_S}\right) \tag{3}$$

Associating a current with a probability and a voltage with an LLR, it is thus possible by using transistors and diodes to convert LLRs to probabilities, equation (2), and probabilities to LLRs, equation (3), respectively. This is a clear advantage of analogue decoders over digital decoders since currents, representing the probabilities, can be easily added and multiplied. Thus, the MAP algorithm can be implemented using a BJT-based analogue network [2]. The frame is decoded by letting this network converge to a stable state. The on-chip network is the direct mapping of the MAP algorithm. It is divided into as many sections as duo-binary symbols to be decoded (see Fig. 3).

Each section is built from four modules: a Γ module to compute the branch metrics, an A module for the forward metrics, a B module for the backward metrics and a *Dec* module to decide on the value of the duo-binary symbol. There are two sets of inputs to the section. The first set is the data produced by the

channel, $L(X_1^i)$ $L(X_2^i)$ $L(Y^i)$ $L(W^i)$, which are associated with the ith symbol $X_1^i X_2^i$ and its parity bits Y^i and W^i. The second set of inputs is composed of the forward and backward metrics α^i and β^{i+1} produced by the adjacent trellis sections. The outputs are the metrics α^{i+1} and β^i, fed to the adjacent sections, and the decisions $d_1^i d_2^i$ for the transmitted symbol $X_1^i X_2^i$. A fifth module is required if the MAP decoder is part of a turbo decoder: the *Extr* module. This module computes the extrinsic information $L(X_{eOUT}^i)$ which is then used by the Γ module of the second MAP decoder as the input $L(X_{eIN}^i)$. All the modules are connected in a voltage mode. Each module, except the *Dec* one, is divided into a computing BJT-based core and two MOS interface circuits. The BJT-based core is an analogue multiplier: the well-known Gilbert cell [2]. Designed for two differential inputs, this cell is adapted for treating binary symbols. However, it can be extended to m-ary symbols. The complexity of the extended structures grows geometrically with m. The A module is taken as an example to illustrate this growth in Fig. 4.

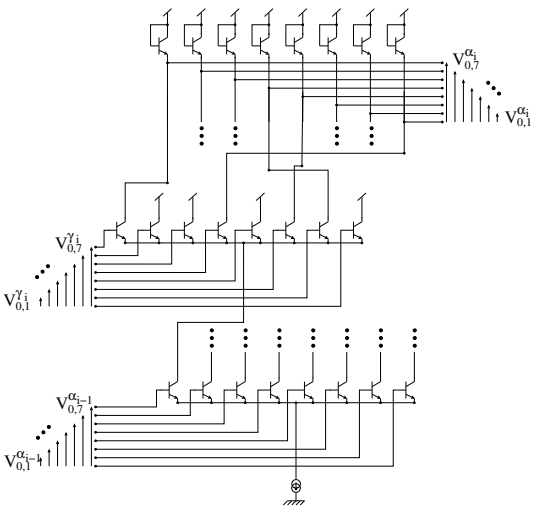

Figure 4: Extended Gilbert cell to compute the state metrics. The differential input voltages represent the LLRs.

Considering the duo-binary trellis section shown in Fig. 2, there are eight possible states per section. Let $\alpha_i(s)$ be the forward metric associated with a state s of the ith section. Let $\gamma_i(s', s)$ be the metric of the branch between a state s' of the ith section and a state s of the $(i+1)^{\text{th}}$ section of the trellis. Applying the MAP algorithm to a trellis of length k, the eight forward metrics of each section i between 0 and $k-1$ are computed using:

$$\alpha_{i+1}(s) = \sum_{s'=0}^{7} \alpha_i(s')\gamma_i(s', s) \tag{4}$$

For a duo-binary convolutional code of rate 2/3 with eight states (only one parity bit is produced per each quaternary symbol) the branch metrics can take eight values (16 for a code of rate 1/2 as illustrated in Fig. 2). The A module requires the design of an extended Gilbert structure with 8-ary inputs (Fig. 4). The bipolar transistors produce the product of probabilities, supplied by the LLR-voltages, and return the results as currents. Consequently, if the multiplication core requires only 6 transistors in the binary case, it uses 72 transistors in the 8-ary case.

4. RESULTS AND COMPARISONS

Running behavioural simulations using Simulink® validated an analogue MAP architecture for decoding frames of 24 duo-binary symbols. The encoding uses the DVB-RCS elementary convolutional code. The modelled decoder was then designed for a $0.25\mu m$ Philips SiGe process. Electrical simulations proved its ability to correct errors: frames altered by a gaussian noise were successfully decoded as predicted by behavioural simulations. Fig. 5 shows that the circuit's state converges to a solution and finally distinguishes the probabilities associated with the four possible values of a received duo-binary symbol. The lower the voltage, the higher the probability of the corresponding value. In this case, the hard decision at the channel output (not illustrated) is 10, which is an error, whereas the analogue decoder converges to the correct value 00.

The decoding capability was tested using several frames altered by a gaussian noise with different signal to noise ratios. The outputs were corrected and sampled after a minimal time of 80ns. This figure gives an estimated decoding speed of 600Mbit/s. Since the circuit is a direct mapping of the MAP trellis, the power consumption must be considered with respect to the length of the coding frame and the number of states of the code. The criterion to consider is the power per information bit and code state. From simulations, the proposed decoder consumes $1.4mW$ per information bit and code state. This result compares well with what was obtained with the decoder described in [2] which consumes $1.2mW$ per information bit and code state. This decoder treats frames of 16 binary symbols, among which eight are information bits (rate 1/2) coded on two states. The circuit presented in this paper decodes frames of 24 duo-binary information symbols coded on eight states, representing 72 bits. Fig. 4

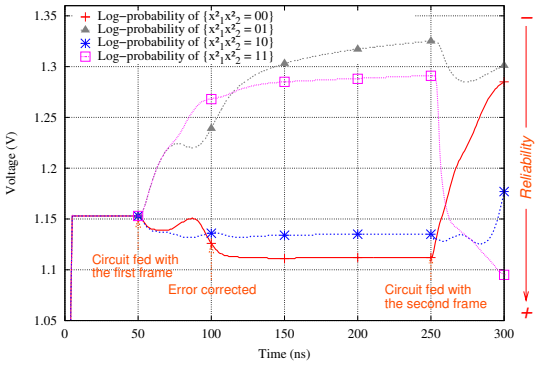

Figure 5: Correction of an error. The four voltages represent the four log-probabilities associated with the quaternary symbol. The lower the voltage, the higher the probability. As can be seen, at the beginning, it is not possible to distinguish which is the correct symbol since symbol 00 and 10 have the same probability.

shows that the complexity of the modules grows geometrically with the number of states, that is four times more than in [2]. It also shows that the complexity grows geometrically with the number of bits per symbol, that is twice as many as in [2]. However, the power consumptions per information bit and code state are similar. There are two reasons for this result. First, the bias current of the extended Gilbert cells does not grow proportionally to their size. Next, the duo-binary decoder needs only one parity bit per two information bits whereas the decoder in [2] uses one parity bit per information bit. As the decoder's need for power depends on the number of bits treated (whether they are: parity or information bits), implementing a code with a minimal rate reduces the power consumption per information bit. These results can also be compared to those obtained by the eight-state analogue turbo decoder presented in [5] which is designed for a CMOS process. [5] uses MOS transistors biased in the subthreshold region resulting in a low power consumption (21μW per information bit and state) at the expense of data throughput (only 2Mbit/s).

5. TOWARDS A TURBO DECODER FOR THE DVB-RCS STANDARD

A turbo decoder can be designed by reusing the described elementary MAP decoder in order to decode the smallest frame of the DVB-RCS standard (48 symbols). This complete turbo decoder was simulated using a high-level model. Fig. 6 shows that the analogue decoding has a gain of $0.1dB$, for a bit error rate of 10^{-4}, compared to an optimal digital version. The digital equivalent circuit uses floating point number representation and runs for 15 iterations, which provides maximum iterative performance. The analogue model performs better because it benefits from continuous time: there is no iteration but a permanent sharing of extrinsic information. The ability of the analogue decoder to use "soft" time enhances its error correcting performance.

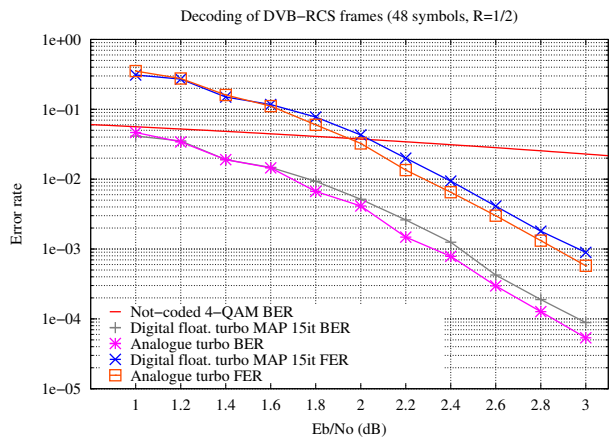

Figure 6: Bit and frame error rate curves for DVB-RCS frames of 48 duo-binary symbols. Optimal analogue and digital turbo decodings are compared on a channel with an additive white gaussian noise (AWGN).

6. CONCLUSION

An analogue MAP decoder for the DVB-RCS standard has been designed by extending the basic concepts of BiCMOS analogue decoding. As this standard is based on a duo-binary 8-state convolutional code, the extended Gilbert cells reach a complexity that had not yet been studied for a an analogue decoder. The decoding of 24 duo-binary symbols frames was simulated at a transistor level. It provides a sufficient accuracy to enable error correction. Moreover, the power consumption per information bit and per state is $1.4mW$ per information bit and state, which is similar to that of a reference circuit [2]. The decoding speed is estimated at 600Mbit/s.

The DVB-RCS decoder is a turbo decoder which was simulated at a behavioural level for the smallest frame length of the standard. The analogue decoding outperforms its digital counterpart by $0.1dB$ at a BER of 10^{-4}. This decoder benefits from the continuous exchange of extrinsic information for better convergence.

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