How to design brains on a chip
LUC LIBRALESSO (\textsuperscript{*,**}) - FLORIAN LARRAMENDY (*) - VINCENT JOST (**) - FRÉDÉRIC MAFFRAY (**) - THIBAULT HONEGGER (*

(*) Univ. Grenoble Alpes, CNRS, LTM, 38000 Grenoble, France
(**) Univ. Grenoble Alpes, CNRS, G-SCOP, 38000 Grenoble, France

CONTACT: luc.libralesso@grenoble-inp.fr

Typical workflow

I. NORMALIZED CHIP DESCRIPTION

![Brain diagram]
source: [1] One of several brain patterns we want to reproduce (basal ganglia loop)

II. TRANSITIONAL PROCESS

- Cortex
- Striatum
- Thalamus
- GPe

Extract graph structure. Each node has a number of neurons, each connection has a connectivity degree, and a maximal width

Final microfluidic chip, that represents the brain part

III. GENERATION OF CAO FILES

Goals

- Chip design is very complex, until now, designs were made by hand
- This work aims to use mathematical and computer tools to automate this process

Why a computer approach ?

Too much constraints and possibilities to be handled by a human
- Lots of choices to make:
  - Chamber positions
  - Lots of possible planar embeddings of a 3D structure
  - Channel dimensions (width, length, height)
  - Channel routing
- Microfluidic constraints:
  - Navier-stokes equations.
  \[
  \Delta z = \frac{\eta Q}{\rho g} \left( \frac{L_{ch} L_{ch}}{W_{ch} H_{in}} + \frac{L_{in} L_{out}}{W_{in} H_{out}} \right)
  \]
- Fabrication constraints:
  - Two chambers should be not too close
- Neural-engineering constraints:
  - Channel width and length related to their brain equivalent
  - Each node contains a specific number of neurons

Work done so far

- Formal representation of chip requirements and chip designs
- Semi-automatic chip design from specifications
- Already done on several practical cases:
  - Basal ganglia loop (5 nodes)
  - Several toy models (2 to 4 nodes)

Perspectives

- Continue to implement brains models
- Study algorithms to optimize chamber placement
- Implement heuristics to route channels automatically

Chip Architecture

Bibliography