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Passive component development in LTCC

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***Abstract*— Passive components integrated in Low Temperature Co-fired Ceramics (LTCC) are of interest for highly integrated microwave and millimeter-wave modules. Metal Insulator Metal and Interdigital capacitors as well as spiral inductors with a maximum surface of 1 mm × 1 mm were designed, fabricated and tested using the ESL41060 tape material. Capacitive and inductive values, the Self Resonance Frequency and the Q-value for these items were found.**

Keywords—LTCC; inductor; capacitor; Self Resonance Frequency (SRF); Q-value

I. Introduction

LTCC is an excellent multilayer platform for system in package designs. In order to integrate active components such as Microwave Monolithic Integrated Circuits (MMICs) or Radio Frequency Integrated Circuits (RFICs) in any module, a biasing network is needed to provide the DC-feed voltages to the chip pads. Most often, one or several shunt capacitors are needed to sink any frequency containing signal to the ground, while letting the DC pass between the voltage source and the chip. On-chip shunt capacitors are often small in value (~1pF to 3 pF) and therefore higher pF capacitors are needed outside the MMIC (to be followed by even larger capacitors further away in the feed network). In some cases, choke inductors are added in the feed line network, acting alone or together with the shunt capacitor, as a low pass filter, to disconnect the RF signal, present on the MMIC, from the voltage source. These two components are not easy to realize in the LTCC when it comes to the values required for the bias network: the higher the inductance and capacitance, the lower the cut-off frequency, which improves the intended protection. A high capacitor value is hard to reach since most LTCC tape providers offer tapes with a relative permittivity of around 6 to 7, which is not enough in this case eliciting the need for a High relative permittivity material. A high inductance value is also difficult to achieve since it takes up a sizeable surface. However, a multilayer inductor design can improve this aspect.

In addition to the capacitive or inductive value, the Self Resonance Frequency (SRF) and the Q-value are also important factors for the designer. Once the SRF is reached, the capacitive component starts presenting inductive properties and vice versa. Thus a low SRF limits the use of the component at higher frequencies. A high-Q component is advantageous given that it has less inherent resistance making it closer to the ideal component, be it an inductor or a capacitor. A Q-factor of 80 was presented for capacitors realized in LTCC and Q-factors of LTCC-based inductors close to 100 were presented in [1], [2] and [3].

In this work a group of first year students at IMT Atlantique were asked to design capacitors and inductors taking up less than 1 mm × 1 mm of real estate surface. The objective was to design 1 pF and 10 pF capacitors and 2 to 5 nH inductors with the given space constraint and material at hand, while also trying to maximize the SRF and the Q-value. Even though primarily intended for DC-feed circuitry, they can also be used for other purposes.

II. LTCC materials, stack_up and design rules

The LTCC material used in this work is the ESL41060 from ElectroScience Laboratories. According to the manufacturer, its relative permittivity is 16 to 19 for frequencies ranging from 0 to 19 GHz. The advantage of this material, compared to ESL41110 and ESL41020 with relative permittivity around 4 and 7 respectively, is that it generates a higher capacitor value for the same surface in use. In this work, full plane tapes of ESL41060 were used, however inserts of this material could also be employed should another lower relative permittivity tape be chosen for the main package.

A prototype substrate containing all devices was designed on a six layer stack; though the test devices were realized using the three top layers only. The choice of a total of six layers is to provide mechanical stability. All metallization was done using gold pastes from ElectroScience Laboratories; ESL802 to fill the metallized vias and ESL803 for the conductor layers. The fugitive tape ESL49000 was used as sacrificial material to produce the openings in one or two layers in order to access the probe pads.

The LTCC stack-up is presented in Fig. 1., below. Details of the produced components are given in the following paragraphs. All the designs were made using design equations in combination with ADS momentum and CST Microwave studio simulations.

To respect our in-house LTCC process design rules, the minimal line width/gap size was set at 100 µm /100 µm, with the exception being the RF probe pads where a 50 µm gap size was allowed. The viaholes' diameter is 150 µm and the landing pads have a 250 µm diameter.

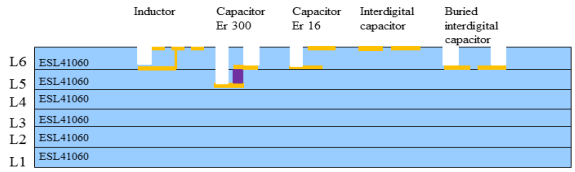

Fig. 1. LTCC stack up. The three top layers (denoted L4, L5 and L6) are used to realize the components.

III. RF PROBE PAD DESIGN

In order to measure scattering parameters of the designed components, two RF probe sets are realized, one for the full two-port scattering parameters and one grounded version, Fig. 2.. The RF pad is designed for a 200 µm Ground Signal Ground (GSG) probe pitch. It is made up of a coplanar waveguide line where the two ground lines are separated to go around the component under test to connect to the counterpart. These RF pads can be placed on any layer as long as cavities are created in all above tape layers to allow for measurements to take place. The designed component is inserted into the RF probe sets and connected to the central lines.

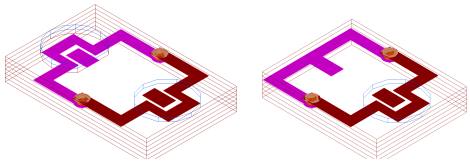

Fig. 2. RF probe sets to plug in the designed components; two port version (left) and grounded version (right). The RF pads could be placed on any two layers, be it the same or different ones. Here they are placed on layer 4 (pink) and layer 5 (red). If on different layers, connection is assured by metallized vias.

The design of a calibration kit to properly de-embed the effect of the RF probe set on the capacitors and inductors is deemed difficult since the ground lines are more or less close to the inserted component depending on its size and geometrical shape. Thus, coupling between the RF probe set and the components would differ and the de-embedding would be erroneous. This is why it was chosen to compare measured and simulated S-parameters for the complete structure and when deemed good enough, simulated parameters of the component only is used to establish the components parameters.

IV. CAPACITORS

A. Metal Insulator Metal (MIM) capacitors

Metal insulator metal capacitors are made up of a dielectric material with metal top and bottom electrodes. The DC value of the capacitor is calculated by

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}$$

where the capacitor value is C, A denotes the area, ε_0 is the permittivity of air and ε_r denotes the relative permittivity and d is the distance between the two electrodes. Thus, a large area, high relative permittivity and a thin dielectric layer is beneficial for increased capacitor value.

1) 1 pF MIM capacitors

As a reference design, a square MIM capacitor was designed with 0.81 mm × 0.81 mm electrodes, using the ESL41060 tape and one layer dielectric thickness, i.e. the electrode distance is 75 µm after firing. According to (1), this configuration should result in a 1 pF capacitor. This capacitor was realized across the top layer (L6), i.e. the top electrode is screen printed on the last layer of the LTCC stack (L6) and the bottom electrode is screen printed on the second to last layer (L5). An opening is made in the top layer to access the probe pad, as can be seen in Fig. 3.. The same capacitor value was given for a circular electrode design where the diameter of the circular electrodes is 0.90 mm.

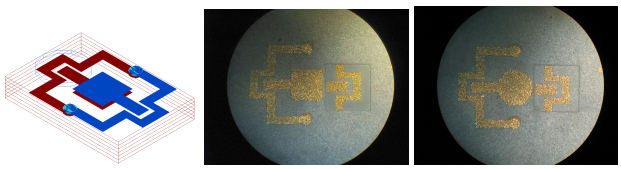

Fig. 3. The 1 pF design. 3D layout of two port configuration for RF measurement (left, where red is layer 5 metal and blue is layer 6 metal), two port RF versions of the prototypes with square (middle) and circular electrodes (right).

Measurements of these capacitors were done using a 40 GHz Vector Network Analyzer from Anritsu and GSG probes model 40A from Picoprobe. Fig. 4. shows the comparison of measured and simulated scattering parameters for the squared capacitor, its capacitive value and Self Resonance Frequency (SRF).

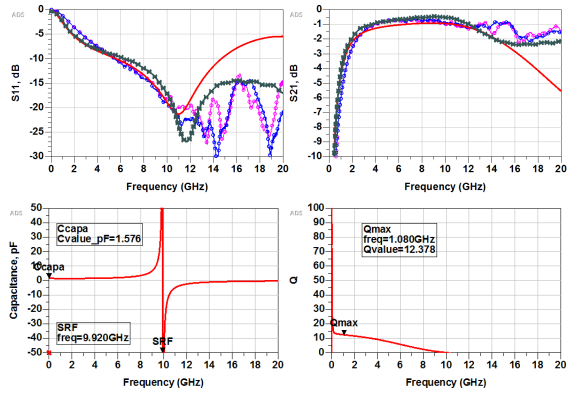

Fig. 4. Comparison between measurements and simulations of the scattering parameters of the two port RF squared capacitor design (top) and simulated capacitive value and calculated SRF (bottom, left) and simulated Q-value (bottom right).

As can be seen there is a quite good agreement between the simulations and the measurements at the lower end of the frequency spectra. Momentum, being a 2.5D simulator does not take into account the difference in material on the same layer which makes it consider the openings for the RF-probes as being filled with the LTCC dielectric. Above 14 GHz CST seems to better represent the measured results.

The capacitors were found to have 1.54 pF and 1.37 pF capacitance and a SRF of 9.93 and 8.41 GHz for the squared and circular versions respectively. The Q-value was found to be 12 for the two capacitors at 1 GHz and declined with the

frequency. The Q-value is determined by the ratio of the imaginary to the real part of the input impedance obtained from a one-port model simulated data.

2) 10 pF MIM capacitors

A square and circular capacitor where the dielectric LTCC tape was replaced by high-K dielectric paste, ESL4117, was also tested in this work. According to the manufacturer, ESL4117 has a relative permittivity of 270 to 300. The capacitors were created using the following scheme; Via and alignment holes were cut out with a Nd-YAG laser, via fill was performed on layer 5. The bottom electrode and the associated RF probe pad were screen printed on layer 4, the top probe pad was screen printed on layer 5 and the top electrode was screen printed on the bottom side of layer 6 (to be overlapped with the high-K dielectric and parts of the probe pad on layer 5 to assure the electrical contact). After screen printing the opening where the high-K paste and RF measurement pad were to be placed, openings were created in layers 5 and 6 to allow access to the probe pads. Thereafter, the stacking was executed with fugitive tape placed in the RF probe pad cavities, and high-K dielectric was dispensed in the MIM cavity before the top layer was stacked. This was followed by lamination and sintering according to standard procedure given by the tape supplier.

Measurement of these capacitors and fitting to simulation data showed a rather low capacitive value of 1 pF instead of the intended 10 pF.

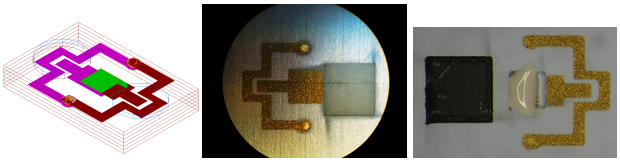

Fig. 5. The 10 pF design. 3D layout of two port configuration with square electrodes for RF measurement (left where pink color is layer 4 metal, red layer is layer 5 metal, green is metal printed on the bottom side of layer 6), laser cut out MIM cavity after screen printing (middle) and layer five during stacking with fugitive tape to protect the left RF pad and dielectric paste filled in the opening of the two port RF version (right).

Several factors could have contributed to these unexpected results; one of these is the non-control of the thickness of the dielectric paste. The MIM cavity was manually filled using a dispenser needle while the lamination step was expected to equalize the height of the paste with that of the tape. A better way to do this would have been to screen print the dielectric paste onto the layer 5 electrode. Moreover, ESL4117 is meant for thick film processing on alumina substrate and not intended to be used in an LTCC procedure. Even though this capacitor failed, the fabrication procedure and the design of openings to access the probe pads one or two layers down gave us useful experience for further work.

B. *Interdigital capacitors (IDC)*

Interdigital capacitors can be easily obtained on a single layer with screen printing. In this work, an interdigital capacitor on the top layer was designed to give 1 pF capacitance from design equations [4] and from electromagnetic simulations. To obtain 1 pF, the required surface of 1 mm² was too small; a surface twice as large was needed for the top layer IDC, see Fig. 6.. The same layout was also reproduced as a buried version on layer 5 to see the impact of having a homogenous dielectric environment on all sides of the capacitor. The buried IDC should theoretically have a higher capacitance.

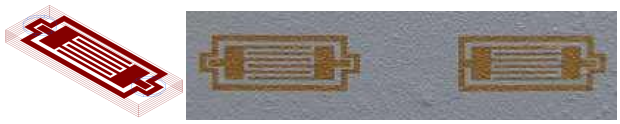

Fig. 6. Interdigital capacitor. 3D layout, buried version (left with red layer 5 metal), top layer prototypes (right) two port version and grounded RF version.

The IDC number of fingers, n, is 6, the finger width, w, is 100 µm, the gap between fingers, g, is 100 µm and the overlapping finger length, L, is chosen to be 2 mm. The top layer IDC proved to have a 1.28 pF capacitance, while the buried one had 2.21 pF which was close to the expected values. The SRF of these components is very low; just about 3.74 GHz for the top layer IDC and 2.92 GHz for the buried one, while the Q-values are 12 for the top layer IDC and 11 for the buried version at 1 GHz.

V. Inductors

In a feed network, a series acts as an RF choke that prevents the RF-signal from the MMIC to be transmitted to the voltage supply. A spiral inductor takes up rather large real estate if it is designed on one layer with a bonding, air bridge or metallized via to take out the signal from the center of the spiral. In this prototype work, different designs were realized on the top two layers. The design equations were taken from [5]. As in the case of the capacitors, electromagnetic simulations were used together with analytical expressions to dimension the inductors.

A. *Screen printed spiral inductor*

The square spiral inductor is presented in Fig. 6. The measured S-parameters for the DUT and associated electromagnetic simulations are presented in Fig. 8. as well as the simulated SRF and Q-value for this inductor. Here, both momentum and CST simulations agree quite well with the measured results. The RF probe pads are both placed on the top layer which seems to be better for momentum.

This circular inductor was found to have a 3.5 nH inductance while the expected value was 4.9 nH according to the design equations. The inductance has a simulated SRF of 6.9 GHz, a Q-value of 31 at 1 GHz with a maximum Q-value of 35 at 1.6 GHz. The discrepancy between the theoretical and the simulated inductance can partly be caused by the fact that the design equations do not include the via/bonding/air-bridge that is needed to connect to the center of the inductor. In addition, this inductor has an quarter of a square winding connected between the external via hole and the GSG central line which is clockwise while the rest of the winding is counter clockwise.

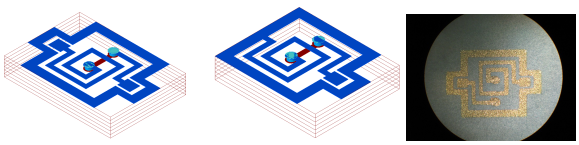

Fig. 7. Square spiral inductor. 3D layouts with two port RF version left and grounded RF version middle (where blue is layer 6 metal and red is layer 5 metal) and two port RF version prototype (right) .

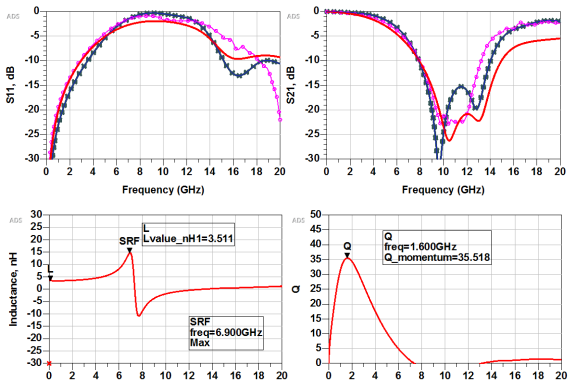

Fig. 8. Measured and simulated scattering parameters for the complete DUT two port RF version inductance (top), Simulated parameters (bottom) of which we have the SRF (left) and Q-value (right) for the square spiral inductor. The S11 and S21 traces are as follows: pink circles for measurement results, red line for Momentum simulation and grey crosses for CST simulation.

Furthermore, the given design equations are, to our understanding, provided for inductors having a ground-plane layer underneath them which is not the situation here.

B. Wire bonded spiral inductor

The wire bonded inductor is basically the same design as the squared one presented above. Replacing the 100 µm wide lines with gold wire bonds of 25 µm in diameter, as is shown in Fig. 9., increases the inductance to 5.1 nH as compared to the screen printed version, Fig. 7..

The SRF remains unchanged at 6.9 GHz while the Q is 26 at 1 GHz and a maximum Q of 30 reached at 1.7 GHz.

The wire bonded version gives a higher inductance which is normal since the wire diameter is only 25 µm as compared to the 100 µm wide screen printed trace. However, the fabrication time and cost are naturally higher for the wire bonded version.

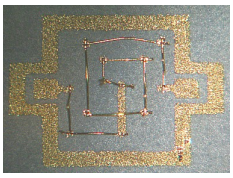

Fig. 9. Wire bonded square spiral inductor prototype with two RF ports.

CONCLUSIONS AND FURTHER WORK

Different circuit topologies such as capacitors and inductors in LTCC were studied. Square and circular MIM capacitors and IDC capacitors on the top or internal tape level were fabricated, as well as a square spiral inductor on the top layer and a wire bonded top layer version of the same design. Their SRF and Q-value was established from simulation. The capacitor values were higher than the expected design values, while the inductor values were lower than those of the design equations. The Q-values are rather low while the SRFs in general are better when comparing with other LTCC based passive devices.

This work will be followed by a more thorough program to design inductors and capacitors on multiple internal layers in the LTCC structure. The capacitance and inductance per square millimeter need to be further increased to allow for a more efficient system in package design.

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