Development of plasma etching processes to pattern sub-15 nm features with PS-b-PMMA block copolymer masks: Application to advanced CMOS technology

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The best strategies to transfer nanoholes formed from the self-assembly of Polystyren/Polymethylmethacrylate (PS/PMMA) based block copolymers into a silicon substrate are investigated. The authors show that specific issues are associated with the plasma etching of materials through the PS masks obtained from self-assembly. Indeed, due to the nanometric size of sub-15 nm contact holes and to their inherently high aspect ratio (>5), plasma etching processes typically used to etch SiO_2 and silicon in the microelectronic industry must be revisited. In particular, processes where the etching anisotropy relies on the formation of passivation layer on the feature's sidewalls are not adapted to nanometric dimensions because these layers tend to fill the holes leading to etch stop issues. At the same time, the ion bombarding energy must be increased as compared to a typical process to overcome differential charging effects in high aspect-ratio nanoholes. However, by developing appropriate processes—such as synchronized pulsed plasmas—the authors show that it is possible to etch 70 nm deep holes into silicon by using block copolymers and a hard mask strategy. Another interesting observation resulting from these experiments is that for sub-15 nm holes, a critical dimension (CD)-dispersion of few nm leads to strong aspect ratio dependent etch rates. In addition, a careful analysis of the dispersion of the holes' CD after each plasma steps shows that the CD control is far from satisfying advanced CMOS technology requirements. A critical issue comes from the uncompleted PMMA removal from the PS/PMMA matrix during our self-assembly process: variable amount of PMMA remains in the PS holes, leading to microloading effects during the etching steps, which in turn generates CD-control loss. This problem perhaps can be solved by combining UV exposure to acetic acid treatment to provide PS masks free of PMMA residues before plasma etching.
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I. INTRODUCTION

Directed self-assembly (DSA) of block copolymers (BCP) stands out as a promising alternative to overcome conventional lithography[1] limitations, i.e., sub-40 nm resolution with line width roughness below 2 nm. This low-cost method was successfully applied to the contact hole patterning in 22 nm static random access memory (SRAM) devices,[2] the shrink of contact holes' critical dimensions (CDs)[3] or the fabrication of silicon FET.[4] Furthermore, recent results suggest that Polystyren-*b*-Polymethylmethacrylate (PS-*b*-PMMA)—one of the most widely studied BCPs chemistry—has an intrinsic low line edge roughness (LER),[5,6] which is a serious advantage for the fabrication of integrated circuits (IC) compared to 193 nm-lithography features. It also has been shown that ultimate resolution of such BCP is sub-10 nm for both line array and holes.[3]

However, for applications in the microelectronic industry, a tremendous challenge must be overcome: the CD of the etched structures must be controlled at 10% of the targeted dimension,[7] i.e., about 1 nm for 10 nm block copolymer features (holes or lines). Practically, the CD control obtained on a 300 mm diameter wafer by combining typical 193 nm-lithography and state-of-the-art plasma etching technologies is about 2 nm, remaining far from international technology roadmap for semiconductors requirements despite constant improvements. However, CD control with polystyrene-based BCP is expected to be complicated due to both their poor etch resistance as compared to the substrate's one and the neutralization layer removal prior to pattern transfer with the PS-mask template. Indeed the typical thickness of BCP mask is only 30 nm and the etching selectivity between PS and the underlying layer is an issue. It is thus typically difficult to transfer directly the BCP mask into the silicon:[8] a multimask patterning strategy is required for accurate critical dimension control. By using adequate hard-mask stacks and H_2 postetch annealing of substrate, BCP-based DSA has been shown to give access to a sub-2 nm CD control and a LER of 1.5 nm.[9]

In this paper, we will focus on contact holes and discuss the best strategy to pattern silicon with BCP in the view of their integration into IC circuits.

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II. EXPERIMENT

PS-*b*-PMMA and PS-*r*-PMMA copolymers were synthesized by Arkema, under the tradename Nanostrength EO®. The materials were used as received. PS-*b*-PMMA and PS-*r*-PMMA powders were dissolved in propylene glycol monomethyl ether acetate (PGMEA) to obtain 1–2 wt. % solutions. The PS-*r*-PMMA solution was spin-coated on 3 × 3 cm silicon (100) pieces at 700 rpm to obtain thin films of ∼90 nm thickness and then annealed at 230 °C for 10 min to ensure the chemical grafting. Afterwards, the substrate was thoroughly washed in PGMEA to remove the ungrafted materials. PS-*b*-PMMA solutions were spin-coated on the top of the PS-*r*-PMMA brush layer and annealed on a hot-plate at elevated temperature for few minutes to allow the self-assembly process to take place, leading to PMMA cylinders in a PS matrix. Samples with different polymer film thicknesses were generated depending of the processing parameters such as spin-coating speed and initial solutions concentration. In a last step the PMMA domains were selectively reconstructed by dipping the samples in glacial acetic acid for few minutes. The 3 × 3 cm samples are stuck on the wafer by Kapton™ tape with a thin film of Fomblin™ oil between them to ensure a good thermalisation of the samples.

The typical stack used to transfer the PS nanoholes into a silicon substrate by plasma etching is shown in Fig. 1. It consists of: PS features (60 nm thick)/random copolymer grafted layer (∼a few nanometers)/10 nm thick PECVD SiO_2 hard mask/silicon substrate. However, we have also investigated the possibility of using the BCP template to pattern a dual hard mask [silicon anti-reflective coating/amorphous carbon (Si-ARC/a-C)] that is typically used to etch materials in the microelectronic industry[3] instead of the single SiO_2 hard mask. The a-C organic mask is a thick PECVD carbon-based layer and the (Si-ARC) is a thin spin coated silicon containing polymer. The Si-ARC layer acts as an antireflective coating during photolithography and is also used to transfer the resist patterns into the organic mask. The development of the etching processes (random copolymer removal, hard mask opening and silicon etching) are performed in an industrial etcher (DPS™ from Applied Materials (AMAT) for 200 mm diameter wafers) that has been described elsewhere.[7,10–14] The DPS is an inductively coupled high density plasma source (ICP) where both the source antennae and the bottom electrode are powered. The inductive source consists of a ceramic dome with a rf three dimensional coil wrapped around it. The bottom electrode is powered trough a capacitive coupling at a slightly higher frequency (13.56 MHz) than the source (12.56 MHz). The source power (W_s) controls the ion flux to the wafer (and the reactive radicals densities), while the bottom power (W_b) controls the ion energy at the wafer level. The lower electrode is a monopolar electrostatic chuck (ESC) and the wafer is kept at 50 °C by circulating He at 8 Torr between the ESC and the wafer, which allows to maintain the wafer at 50 °C (i.e., the ESC temperature). The Al_2O_3 chamber wall temperature is maintained at 80 °C by a heat exchanger while the ceramic dome is air-cooled when the plasma is on, and is heated by lamps when the chamber is idle, providing a constant temperature of 60 °C. Process reproducibility is ensured by using typical cleaning/conditioning strategy of the reactor walls between each experiment.[15–17] Additional experiments in pulsed plasmas[18] have been carried out in another ICP reactor from AMAT: a DPS advantage™ in which both power supplies can be pulsed synchronously.[18,19] This reactor, designed for the etching of 300 mm diameter wafers, has been described extensively elsewhere.[20–25]

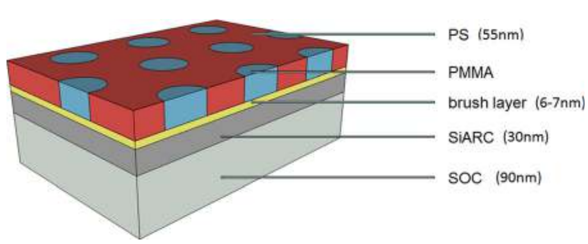

FIG. 1. (Color online) Stack to be etched after block copolymer lithography.

Both reactors are connected under vacuum to a quasi-*in situ* XPS analyzer, which can be used for sample chemical composition measurement. Those systems have been described elsewhere.[26,27] Finally, the surface roughness of the sample is analyzed by *ex situ* AFM measurements (see Martin and Cunge for details[11]).

III. RESULTS AND DISCUSSION

We have developed and optimized the etch processes to transfer the PS features from PS-*b*-PMMA BCPs into Si taking advantage of the relatively thick PS layer (∼60 nm) that is resulting from our specific self-assembly process. Indeed, the PS thickness is usually about 30 nm in most of the previous studies reported in the literature, making the pattern transfer step into silicon very challenging.[28] With our integration scheme, the PS mask is close to twice thicker, which reduces the selectivity requirement during the etching of the random polymer layer and of the hard mask. In the following, we discuss one by one the etching steps that are needed to etch silicon with a SiO_2 hard mask (patterned with the PS holes template). The transfer of the PS mask into the dual hard mask SiARC/a-C and silicon etching through this mask are discussed later at the end of this paper.

A. Samples characterization before plasma etching

Prior the transfer of PS nanoholes into the substrate by plasma etching, the PMMA domains in the BCP mask must be removed. This can be done by dry etching, taking advantage of the large difference in dry-etch resistance between O-containing polymer and aromatic polymer.[29] Ar/O_2 plasma seems to be the best choice for PMMA removal in terms of surface roughness and etch selectivity to the underlying material.[30] However, the O_2-based plasma etches the PS both vertically and laterally (due to spontaneous etching reactions between O radicals and PS on the contact holes sidewalls), leading to selectivity issues in the subsequent etching steps and to an increase of the PS holes diameter. Therefore, the removal of the PMMA domain is preferentially achieved by deep UV exposure of the sample (degradation of PMMA domain and PS cross-linking) followed by a wet acetic acid treatment.[31,32] Alternatively, it has been reported that acetic acid treatment on PS-*b*-PMMA without preliminary UV exposure drawn the PMMA chains to the film surface, leaving opened pores in the film.[33] This so-called[34] "surface reconstruction" approach has been used in the present work.

Figure 2 shows the AFM measurements performed on our PS-*b*-PMMA thin film before and after the acetic acid treatment. Figure 2(a) shows that before the acetic acid bath, the difference between the PS and PMMA domains is clearly visible by phase imaging. By contrast, the phase image in Fig. 2(b) shows that after the acetic acid treatment the surface of the sample does not exhibit a well-defined structure anymore. At the same time, the topographical images show that the surface roughness considerably increases after the acetic acid bath. This is attributed to the migration of the PMMA chains to the surface during the acetic acid bath: the surface is now partially covered by PMMA chains (probably chemically modified by the acetic acid). This conclusion is supported by the XPS analysis of the C1s peak that is shown in Fig. 2(c). This figure shows that the contribution to the C1s peak at 289.1 eV, (which is attributed to C=O bond environment in PMMA material) is much higher after the acetic acid bath than before. The amount of PMMA at the near surface (the depth probed by XPS is <10 nm) has

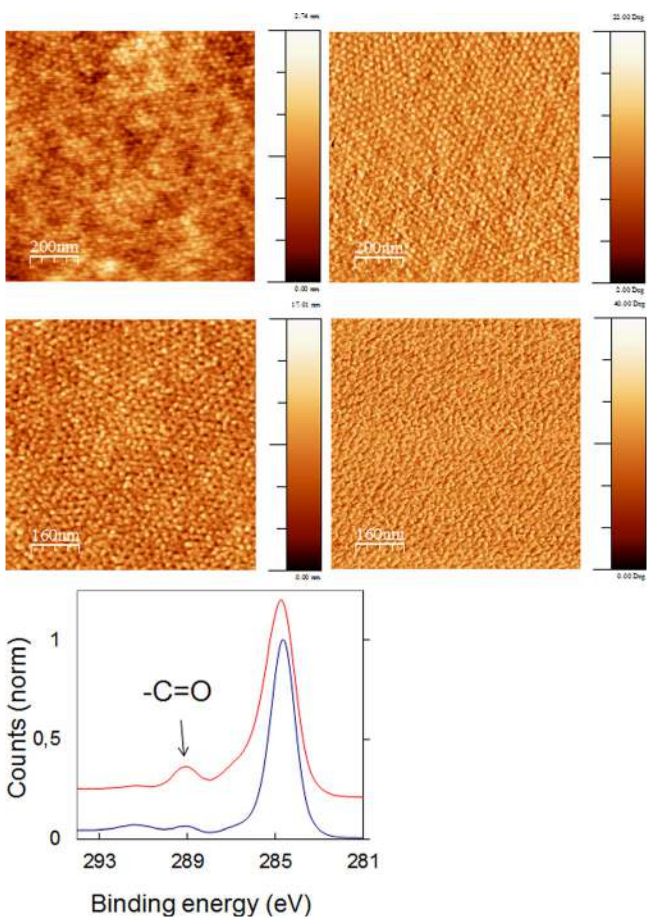

FIG. 2. (Color online) AFM measurements for (a) the original PS-*b*-PMMA copolymer and (b) after swelling with acetic acid and drying. (c) Corresponding C1s XPS measurement: a larger amount of PMMA (C=O peak) is detected after acetic acid treatment (spectra are offset in intensity for clarity).

increased from 20% before the acetic bath to 55% after, which is clearly indicating that the surface of the sample is now partially covered by PMMA.

From this observation, we can conclude that the etching processes that are used to transfer the PS-mask template into the underlayers will first need to etch the PMMA chains at the top of the surface to reveal the PS-mask template. As discussed below, this can be an issue in terms of critical dimension control.

B. Etching the random PS-*r*-PMMA neutralization layer and removing PMMA residues

Prior to the etching of the SiO_2 hard mask through the PS holes, it is necessary to remove the PMMA chains from the PS surface and then to etch the ca. 7 nm-thick-PS-*r*-PMMA-neutralizing layer at the bottom of the PS holes (i.e., on top of the SiO_2 layer, see Fig. 1). This is achieved by a single plasma step in Ar/O_2 chemistry. Since the O atoms in O_2-containing plasmas tend to etch laterally the PS mask, we have used a heavily diluted gas mixture [gas flow rate ratio Ar/O_2 (10:1)]. At the same time the ICP source rf power is kept low (220 W) to minimize the gas fragmentation and thus the O atoms density, leading to lateral etching of the contact hole's sidewalls. Finally, to minimize the PS-mask consumption we use a low RF bias power (10 W) to minimize the ion-bombardment energy. This value gives the best compromise between the PMMA and random-layer-etch rates, the PS-mask faceting, and PS consumption.

Figure 3 shows SEM top views of the samples before and after the PS-*r*-PMMA-layer removal in the Ar/O_2 plasma (PS-PMMA was treated before with acetic acid).

Figure 3(a) shows that after the acetic acid treatment an important percentage of the holes are not "opened" (a rough estimate indicates that around 30%–35% of the total amount of holes have sub-4 nm diameters right after acetic acid bath), i.e., they are still covered by PMMA chains which have migrated to the surface, as discussed before. We underline that PMMA degrades rapidly under the SEMs electron beam and therefore the amount of PMMA remaining at the surface in Fig. 3(a) is largely underestimated compared to the sample before SEM exposure (as observed by AFM in Fig. 2). However, this figure shows another important point: before any plasma treatment holes diameter range from 6 to 14 nm. With our block–copolymer system, we expected a regular 13 nm-hole diameter after PMMA removal. Therefore, we first concluded that not only are PMMA residues left at the surface on top of the contact holes but also that some PMMA is remaining inside a minority of the holes after the acetic acid treatment thus reducing the hole diameter. In addition to that, we conclude that the amount of PMMA residues varies significantly from hole to hole. Therefore, the acetic acid treatment alone is not efficient enough to fully extract the PMMA chains from all the contact holes and bring them to the surface. We shall see below that this is a serious issue for CD control during the subsequent plasma etching steps.

Figure 3(b) shows that after the 7 s-long Ar/O_2 plasma the PS contact holes are now fully opened. After the process, the holes average diameter is larger and tends toward its

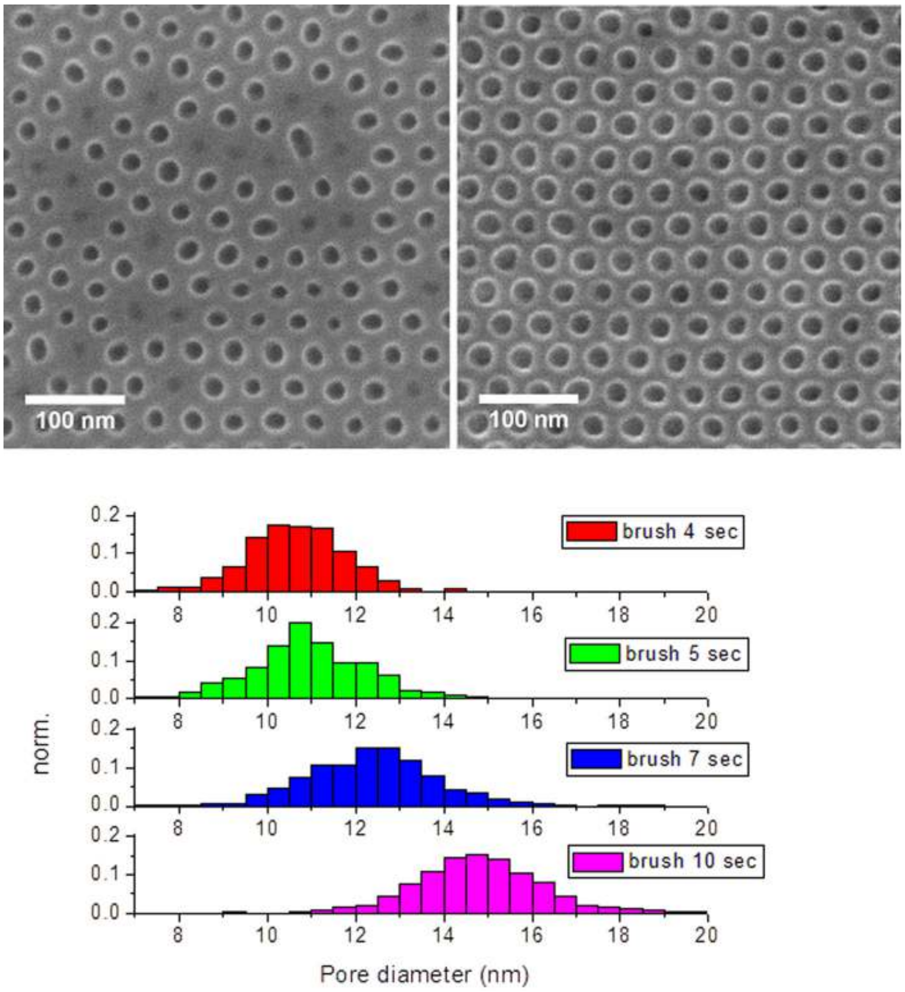

FIG. 3. (Color online) SEM top view of the PS-*b*-PMMA surface (a) before and (b) after PS-*r*-PMMA-layer removal by the Ar/O_2 plasma. (c) Evolution of the pore diameter distribution as a function of the Ar/O_2 plasma time (statistics done from 300 up to 500 different contact holes).

expected value of 13 nm, which suggests that the short Ar/O_2 plasma step has efficiently cleared the PMMA chains both from the surface and from inside the PS holes.

At the same time, this plasma step is also used to etch the random PS-*r*-PMMA layer and its duration must be chosen accordingly. However, we underline that the holes diameter is increasing during this process due to isotropic etching by O atoms. As an evidence, Fig. 3(c) shows the hole-diameter histogram (deduced from the SEM pictures) as a function of the O_2-based plasma duration. The hole diameter increases during the process, which can be attributed first to the etching of the residual PMMA from the PS-feature sidewalls (thus revealing the real PS hole template) and then to the isotropic etching of PS sidewalls by O atoms. The PS isotropic etch rate is expected to be less than PMMAs one but is still significant and the hole diameter continue to increase after the complete PMMA removal. However, since the amount of PMMA that is initially present in the holes fluctuates from one hole to another, this step has dramatic consequences on the CD control of the process. As a matter of fact, if PMMA has been fully removed from some contact holes, those contact holes are etched laterally by O atoms as soon as the plasma is ignited, leading to an immediate CD gain above 13 nm. By contrast, for a hole that is partially filled by PMMA, the O atoms will first be consumed by PMMA etching reactions and the lateral etching of the PS holes will be delayed as compared to a PMMA-free contact hole. This situation in which some contact holes are PMMA-free and others are filled by PMMA generates a microloading effect during the O_2/Ar plasma. The consequence of this microloading[35] effect is that the dispersion of the hole diameter [the FWHM of the histogram in Fig. 3(c)] is increasing continuously with time, reaching more than 3.5 nm after 7 s of plasma. This CD dispersion is a significant issue considering the fact that the control over the CD of the holes should be better than 10% of the targeted CD, i.e., <2 nm for 20 nm holes diameter. Therefore, for practical use of block copolymer masks in IC circuit fabrication, it will be mandatory to develop better PMMA-removal processes in order to provide etching masks with a good initial CD control. As discussed previously, this can probably be achieved by combining UV cure and acetic acid treatment, but intense UV light sources were not available for our studies.

In the following, we fixed the Ar/O_2 step duration to 6 s, which allows to remove the random copolymer layer as well as to minimize the vertical and lateral consumption of the PS mask.

C. Etching the SiO_2 hard mask and curing the PS mask

After the PS-*r*-PMMA removal (6 s of Ar/O_2 plasma), a fluorocarbon-based plasma etching process is used to open the 10 nm thick SiO_2 mask. Two different CF_4 plasma conditions are investigated, both being efficient to open hard masks dedicated to silicon gate etching application. The first one is an highly dissociated plasma at high power (1000 W_s/150 W_b), which delivers a high flux of 200 eV ions to the wafer. The second one is a plasma operated at lower power (500 W_s/40 W_b), which produced a twice smaller flux of 140 eV energy ions (the ion energy distribution function are measured by a SEMION multigrid analyzer[36]). Figure 4 shows CD SEM top views of the samples for both plasma conditions, and in each case with and without the stripping of the remaining PS mask.

Figure 4(a) shows that the shape of the PS mask is apparently preserved when the SiO_2 layer is etched under low power conditions. However, after the stripping of the remaining PS by an O_2 plasma, it is evident that the nanoholes from the PS mask are hardly transferred into the SiO_2 mask under these conditions. Furthermore, it is impossible to increase the duration of the etching step because the etching selectivity between the PS mask and SiO_2 is too low. These plasma etching conditions, which works well for lower aspect ratio structures are thus not adapted to nanoholes etching.

By contrast, Fig. 4(b) shows that the PS mask is severely damaged after exposure to the high power etching plasma: the edge roughness of the holes increases and the initial circular shape of the PS holes is lost due to striations and faceting. Furthermore, these defects generated on the etched mask are partially transferred in the SiO_2 layer. However, after the removal of the remaining PS mask, one can see that the PS patterns are fully transferred into the SiO_2 hard mask (all the holes are open). This conclusion is not surprising since it is well known that contact holes etching in fluorocarbon plasmas

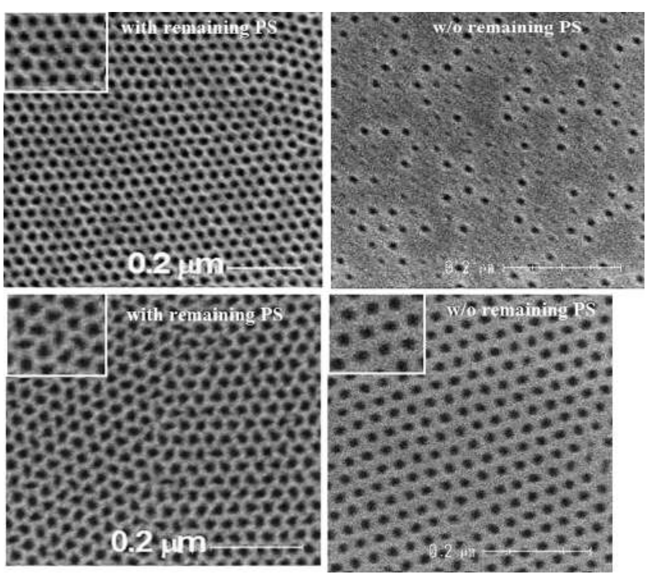

Fig. 4. CD SEM top view after SiO_2 etching (with and w/o remaining PS) for two CF_4 plasma conditions: (a) 45 SCCM CF_4, 500 W_s, 40 W_b, 4 mTorr and (b) 70 SCCM CF_4, 1000 W_s, 150 W_b, and 4 mTorr.

requires very energetic ion bombardment to overcome charging effects[37] (the accumulation of positive charges at the bottom of the holes reduces the ion flux and ion energy eventually leading to etch stop phenomena). Figure 4(b) also shows that the striations generated on top of the PS mask have not been fully transferred into the SiO_2 layer: the SiO_2 holes shape is slightly distorted but much less than the PS mask where the damage is mostly located at the top.

Therefore, those results show that a high flux of energetic ions is required to successfully transfer the PS nanoholes into the SiO_2 mask, but that such conditions may damage the PS mask, leading to poor critical dimension control if the initial PS mask thickness is too small (the issue is critical for 30 nm thick PS layer, less critical with our 60 nm PS mask).

The issue of photoresist (PR) mask degradation (striations and wiggling) under energetic ion bombardment is well known during fluorocarbon based plasmas exposure.[38,39] The PR damages are mainly explained by the crosslinking (agglomeration) and evaporation of the photoresist mixed with a plasma-deposited fluorocarbon polymer. In the 193 nm photoresist case, it has been shown that the mask LWR and its resistance to reactive etching plasmas is significantly improved by using hydrogen bromide (HBr) plasma cure of the photoresist before the plasma etching steps.[40–42] The main impact of the HBr plasma is the photolysis of the photoresist by vacuum ultra violet (VUV) photon, modifying the chemical and mechanical properties of the photoresist leading to a reduced LWR and an increased etch resistance toward aggressive plasmas.

Although PS has a chemical composition that is very different from 193 nm-photoresist (in particular PS has no ester nor lactone groups), we have evaluated the impact of a typical HBr plasma cure treatment (100 SCCM HBr, 5 mTorr, 1200 W_s) on the PS etch resistance during the SiO_2 etching step. Figure 5 shows the SEM top view of the sample after the HBr plasma and after the SiO_2 etching steps (both with and without HBr cure). The HBr cure does not modify the PS patterns' shape as evidenced Fig. 5(a), although a more careful analysis (see below) indicates that the holes diameter slightly shrinks during this process. Furthermore, the comparison between Figs. 5(b) and 5(c) indicates that the HBr cure treatment has a strong impact on the PS mask etch resistance: after SiO_2 etching process the shape of the HBr-cured PS holes is more circular and regular than without HBr cure. In addition, cross sections SEM indicate that the SiO_2 etching profiles are less tapered when the PS has been modified by an HBr plasma cure. This demonstrates that the HBr plasma cured PS is more resistant to plasma etching: it is less facetted and less eroded laterally than the nontreated PS.

To get insights into the chemical modifications undergone by the PS in the HBr plasma, we have carried out thermogravimetric analysis (TGA), in which mass loss is measured as a function of increasing temperature (with constant heating rate) and FTIR measurements as well as high resolution focused ion beam and scanning transmission electron microscopy (FIB-STEM) cross sections. Figure 6(a) shows that when the HBr plasma duration is increased, the residual mass after an annealing treatment at 500 °C under inert

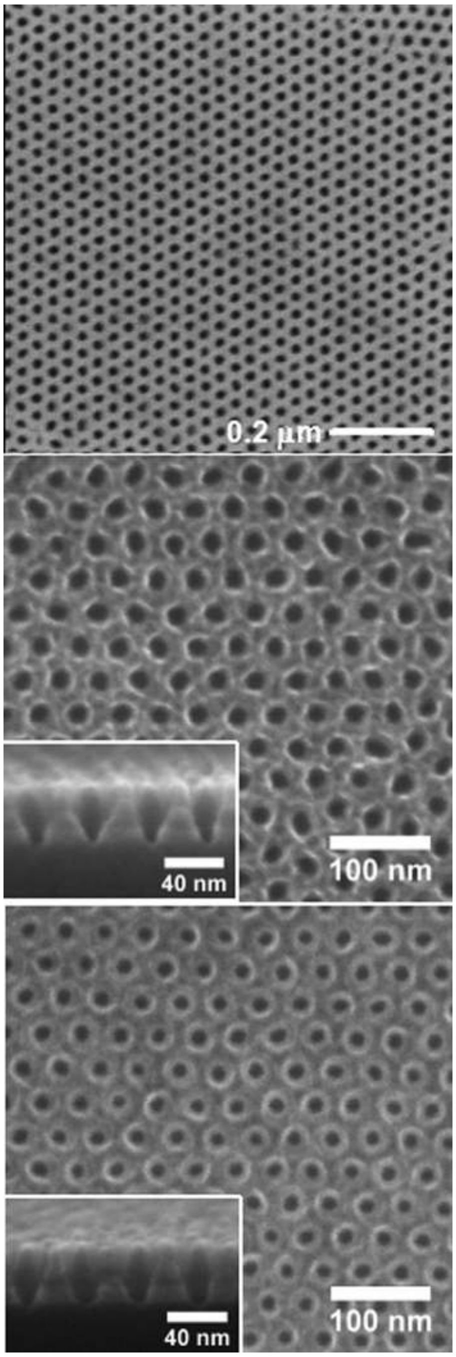

FIG. 5. SEM top view and cross section of (a) PS mask after HBr cure, (b) and (c) after the SiO_2 etching step without and with the HBr cure, respectively.

atmosphere increases. This is accompanied by a decrease of the CH bonds intensity (2800–3100 cm^{-1} region) measured by FTIR. All together, these results suggest that the increased etch resistance of the PS mask can be attributed to the graphitization and cross linking of the PS material induced by the VUV photons of the HBr plasma. Cross-sectional FIB-STEM images show that there is no change in the PS film thickness after HBr plasma treatment. However, a slight shrink of the holes diameter is induced by the HBr plasma [already observed in Figs. 5(b) and 5(c)] and is clearly visible by comparing Figs. 6(b) and 6(c). This "swelling" of the PS patterns during HBr plasma exposure is unexpected and the mechanisms responsible for the shrinking of the PS holes diameter induced by the HBr plasma treatment remain puzzling. The most plausible explanation is the redeposition of CBr_x radicals on the feature sidewalls.

At first glance, these results suggest that it is interesting to treat the PS masks by an HBr plasma to enhance their etch resistance and consequently to minimize the cylinder profile distortion during the SiO_2 hard mask etching steps. However, it must be underlined that during the HBr treatment the holes CD dispersion increases (while their diameter decrease). This is evidenced in Fig. 6(d), which shows the evolution of the histogram of the holes diameter distribution as a function of the HBr plasma duration. The mean pore diameter reaches his final value after 20 s of HBr plasma but the standard deviation of the holes CD distribution increases continuously with the plasma duration (i.e., the FWHM of the distribution increases from 2.3 nm before the HBr cure to 2.6 and 3.0 nm after, respectively, 20 and 60 s of plasma), showing that the HBr cure treatment induces an additional source of CD dispersion. A possible reason for this is the presence of variable amounts of PMMA residues remaining in the holes before the HBr treatment. This step is therefore interesting mainly if the etching selectivity is an issue and if CD-control is not drastic, i.e., for thin PS masks ($<$30 nm) and applications in nanotechnologies others than microelectronics.

D. Patterning silicon with the BCP/SiO_2 hard mask

After the SiO_2 hard mask opening step, the underlying silicon substrate is etched by a typical $HBr/Cl_2/O_2$ silicon gate etching process. In this chemistry the etching anisotropy relies on the formation of a $SiOCl_x$ passivation layer on the sidewalls during the etching process.[26,43,44] The passivation layer thickness must be minimized in order to achieve a good critical dimension control[7] but thick enough to prevent lateral etching below the SiO_2 mask. The thickness of these layers is directly controlled by the atomic oxygen concentration in the plasma[45,46] and can therefore be tuned, typically by controlling the O_2 dilution in the gas mixture. However, at the same time, the selectivity toward SiO_2 is also controlled by the O_2 gas flow rate, as well as by the ion energy (bias power). Hence, in typical silicon etching processes there is a tradeoff between the anisotropy and the selectivity.[44]

Figure 7 shows the SEM top view of the silicon substrate after etching through the PS/SiO_2 mask under various conditions of RF bias power and O_2 dilutions (after removal of the SiO_2 mask in a HF dip). Figure 7(a) is the result obtained with a process that is optimized for silicon gate etching, i.e., for the etching of silicon lines with a pitch larger than 70 nm. This process is $HBr/Cl_2/O_2$ plasma at low bias power (70 W) and low oxygen concentration. Under these etching conditions, only a small percentage of the SiO_2 mask holes have been transferred into the Si underlayer after 40 s of etching, which demonstrates that a typical gate etching process cannot be used to etch nanoholes. Figure 7(b) shows that increasing the rf bias power (hence the ion energy) does not really improve the situation: the

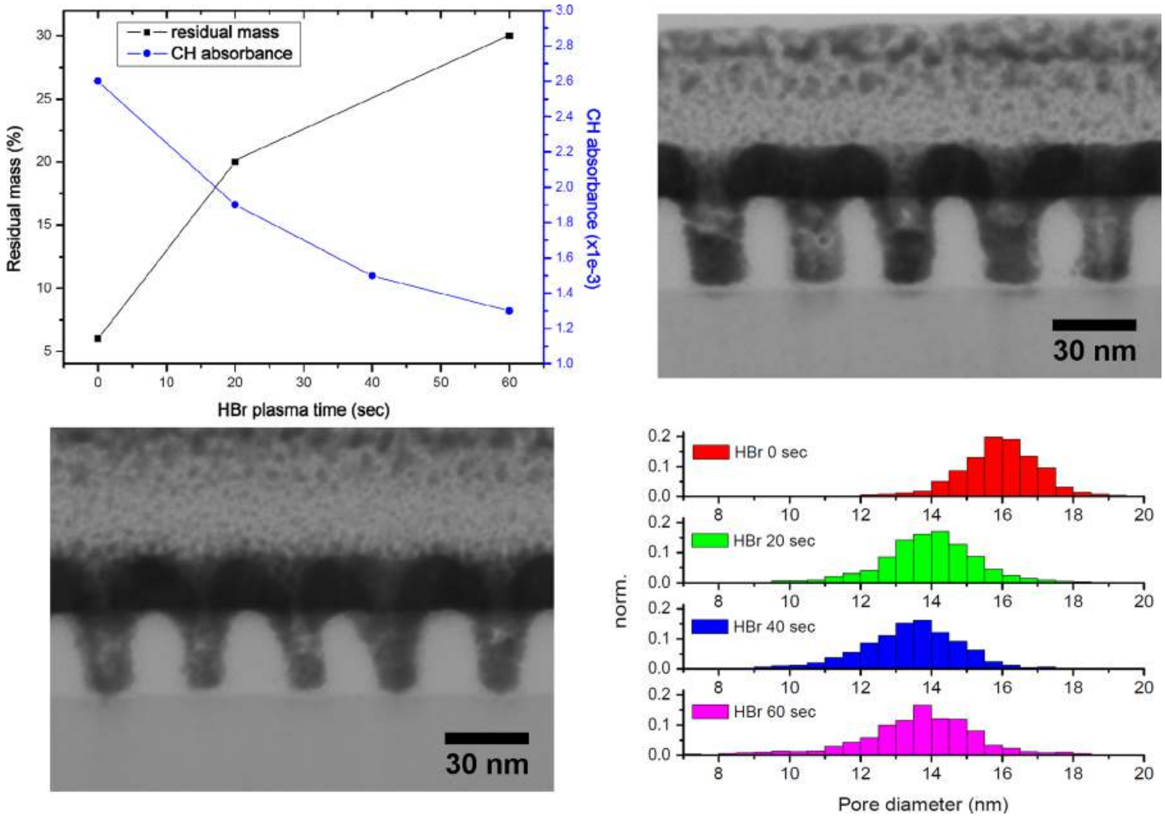

FIG. 6. (Color online) (a) Evolution of the residual mass of PS matrix film after 500 °C annealing under inert atmosphere (TGA) and C–H bonds intensity (2800–3000 cm^{-1} region—FTIR) in function of HBr plasma time. FIB-STEM cross section of PS matrix (b) before and (c) after 40 s of HBr plasma. A thin Pt layer was deposited on top of the PS matrix film to enhance the contrast between the copolymer and the amorphous carbon capping layer. (d) Evolution of pore diameter distribution with the time of HBr plasma.

SiO_2 holes are not fully transferred into the Si. By contrast, Fig. 7(c) shows that using a high bias power without O_2 in the plasma chemistry (i.e., a pure HBr/Cl_2 plasma) allows the successful transfer of SiO_2 holes into the Si layer. This is indicating that during the etching of nanoholes into silicon, even very small amounts of O_2 leads to an excessive formation of $SiOCl_x$ passivation layers, which tend to clog the PS mask holes thus preventing their transfer into the silicon. It is indeed known that the passivation layer tend to grow mostly on the top part of the sidewalls of high aspect ratio structures due to the high surface sticking probability of O atoms: in the case of nanoholes, this leads rapidly to the closing of the mask. It is thus mandatory to use a non-passivating chemistry to get an efficient transfer of the PS holes into the silicon. However, without passivation layers, the silicon sidewalls are not protected and one could expect them to be etched laterally generating an undercut below the mask. Surprisingly, Fig. 9, which shows a cross section of the silicon etching profile, demonstrates that it is not the case.

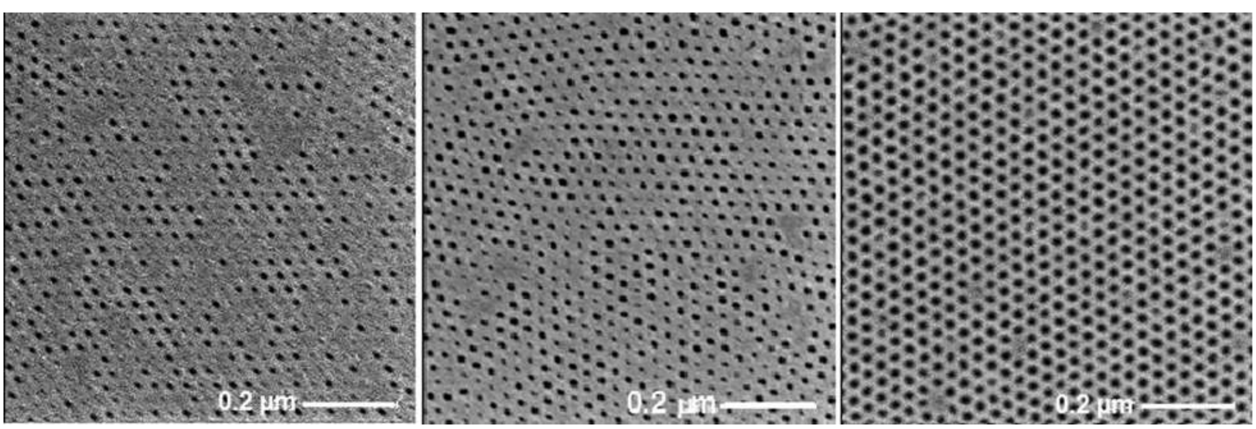

FIG. 7. SEM top view after Si etching step (after SiO_2 removal) using conventional plasma chemistry (4 mTorr, 120 SCCM Cl_2/xO_2, 250 W_s, (a) at low bias power condition ($W_b = 70$ W) and low oxygen concentration (1.5 SCCM O_2), (b) at high bias power condition ($W_b = 120\,W_b$) and low oxygen concentration (1.5 SCCM O_2), and (c) at high bias power condition ($W_b = 120$ W) and without O_2).

Etch profiles into silicon for different plasma etching durations were investigated by cross section observation with a FIB-STEM. An anisotropic etch profile is observed with a slight slope and almost no undercut whatever the etch duration [Figs. 8(a) and 8(b)]. There is no detectable passivation layer on the feature sidewalls on the FIB-STEM cross section, which is to be expected since the silicon was etched in an O_2-free plasma etching chemistry.

The absence of undercutting under our conditions could simply be the consequence of a lack of etchants reaching the feature sidewalls. This lack of etchant is due first to the fact that in Cl_2-based plasmas without O_2 the reactor walls stays "clean" and that the recombination coefficient of Cl atoms into Cl_2 molecules on clean walls is very high, leading to a low Cl density in the discharge.[47,48] Second and more importantly, we expect that during the etching of nanoholes only a very low flux of Cl atoms can reach the feature sidewalls because of the shadowing effect.[35] Indeed, the solid angle of collection of the reactive species (H, Br, and Cl) from the plasma in a high aspect ratio hole is so small that only a very low flux of etchant is expected to reach the sidewalls thus leading to negligible undercutting. This is an important conclusion as it means that anisotropic etching without passivation layers could be an inherent property of the plasma etching mechanisms in high aspect ratio, nanometric size holes.

Finally, we cannot rule out the possibility that some sidewall passivation is provided by the bottom of the holes: the energetic ions bombardment can lead to the chemical sputtering of poorly volatile $SiCl_x$ radicals ($x = 0$–1) from the bottom of the holes and these radicals can redeposit on the feature sidewalls before escaping the hole. This "passivation" mechanism is known to take place during silicon etching in other chemistries[49] and it leads to tapered profiles comparable to those observed in Fig. 8. In low aspect ratio structure, without oxygen to fix the silicon on the surface by oxidation, the redeposited silicon is etched away by Cl and recycled in the plasma as $SiCl_4$ (Ref. 50) and this mechanism is not expected to be very efficient. However, in high aspect ratio holes, the shadowing of Cl atoms is significant, and this passivation mechanism may be effective.

Finally, Fig. 8(c) shows that the etch depth and etch rate as a function of the etching time. The silicon etch rate decreases continuously when the etch depth increases, which is indicating that the etch rate is aspect ratio dependent. This is a well-known phenomenon, so called RIE lag, which is also due to the fact that the shadowing effect of radicals depends on the aspect ratio[36]: as the aspect ratio increases a smaller flux of etchants reaches the bottom of the features because their solid angle of collection decreases. Furthermore, charging effects of the insulator SiO_2 mask may also be responsible for a decrease of the ion flux and energy at the bottom of the holes thus participating to the etch rate drop.[51,52] These effects are critical with block copolymer masks as the solid angle of collection of radicals from the plasma is strongly reduced when 10 nm diameter holes are considered. Indeed, at the nanometer scale we can expect that the variability in holes diameter will result in a variability of the etch rate since the AR varies

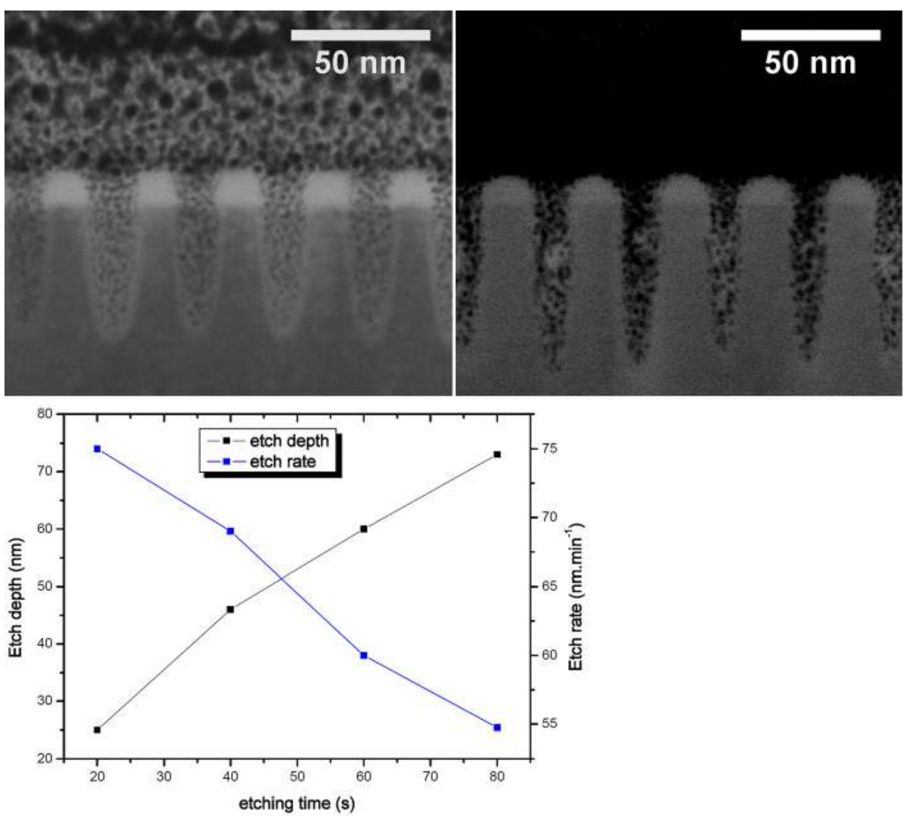

FIG. 8. (Color online) FIB STEM cross section view after Si etching with the optimized etching process for a duration of (a) 40 s and (b) 60 s. (c) Etch depth and etch rate of Si as function of time with the optimized etch process.

with the hole diameter: this is clearly visible in Fig. 8 and this effect is expected to complicate etching processes.

Finally, we have investigated the maximum possible depth that can be etched in the silicon substrate with a 10 nm thick SiO_2 hard mask. We found that the PS mask, which remains on top of the SiO_2 mask, plays an important role on the maximum etching depth because it protects the SiO_2 hard mask from erosion during several seconds. Indeed our SiO_2 mask is etched away by the silicon etching plasma (the etching selectivity Si/SiO_2 is about 8 in our O_2 free HBr/Cl_2 chemistry). However, if the PS mask used to pattern the SiO_2 hard mask is kept in place during the silicon etching process, it will protect the SiO_2 hard mask for a significant time thus allowing a longer etching time to be achieved. As shown in Fig. 8, 70 nm deep nanoholes were successfully transferred into the silicon substrate after 80 s of etching, but above that time the SiO_2 mask becomes too thin to allow a good CD control.

For deeper etching, a thicker hard mask is required. We have thus investigated the capability of PS-*b*-PMMA BCPs to pattern state-of-the-art trilayer HM that is typically used to pattern most materials in the microelectronic industry.

E. Patterning the SiARC/a-C/Si stack with BCP

Typical etching processes involved in IC circuits fabrication are using a complex stack as a hard mask.[3] The motivation for this choice includes the necessity to have an antireflective layer for the 193 nm-lithography and the necessity to start the etching process with a well-defined (in terms of CD control) and thick mask that will allow pattern transfer in many materials. Therefore, if BCP can be used instead of a 193 nm resist to pattern this hard mask stack with a good critical dimension control, it will pave the way to the use of BCPs in CMOS technology. Our hard-mask stack consists of 30 nm of Si-ARC (which is basically a spin-on layer containing Si, O, and C elements) on top of a 70 nm thick spin-on amorphous carbon layer (a–C). The BCP are deposited on top of this stack and as previously, we start by etching the random copolymer layer and curing the PS mask with an HBr plasma. The PS mask is then used to etch the 30 nm thick SiARC layer.

The optimized Si-ARC etching process uses different and more polymerizing plasma chemistry (CF_4/CH_2F_2/Ar) than the typical process used previously to etch SiO_2 (70 SCCM CF_4, 4 mTorr, 1000 W_s, 150 W_b, and 10 s). This Si-ARC etching plasma was originally optimized to etch 70 nm diameter contact holes giving satisfactory results for such dimensions and aspect-ratio. When using for sub-20 nm diameter holes through a PS mask, strong striations and deformation of the PS matrix are observed and the Si-ARC layer is not etched at all [Fig. 9(a)]. This indicates that this process is not adapted neither to high aspect ratio hole etching nor to PS masks. This is the result of using a strongly polymerizing chemistry in conjunction with charging effect of the insulating Si-ARC in high aspect-ratio holes: both the flux and the energy of the ions are strongly reduced in high aspect-ratio structures due to accumulation of positive charges at the bottom of the holes, so that polymer deposition prevails over Si-ARC etching.[37] In addition, the presence of neutralizing layer (PS-*r*-PMMA) residue at the bottom of the PS pore could also explain why the Si-ARC cannot be opened in highly polymerizing plasma. We have therefore removed the CH_2F_2 gas from the gas mixture to reduce the polymerization capabilities of the plasma. As shown in Fig. 9(b) this is effective enough to etch the SiARC layer. However, a strong

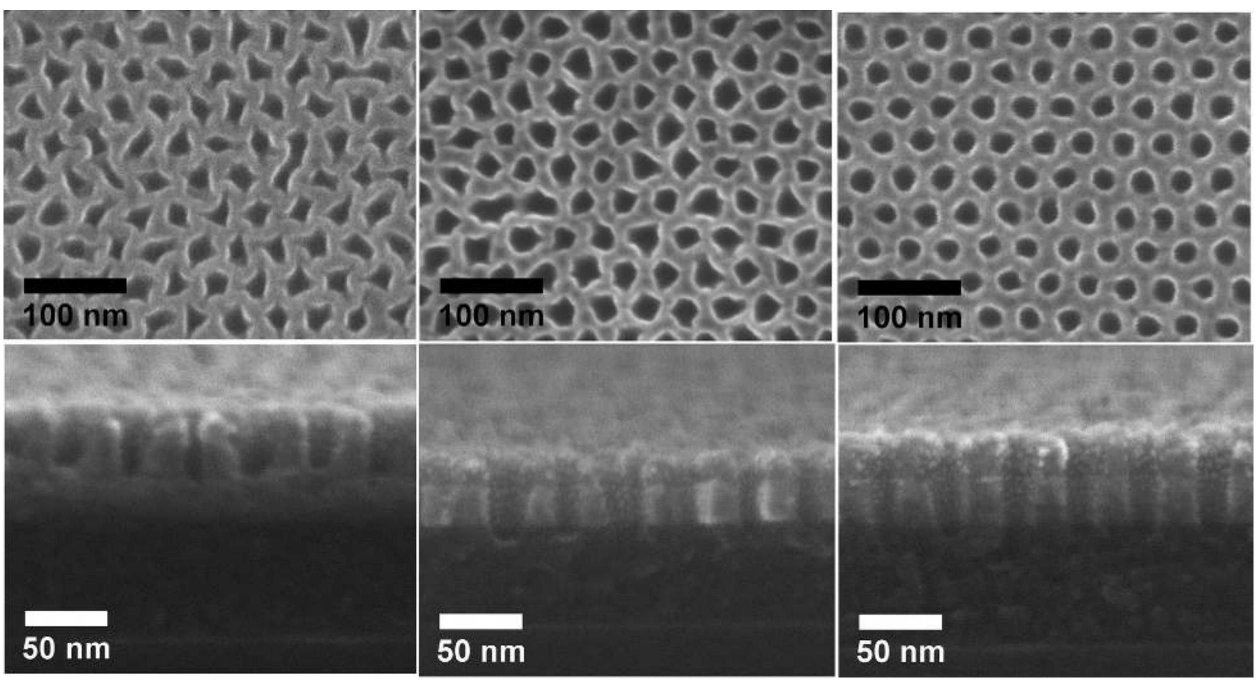

FIG. 9. SEM top view and cross section of PS/Si-ARC/a-C/Si stack after Si-ARC etching with (a) conventional plasma (CF_4/CH_2F_2/Ar), (b) plasma with low polymerization (CF_4/Ar), and (c) SiO_2 etching plasma condition (CF_4).

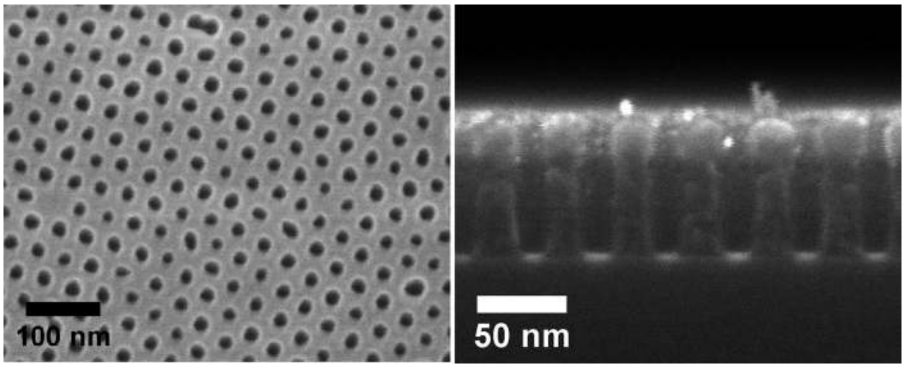

FIG. 10. (a) SEM top view and (b) cross section of Si-ARC/a-C/Si stack after a-C etching with conventional HBr/O_2 plasma.

profile deformation of the contact holes shape is observed when the Si-ARC is etched in the Ar/CF_4 plasma. This is most probably due to the energetic bombardment of the PS by a high Ar+ ions flux leading to low selectivity toward the PS under these conditions. It is also visible that the process suffers from aspect ratio dependent etch: the second hole from the left in Fig. 9(b) (bottom) has a larger diameter than other holes and as a result it has been etched faster resulting in some consumption of the a-C layer.

Finally, the best results in terms of selectivity and anisotropy [Fig. 9(c)] are obtained with the same process described previously to etch the SiO_2 HM (CF_4 plasma without Ar, which preserves the PS mask).

The a-C layer is then etched by an HBr/O_2 plasma. This process was originally developed for 70 nm diameter holes and as shown in Fig. 10 it is also able to pattern higher aspect ratio structure since the a-C is etched with an excellent anisotropy. This is attributed to the fact that the process is strongly ion-assisted (no polymerization or passivation layer formation) and that the a–C is a conductor which does not charges electrically. We note that the original PS mask is totally etched after few seconds of etching but that the selectivity between a-C and Si-ARC is so high that very deep holes can be etched in the carbon with the 30 nm thick Si-ARC mask. At this stage, we have defined a high aspect ratio (~5), plasma resistant hard mask that can be used to pattern a wide variety of materials.

Finally, the transfer of this mask into the silicon layer was done by using the HBr/Cl_2 plasma described previously to etch silicon through the thin SiO_2 mask. Figure 11(a) shows the initial mask (hole array into Si-ARC/a-C) and Fig. 11(b) the result observed after the silicon etching process. It turns out that the silicon is hardly etched and that at the same time the etching selectivity toward the a-C/Si mask is very low (there is almost no mask remaining on the silicon). This is attributed unambiguously to the high aspect ratio of the

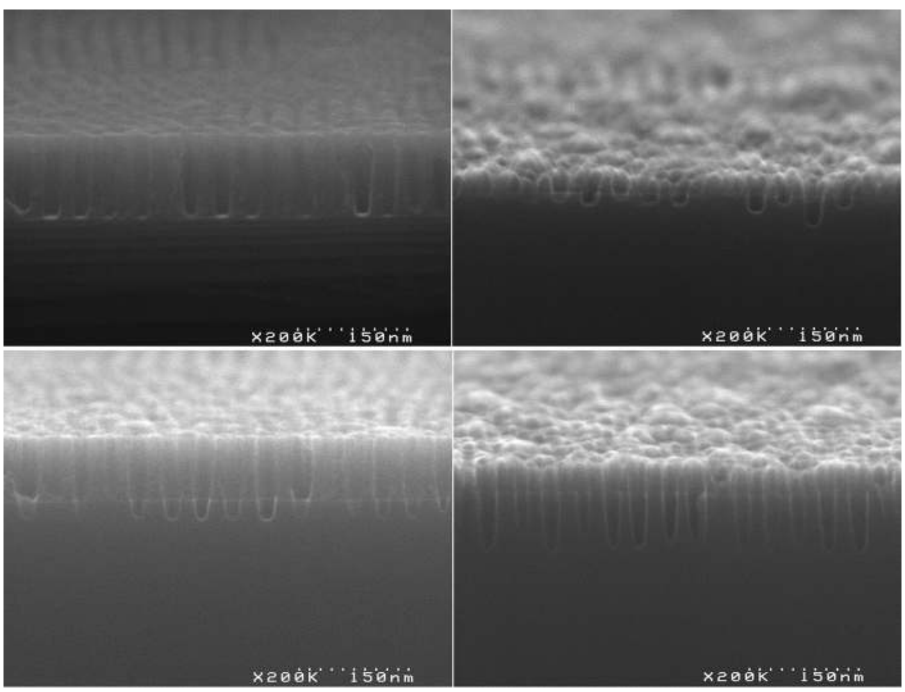

FIG. 11. SEM cross section views after transfer into Si with different plasmas. (a) Initial Si-ARC/a-C mask, (b) after 30 s of continuous HBr/Cl_2 plasma, (c) after 120 s of pulsed HBr/O_2 plasma, and (d) after 360 s of pulsed HBr/O_2 plasma.

initial mask. It is indeed probable that the little etch observed in silicon has taken place at the end of the process, when the aspect ratio was reduced by the mask consumption.

This is indicating that to etch silicon with a high aspect ratio Si-ARC/a-C mask, it is necessary to strongly increase the etching selectivity toward the mask and to use more energetic ions bombardment to ensure that the etching proceeds. Such conditions are typically those obtained in CCP plasma reactors, but recent work suggests that they can also be reached in ICP plasma by pulsing the discharge at high frequency and low duty cycle, because under such conditions the ion flux drops resulting in higher ion energy at constant rf biasing power.[36] In addition, it is known[53] that pulsing the plasma prevent charging effects of the patterns, favoring thus the etching. We have therefore etched the silicon wafer by using a pulsed HBr/O_2 plasma (which is well known to be highly selective toward the SiARC). The plasma was pulsed at 1 kHz with a duty cycle of 20%. Figure 11(c) shows the cross section after silicon etching with this plasma and for an almost equivalent rf ON duration as for continuous HBr/Cl_2 plasma [Fig. 11(b)]. This figure shows that this process etches the silicon at a relatively slow rate, but that the selectivity toward the mask is much higher than in the cw plasma, therefore allowing a much longer etching time to be achieved. This is demonstrated in Fig. 11(d), in which the etching time was increased to 360 s: 75 nm deep holes were successfully transferred into the silicon by using the pulsed plasma process, demonstrating the interest of using such plasmas to pattern high aspect-ratio, nanometer scale features.

IV. SUMMARY AND CONCLUSIONS

We studied the best strategies to transfer nanopatterns formed from the self-assembly of PS/PMMA block copolymers into a silicon substrate. Since the etching selectivity between PS and silicon is low, it is necessary to use a hard mask strategy for accurate etching of sub-20 nm holes into silicon. We have investigated both a single hard-mask approach (10 nm thick SiO_2) or a dual hard mask strategy (Si-ARC/a-C). In both cases, the substrate patterning with a BCP mask requires specific steps and strong modifications of the typical etching processes that are used to pattern larger features (193 nm-lithography). These process modifications are imposed by the high aspect-ratio and the nanometric dimensions of the etched structures. The nanometric size of the holes precludes the use of polymerizing plasma chemistries, which fills the holes and blocks the etching. Therefore, plasma processes in which the anisotropy relies on the formation of passivation layers on the feature sidewalls must be modified to reduce (or prevent) the deposition rate of these layers. Surprisingly, we observe that this is not at the detriment of the etching anisotropy. This was attributed to a lack of etchant available for lateral etching: in high aspect ratio holes the flux of etchant is strongly reduced by shadowing effects. In addition, we have often observed that typical state of the art etching processes are sometime unable to etch the material (in particular insulating materials) due to charging effects in high aspect ratio holes. Increasing the ion bombardment energy (if necessary by using synchronized pulsed plasma) is the only solution to this issue. Finally, we have also identified a serious issue associated with BCP in terms of CD control when the BCP material is reconstructed by an acetic acid treatment: chains of PMMA inside the PS holes lead to CD microloading during the subsequent etching steps (random polymer etching and HBR cure). The CD control is thus not yet satisfying but if this issue can be fixed (by using UV treatment combined to wet) our results indicate that block copolymer can be readily used as etching masks for advanced CMOS technology.

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