Rutile-structured TiO2 deposited by plasma enhanced atomic layer deposition using Tetrakis(dimethylamino)titanium precursor on in-situ oxidized Ru electrode

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Rutile-structured TiO_2 deposited by plasma enhanced atomic layer deposition using tetrakis(dimethylamino)titanium precursor on *in-situ* oxidized Ru electrode

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In this work, tetrakis(dimethylamino)titanium precursor as well as *in-situ* oxidized ruthenium bottom electrode were used to grow rutile-structured titanium dioxide thin layers by plasma enhanced atomic layer deposition. Metal–insulator–metal capacitors have been elaborated in order to study the electrical properties of the device. It is shown that this process leads to devices exhibiting excellent results in terms of dielectric constant and leakage current. © *2014 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4843515]

I. INTRODUCTION

The requirements for future dynamic random access memory (DRAM) capacitors are summarized in the International Technology Roadmap for Semiconductors. For sub-22 nm node, challenging performances like equivalent oxide thickness (EOT) < 0.5 nm and leakage current density $<1 \times 10^{-7}$ A/cm^2 at 0.8 V are required. Titanium dioxide (TiO_2) is an attractive dielectric material for such application thanks to its high dielectric constant (k) and possibility of conformal deposition for this metal oxide on high aspect ratio 3D structures.[1] Depending on its growth conditions, TiO_2 can be prepared in amorphous, anatase, or rutile phase. Rutile-structured TiO_2 might be a promising candidate for next generation DRAM capacitor as it exhibits dielectric constant ranging from 90 to 170,[2] depending on the layer's lattice orientation. Rutile phase is difficult to obtain at back-end compatible temperature, i.e., $<400\,^{\circ}$C, since thermal processing at higher temperature ($>800\,^{\circ}$C) is commonly needed to get this phase.[3] However, it was recently reported that rutile phase could be obtained at low temperature by using the local epitaxial relationship between the rutile structure of TiO_2 and structurally compatible electrodes such as RuO_2 (Ref. 4) and IrO_2.[5] It was also shown that this rutile phase can be obtained by using a specific plasma enhanced atomic layer deposition (PEALD) setup, enabling substrate-biasing during TiO_2 growth.[6] Despite interesting electrical properties of rutile TiO_2, its small band gap (3 eV) and the n-type nature of TiO_2 due to the presence of various defects such as oxygen vacancies or Ti interstitials[2] lead to a low Schottky barrier height for electron injection when in contact with a metal electrode. This makes it difficult to obtain small leakage current required for high-performance DRAM capacitors. Aluminum doping of TiO_2 layer (ATO) is commonly used[7,8] in order to reduce the leakage current. Indeed, Al ions act as an acceptor to compensate the n-type nature of TiO_2 (Ref. 8) and thus prevent energy barrier between conduction band edge of TiO_2 and the Fermi level of the electrode from being reduced.

The aim of this work is to study the electrical properties of TiO_2 layers grown by plasma enhanced ALD using tetrakis(dimethylamino)titanium (TDMAT) as a precursor and by performing *in-situ* Ru bottom electrode oxidation. Indeed, we compare TiO_2 and ATO MIM capacitors based on two different bottom electrodes (Pt or RuO_2/Ru). ATO layers are obtained with several Al-doping levels.

II. EXPERIMENT

TiO_2 layers were deposited using TDMAT precursor and O_2 plasma as oxidant at 250 °C in a Cambridge (Fiji) PEALD reactor. They were grown on two different metal electrodes (Pt and RuO_2/Ru) at a typical growth rate of 0.05 nm/cycle. Pt and Ru electrodes are deposited using e-beam evaporator. The thin layer of RuO_2 (~3 nm) is obtained from Ru electrode after annealing process in PEALD chamber during 1 h at 400 °C under O_2 plasma atmosphere. AlO_x layer in ATO layers were grown in the PEALD reactor, using trimethylaluminum (TMA) precursor and O_2 plasma as oxidant. ATO MIM capacitors with several doping levels were elaborated. For example, ATO 1/60 stands for an ATO layer which is deposited by pulsing 1 Al ALD cycle every 60 Ti ALD cycles. Thickness measurements of TiO_2 and ATO films in studied MIM capacitors have been monitored using x-ray reflectometry and ellipsometry techniques. Oxides (TiO_2 or ATO) are about 19 nm thick. Gold top electrode is made by using e-beam metal evaporator. Gold layer is deposited on patterned photoresist layer, followed by lift-off process. The Au electrodes surface area range from 50 μm $\times$ 50 μm to 400 μm $\times$ 400 μm. All samples were annealed in the PEALD reactor at 400 °C under O_2 plasma atmosphere for 1 h in order to enhance their electrical properties. Current–voltage and capacitance–voltage measurements were achieved, using a Keithley 4200-SCS electrical characterization setup. GA-XRD (grazing angle x-ray diffraction) and HRTEM (high resolution transmission electron microscopy) have been carried out for physicochemical characterization.

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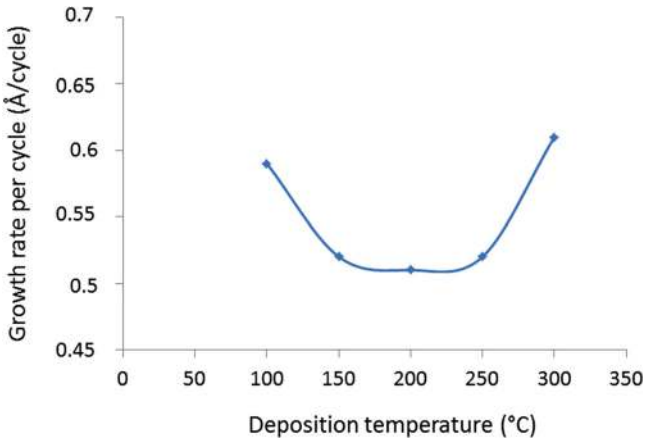

FIG. 1. (Color online) GPC vs deposition temperature for plasma assisted ALD TiO_2 film growth from TDMAT and O_2. An ALD window is observed between 150 and 250 °C.

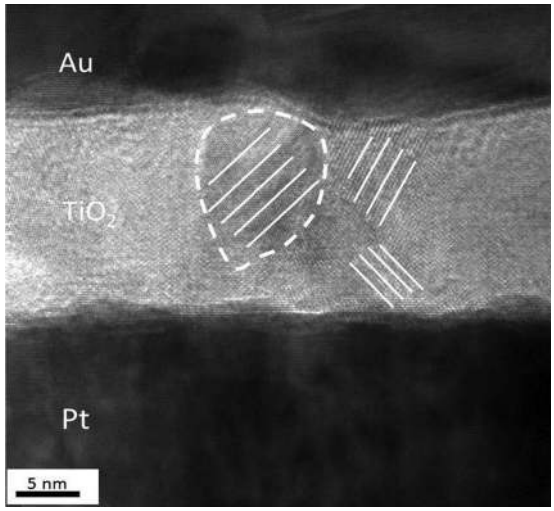

FIG. 2. Cross-section HRTEM image of a 19 nm polycrystalline TiO_2 film deposited on Pt substrate.

III. RESULTS AND DISCUSSION

The deposition temperature used in this work (250 °C) is recommended by the PEALD equipment supplier. This temperature might be too high and incompatible to ALD deposition mode with TDMAT as a precursor. Indeed, it is known that thermal decomposition of TDMAT precursor starts at temperatures as low as 130 °C.[9] In that respect, the film growth at 250 °C may be in the CVD (chemical vapor deposition) mode due to possible thermal decomposition or desorption of the TDMAT precursor or intermediate species before the surface reactions with the oxygen radicals takes place, during the second step of the ALD cycle. However, the following experimental results show that, in our case, the TiO_2 layer growth at 250 °C takes place in the ALD mode. Indeed, we investigated the TiO_2 layer growth rate as a function of the deposition temperature. As shown by Fig. 1, the growth rate is flat between 150 and 250 °C. This strongly suggests an ALD growth mechanism (ALD window). Moreover, the growth rate per cycle (GPC) of TiO_2, shown by Fig. 1, is rather small and consistent with previously reported values for ALD deposition process.[10] In contrast, typical TiO_2 growth rate by CVD is largely higher[11] than the growth rate observed in our work. We have also investigated the influence of TDMAT precursor pulse duration on the deposited layer thickness. Different pulse durations ranging from 0.1 to 0.5 s have been used to grow TiO_2 layers, while keeping a common sequence of 200 deposition cycles. The resulting layers showed very close thickness value (~10 nm). This is another strong indication of the self-limiting nature of the deposition process used in this work.

Preliminary study has been performed on platinum bottom electrode on which TiO_2 thin layer has been grown by PEALD using TDMAT precursor. The platinum electrode is interesting in MIM capacitor due to its high work function (5.6 eV) allowing drastic reduction in leakage current. Furthermore, its chemically inert nature prevents the formation of low-k interfacial layer between electrode and insulator that may degrade the global dielectric constant of the structure. HRTEM image of TiO_2 on Pt, shown in Fig. 2, reveals that polycrystalline phase is present in TiO_2 layer, but it was not possible to determine if it is an anatase or a rutile one. Consequently, x-ray diffraction (XRD) measurements have been performed as shown in Fig. 3, where no rutile peaks can be observed. Only anatase phase is present. Therefore, deposition of TiO_2 layer by PEALD at low temperature (250 °C) on platinum electrode using TDMAT precursor leads to anatase-structured TiO_2 with rather low dielectric constant value. Indeed, we measured k values around 40 as shown in Fig. 4. This value is too low and does not allow meeting the international technology roadmap for semiconductors (ITRS) requirements (EOT of 0.5 nm) for next generation DRAM capacitors. These results obtained with TDMAT precursor are consistent with different results in the literature obtained for TiO_2 growth on Pt electrode by using other Ti precursors.[12] Furthermore, a high leakage current density ($\sim 10^{-4}$ A/cm^2) is observed on TiO_2/Pt stack as shown in Fig. 4. Although this leakage current can be reduced by Al doping to a value of 10^{-5} A/cm^2 (Fig. 4), this value remains too high to meet the targeted requirements. Giving the previously reported good electrical properties obtained on rutile-phase TiO_2, we set out to investigate this phase growth with TDMAT precursor. Considering that low

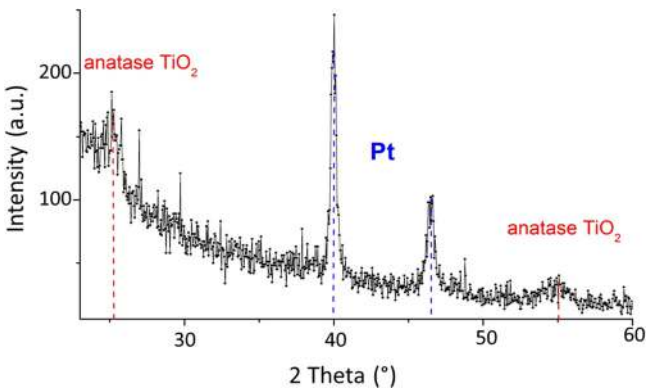

FIG. 3. (Color online) GA-XRD pattern of a 19 nm thick TiO_2 layer deposited on Pt substrate. TiO_2 layer is polycrystalline and anatase-structured.

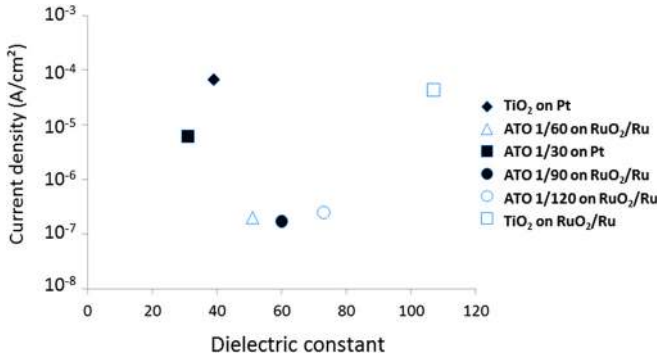

FIG. 4. (Color online) Leakage current density measured at 0.8 V vs dielectric constant for MIM capacitors embedding TiO_2 or ATO as insulators and either Pt or RuO_2/Ru as bottom electrodes.

temperature (<400 °C) growth of rutile phase can only be obtained from a lattice-matched bottom electrode, ALD oxidation process with remote O_2 plasma has been defined to get thin RuO_2 layer on top of a 30 nm thick Ru electrode. Indeed, this *in-situ* process allows consecutive oxidation of the Ru and deposition of the dielectric (TiO_2 or ATO) layer. Moreover, as RuO_2 is a conductive oxide, no low-k interfacial layer will interfere with high-k TiO_2 or ATO insulators in MIM capacitors. X-ray reflectometry (XRR) measurements have been carried out to get accurate thickness value of RuO_2 formed during the oxidation step in the ALD chamber. Accurate RuO_2 thickness measurements are possible by XRR even with ultrathin layers (2–3 nm) as it is the case in the present study. Indeed, XRR technique is well suited if the ultrathin layers have very different densities, which is the case for the RuO_2 and Ru layers whose respective densities are 6.97 and 12.1 g cm^{-3}. XRR measurements yielded 3 nm for RuO_2 thickness. Furthermore, as low roughness is required in XRR to safely extract such small thicknesses, one could affirm that RuO_2 layer presents very low surface roughness.[13] This thickness value is high enough (>2 nm) for making possible local epitaxial growth of TiO_2. In Fig. 5,

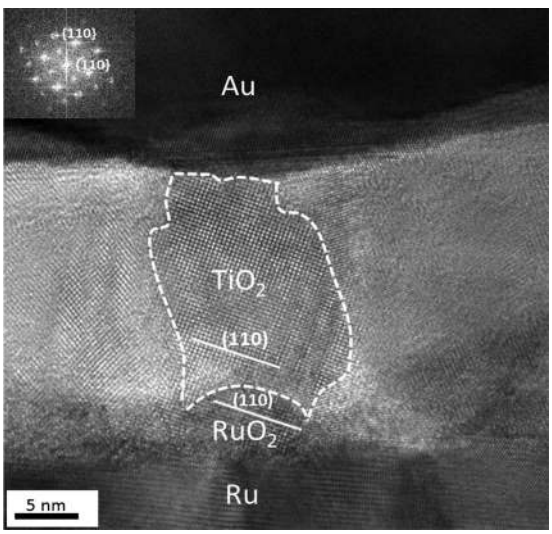

FIG. 5. Cross-section HRTEM image of TiO_2/RuO_2/Ru stack, TiO_2 is in epitaxial relation with RuO_2. Fast Fourier transform diffraction pattern (inset) of the delimited TiO_2 grain exhibits rutile structure.

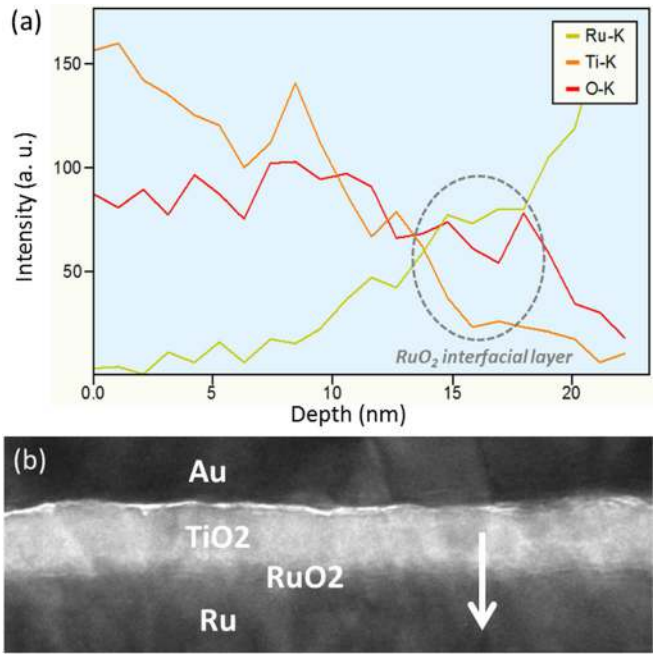

FIG. 6. (Color online) (a) EDX profile of Ru-K, Ti-K, and O-K lines across the TiO_2/RuO_2/Ru stack. (b) STEM image of the Au/TiO_2/RuO_2/Ru stack where the EDX profile cutline is indicated.

HRTEM image analysis of the whole stack strongly suggests the presence of RuO_2 layer at the TiO_2/Ru interface. In order to confirm this assumption, the composition of this interfacial layer can be identified by performing energy dispersive x-ray spectroscopy (EDX) analysis, coupled to HRTEM observation. The resulting profile of TiO_2/RuO_2/Ru stack is shown in Fig. 6. This profile displays Ru-K, Ti-K, and O-K lines intensity across the TiO_2/RuO_2/Ru stack. RuO_2 area is materialized on the graph by the decrease of Ti-K intensity, the increase of Ru-K intensity, whereas the O-K intensity remains constant (x-position between 15 and 18 nm).

Dashed line on the HRTEM image (Fig. 5) highlights the presence of a rutile TiO_2 grain whose (110) plans are oriented in the same direction as (110) plans of RuO_2. It can be

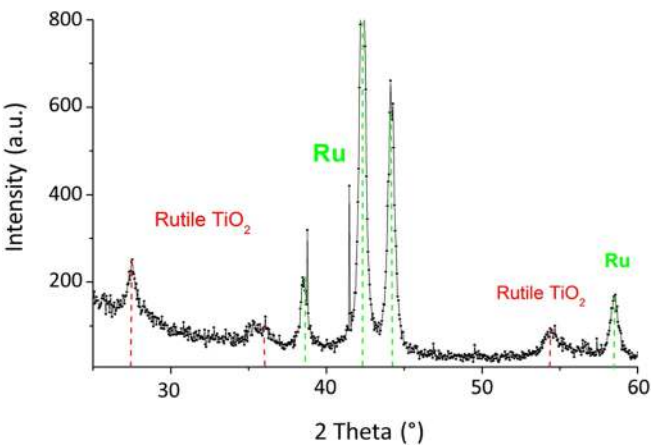

FIG. 7. (Color online) GA-XRD pattern of a 19 nm thick TiO_2 layer deposited on RuO_2/Ru substrate. TiO_2 layer is polycrystalline and rutile-structured.

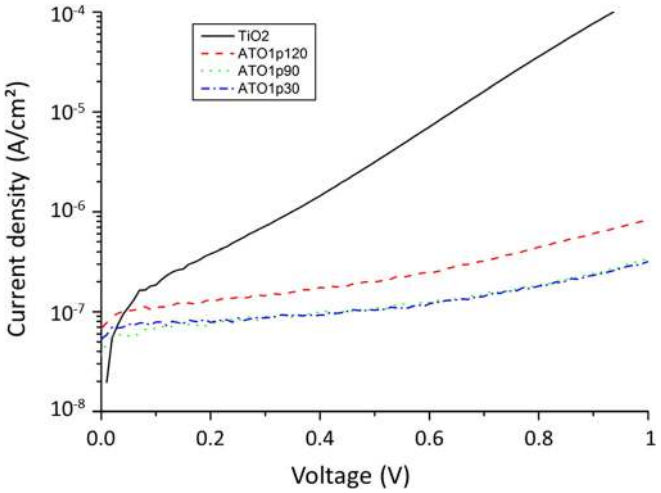

FIG. 8. (Color online) Current–voltage characteristic of Au/TiO_2/RuO_2/Ru and Au/ATO/RuO_2/Ru MIM capacitors. Results are shown for ATO layers with different Al-doping levels.

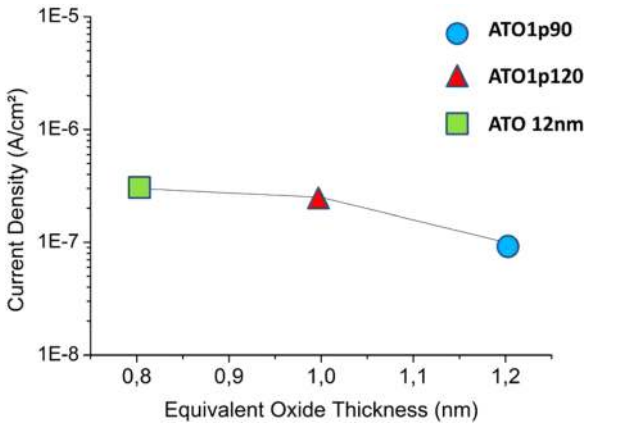

FIG. 9. (Color online) Leakage current density at 0.8 V vs EOT for ATO layers with different Al-doping levels and thicknesses. ATO 12 nm stands for a 12 nm thick ATO 1/60 layer.

deduced that TiO_2 is in epitaxial relation with RuO_2 in this area. GA-XRD characterization of TiO_2 on RuO_2/Ru electrode, shown in Fig. 7, confirmed this assumption by displaying rutile peaks. Although RuO_2 has almost the same lattice parameters as rutile TiO_2, those peaks can only be attributed to rutile TiO_2 layer because the 3 nm thick RuO_2 layer is far too thin to be detected with GA-XRD technique. Therefore, these results guarantee that rutile-structured TiO_2 can be obtained from TDMAT precursor, using a low temperature ALD process for consecutive bottom Ru electrode oxidation and TiO_2 deposition.

For electrical characterization part, current–voltage [I(V)] measurements have been achieved on MIM capacitor embedding TiO_2 and ATO as dielectrics, with RuO_2/Ru as bottom electrode. I(V) characteristics, shown in Fig. 8, clearly reveal a drastic decrease in leakage current for capacitors with Al-doped titanium dioxide layers, compared to undoped TiO_2. Indeed, considering ATO MIM structures, leakage current decreases with the increase of [Al]/([Al] + [Ti]) ratio. In addition, it is interesting to notice that capacitors integrating ATO 1/90 or ATO 1/30 are close to fulfill the ITRS requirements in terms of leakage current (i.e., leakage current $\sim 10^{-7}$ A/cm^2 at 0.8 V).

Dielectric constants extracted from capacitance measurements at 10 kHz on different types of studied samples are listed in Table I. For TiO_2 grown on RuO_2/Ru or on Pt electrodes, dielectric constants are, respectively, 107 and 39, which is consistent with the theoretical value for TiO_2 rutile and anatase phases. In addition, Table I shows that although Al-doping tends to reduce the dielectric constant, values obtained for MIM capacitors with 1/120 or 1/90 ATO on RuO_2/Ru electrode stay rather high (respectively, 73 and 60),[7] compared to the one obtained on pure TiO_2 on Pt. Since the electrical performance criterion for MIM capacitors is the result of the combination of low leakage current and high dielectric constant, we summarized in Fig. 4 the electrical properties for all studied structures. Figure 4 shows that 1/120, 1/90, or 1/60 ATO layers represent the best tradeoff between leakage current density and dielectric constant. Moreover, Fig. 9 is presented to highlight achievements in terms of electrical performances but also to assess the necessary work on reducing the physical oxide thickness in order to get EOT closer to 0.5 nm. An insight of the forthcoming work is proposed since a result of 0.8 nm in terms of EOT has been reached for the last 12 nm thick oxide without noticeably degrading leakage current ($\sim 10^{-7}$ A/cm^2 at 0.8 V). Moreover, these results show that rutile ATO layers are good candidates for future DRAM capacitors. They could replace more traditional dielectrics such as Al_2O_3, HfO_2, or ZrO_2, exhibiting lower k value ($k < 40$).[14–16]

IV. SUMMARY AND CONCLUSIONS

In conclusion, we have shown that aluminum doped titanium dioxide layers, grown by PEALD on *in-situ* oxidized ruthenium electrodes, have electrical properties that could meet the ITRS requirements for advanced DRAM capacitors. Dielectric constant around 70 has been obtained on this type of layers while keeping leakage current close to 10^{-7} A/cm^2. The aim of the next step on which we are currently working on is to enhance the stoichiometry of ATO layers by optimizing the *in-situ* PEALD oxidation process. A noticeable change in the leakage current should be expected.

TABLE I. Recap for k values for ATO (Al doped TiO_2) and TiO_2 obtained in different MIM structures.

MIM stack	TiO_2 on RuO_2/Ru	ATO 1/120 on RuO_2/Ru	ATO 1/90 on RuO_2/Ru	ATO 1/60 on RuO_2/Ru	TiO_2 on Pt	ATO 1/30 on Pt
Extracted k	107	73	60	53	39	31

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