

Sidewall roughness characterization of a 20 nm half pitch resist-core spacer patterning process



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Outline

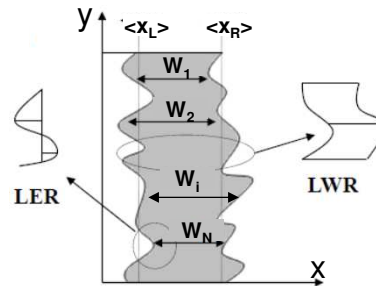
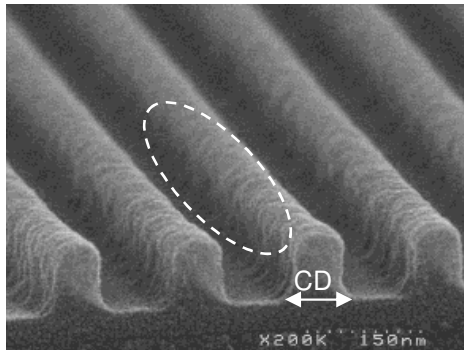
- Introduction

- Development of a spacer patterning process for the 20 nm node

- Characterization of the sidewall roughness



Sidewall Roughness issues



- Line Width Roughness

$$LWR = 3\sigma_{CD} = 3\sqrt{\frac{1}{N} \sum_{i=1}^N (W_i - \langle W \rangle_N)^2}$$

- Line Edge Roughness

$$LER_{Left} = 3\sigma_L = 3\sqrt{\frac{1}{N} \sum_{i=1}^N (x_{L,i} - \langle x_L \rangle_N)^2}$$

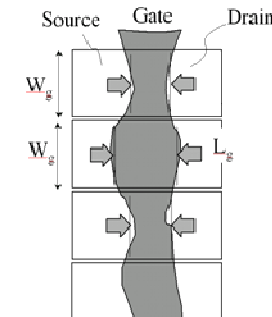
- ❑ Degradation of transistor electrical performances
Source of device variability and yield

- ❑ ITRS specifications : $LWR \sim 10\%$ of CD_{target}

- ❑ For Sub-20nm nodes, LWR and $LER < 2 \text{ nm}$

- Critical process parameter => **Roughness reduction issue**
- Resolution limit of measurement instruments => **Metrology tool issue**

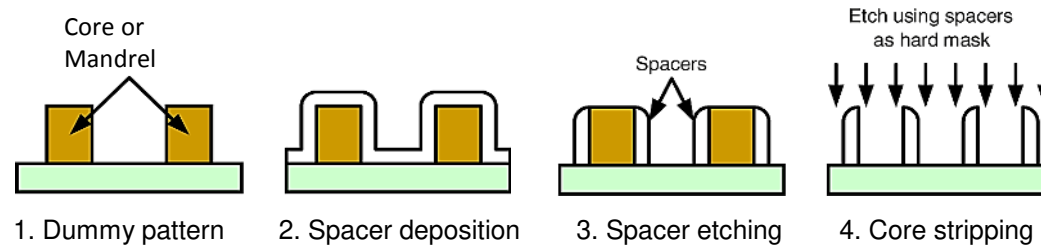
➔ Need of an accurate and insightful characterization of the sidewall roughness



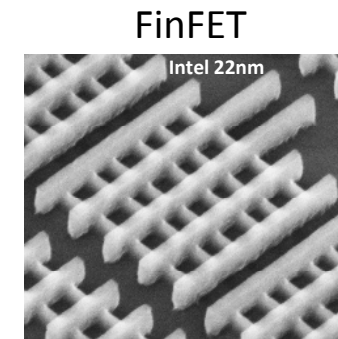
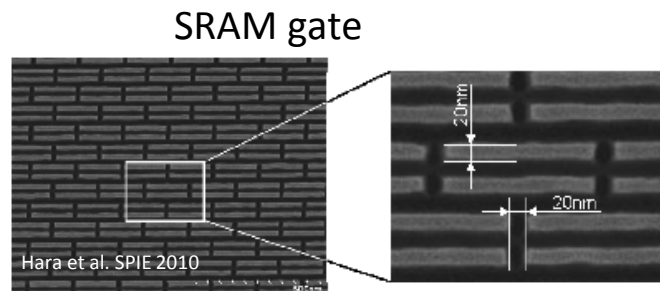


Self-Aligned Double Patterning : SADP

- A Nanopatterning lithography technique



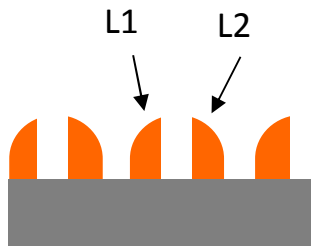
- Dense array of Lines\Spaces structures by pitch division
- Extension of the 193 nm optical lithography resolution limit
- HVM for memory and logic applications



- Candidate to the 10 nm node and beyond !



Problematic / Objectives



- Spacers are asymmetric by nature
- 2 populations of lines : L1 and L2
- When they are used as an etch mask, it can result in asymmetric profiles or LER

❑ **Evaluate the LWR and LER** of dense array of lines/spaces structures obtained with a **spacer patterning process** targeting a **20 nm half-pitch**

❑ **Power Spectral Density** method

- ➔ Unbiased LWR and LER measurements
- ➔ Spatial frequency analysis of the roughness



Outline

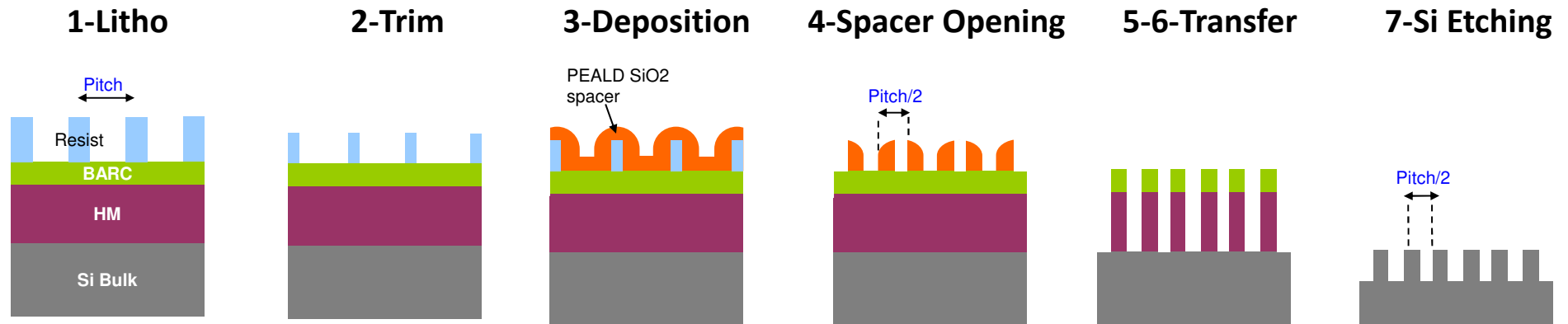
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Resist-core spacer patterning process flow



Spacer material is directly deposited on the resist lines

Challenge

- PR are thermally degradable
- CDV Spacers are not compatible

Solution : PEALD

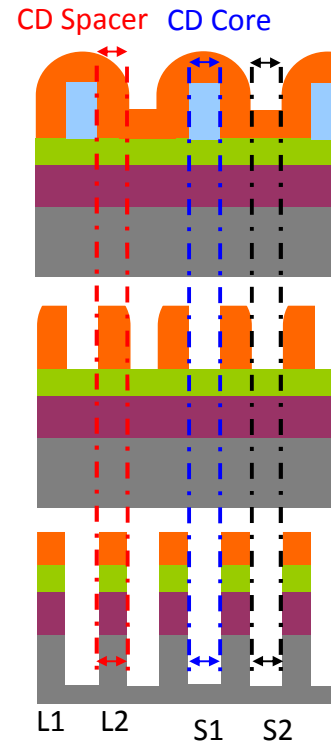
- Low-temperature deposition technique
- Highly Conformal and uniform film
- No loading effect

Benefits of this integration

- Simplified stack
- Less steps than HM approach
- Improved cost of ownership



Key parameters of the SADP process



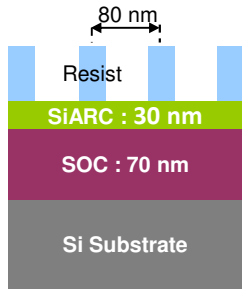
To control the width of the final lines and spaces, one can play with two parameters :

- CD Spacer → CD L1 and L2
 - CD Core → Space S1
- } → Space S2



20nm HP Optimized Process

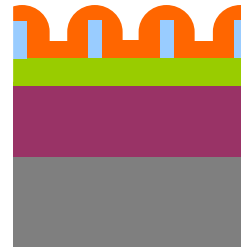
1-Litho



2-Trim



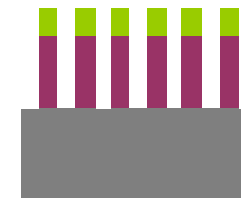
3-Deposition



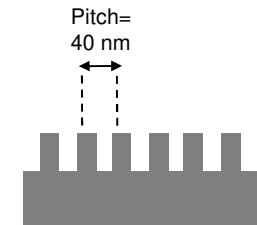
4-Spacer Opening



5-6-Transfer



7-Si Etching



Process
infos

E-beam
resist lines

Resist : HBr / O₂
CD_{trim} = CD_{theo} + 10nm

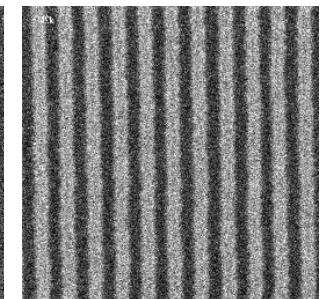
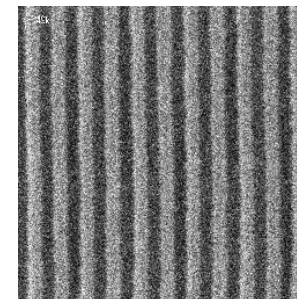
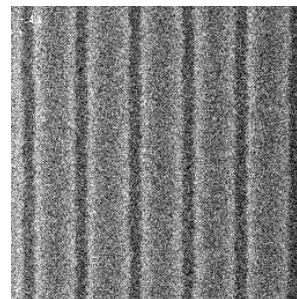
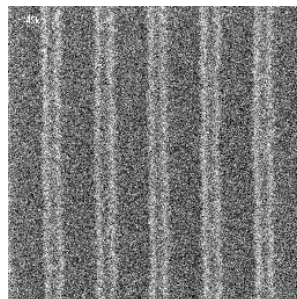
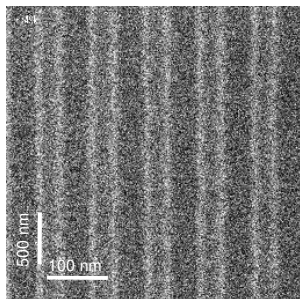
SiO₂ spacer by PEALD
20nm @ 50°C

Spacer : CF₄
Resist Stripping : O₂

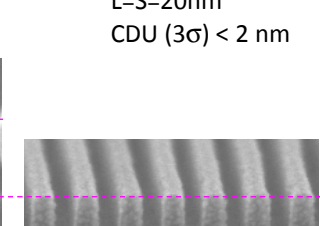
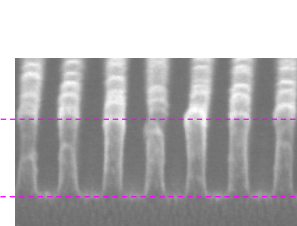
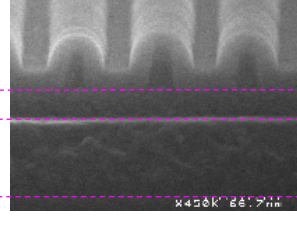
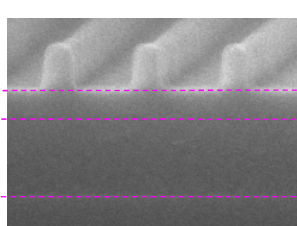
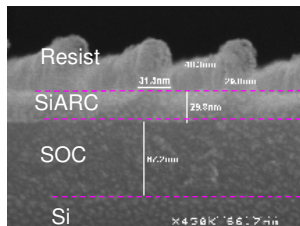
SiARC : CF₄ / CHF₃ / Ar
SOC : HBr / O₂

Si : SF₆ / CHF₃ / Ar
Spacer stripping : O₂

CDSEM



XSEM



L=S=20nm
CDU (3σ) < 2 nm

x150k 66.7um



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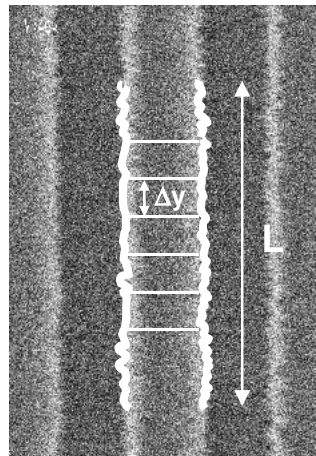
Sidewall roughness Characterization

- Unbiased LWR and LER measurements from CD-SEM images

$$\sigma_{\text{meas}}^2 = \sigma_{\text{real}}^2 + \sigma_{\text{noise}}^2$$

- Power Spectral Density method** → Spatial frequency analysis of the roughness

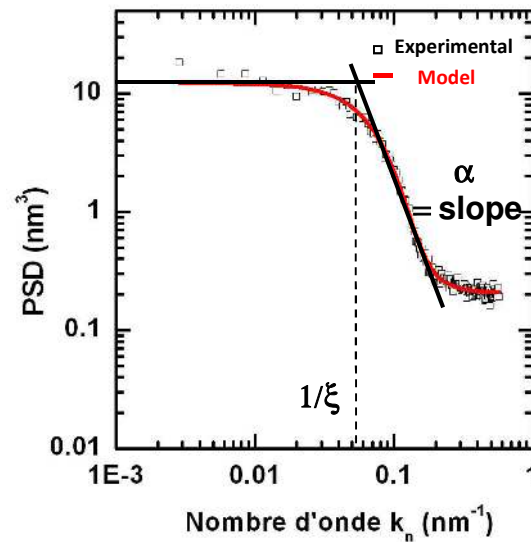
CD-SEM line segments (N^*)



$N^* > 200$
 $L = 2154 \text{ nm}$; $\Delta y = 5.4 \text{ nm}$



Average PSD calculation



Fit the PSD with FFT of ACF

$$\text{ACF} : R(u) = \sigma^2 e^{-|u/\xi|^{2\alpha}}$$

$$P_n = \frac{\Delta y}{2\pi N^*} \left[\sigma_{\text{real}}^2 \sum_{m=0}^{N-1} 2k_n \left| \frac{m\Delta y}{\xi} \right|^{2\alpha} \cos(k_n m \Delta y) (N-m) \right] + \frac{\Delta y}{2\pi} \sigma_{\text{bruit}}^2$$

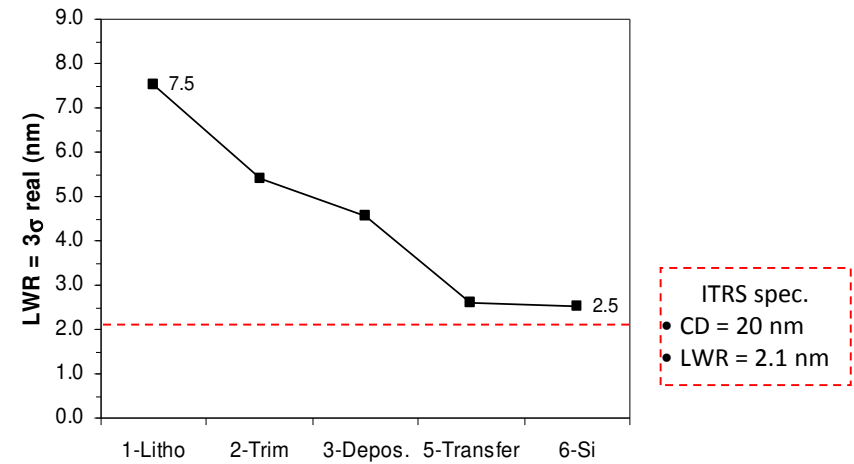
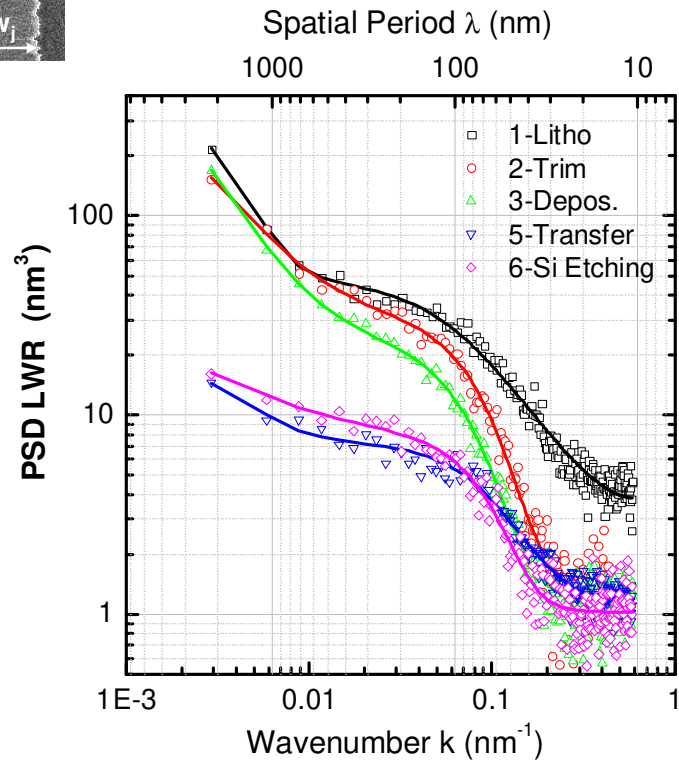
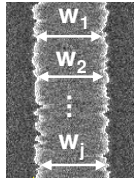
L. Azarnouche et al. JAP 2012

Extraction of

- σ_{real} : amplitude
- ξ : correlation length
- α : fractal exponent

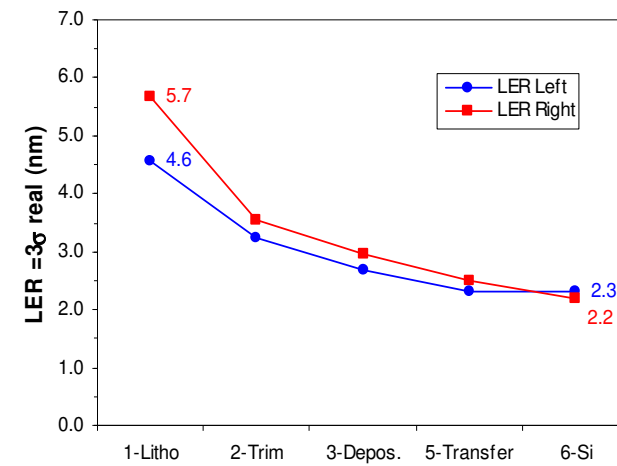
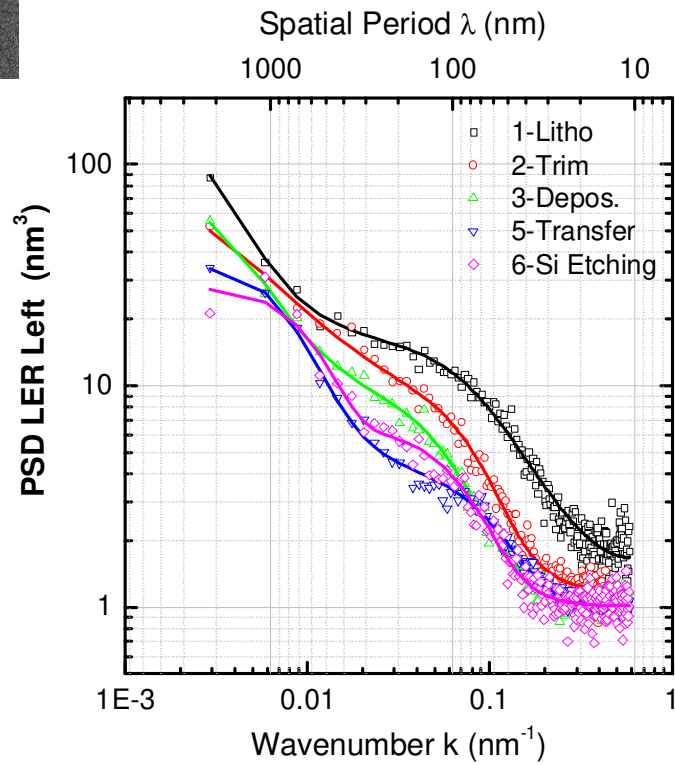
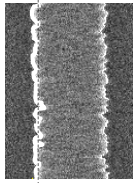


LWR





LER





Conclusion

- ❑ Demonstrated a successful integration of the resist-core spacer patterning process for 20 nm HP silicon lines
- ❑ Full description of the sidewall roughness evolution
 - PSD method
 - Unbiased LWR / LER measurements
 - Spectral analysis of the roughness
- ❑ Achieved specifications
 - L/S = 20/20 nm
 - CDU < 2 nm
 - LWR = 2.5 nm
 - LER ~ 2.3 nm

