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A CMOS Envelope Detector for Low Power Wireless Receiver Applications

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Abstract—Recent studies have shown that the power consumption of a wake-up receiver can be reduced by using an envelope detector as its first stage. Designing a low power envelope detector is challenging because of stringent requirements such as data rate, operating frequency, conversion gain and sensitivity. This paper describes the design of a 915 MHz envelope detector which uses a combination of active inductors and an input matching circuit to improve its conversion gain. The proposed design consumes 2 μ A of bias current, achieves a 37.8 dB of conversion gain, a sensitivity of -60 dBm and a data rate of 200 kb/s in a 0.13 μ m CMOS process.

I. INTRODUCTION

Recent studies have shown that by 2022, battery powered Internet of Things (IoT) devices will become ubiquitous. In order to minimize battery usage and prolong battery life, it will be necessary to develop energy efficient wake-up receivers that monitor wireless channel continuously and turn on the battery powered devices on demand.

Cheng and Chen have shown that the power consumption of wake-up receivers can be reduced significantly by using the direct RF detection approach, which eliminates the need for RF amplification and generation of LO frequency [1]. The envelope detector is the first stage of the RF front-end, and hence dominates the sensitivity of the wake-up receiver.

Similar to elementary amplifiers, envelope detectors can be categorized as common-drain (CD) [2], common-gate (CG) [3], and common-source (CS) [4] envelope detectors. Even though the CG envelope detectors can potentially achieve higher conversion gain than that of the CS envelope detectors, the CG envelope detectors have lower input impedance and result in lower passive gain when they are input matched [1].

There are two approaches for increasing the conversion gain of the envelope detectors in the literature. The first approach involves creating a passive gain from the antenna to the input of the envelope detector. Examples of the first approach include implementations using passive components such as a RF voltage transformer implemented on a PCB [5], a high-Q transformer with a lumped/distributed filter [6], and an inductive degeneration matching circuit [1]. The second approach involves increasing the output resistance of the envelope detector circuit through resistive feedback [6].

In this paper, the conversion gain of the envelope detector is enhanced by using a high-quality off-chip inductor that

resonates with the total capacitance seen at the input of the envelope detector to create a passive gain. The output resistance of the enveloped detector is increased by using an active inductive load as shown in Fig. 1. Different from the resistive feedback approach implemented in [6], the pole of the active inductor is determined by g_{ma} of M_a and is independent of M_1 which is responsible for the nonlinear operation of the envelope detector.

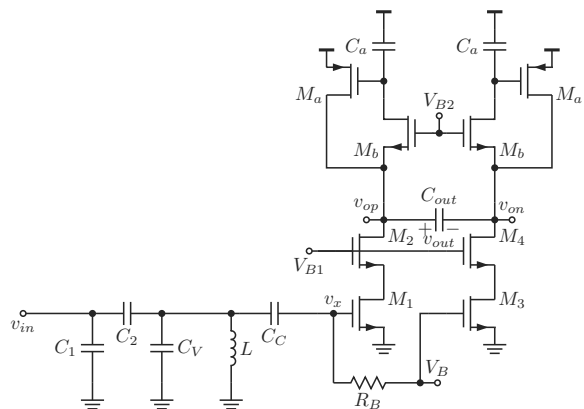


Fig. 1. An envelope detector with passive gain and active inductive load.

Compared to the envelope detector described in [7], the proposed envelope detector increases the conversion gain by 67.5 dB, achieves a sensitivity of -60 dBm while consuming power at a level comparable to that of previously reported envelope detectors ([1] and [5]).

Section II reviews the fundamentals of a common-source envelope detector. Section III describes the process of designing the input matching circuit and the active inductive load. Section IV summarizes the simulation results.

II. FUNDAMENTALS

The gain of the envelope detector in Fig. 1 is enhanced by a combination of passive gain achieved through input matching (via C_1 , C_2 , C_V , and L) and an active inductance load implemented via C_a , M_a and M_b . The gain of the envelope detector passive gain (G_v) can be computed as

$$G_v = G_{v,match}G_{v,ED}, \quad (1)$$

where $G_{v,match}$ is the passive gain of the input matching network and is defined as v_x/v_{in} . The design of the input

matching network will be discussed in Sec. III-A. $G_{v,ED}$ is the conversion gain of the envelope detector without input matching and is defined as $G_{v,ED} = v_{out}/v_x$.

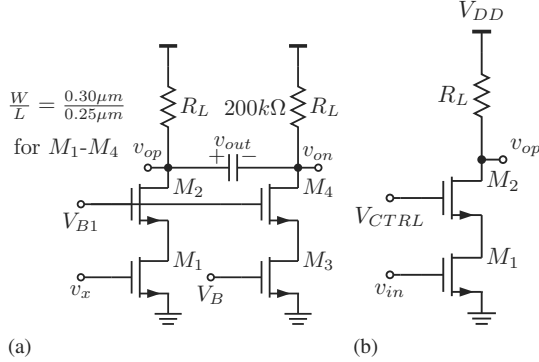


Fig. 2. (a) Simplified schematic of the envelope detector shown in Fig.1. (b) Equivalent circuit for the envelope detector in Fig. 2a.

The basic operation of the envelope detector circuit without passive gain can be understood by examining the simplified schematic in Fig. 2a [4]. The modulated signal at v_x is down-converted to the baseband frequencies through the nonlinearity of M_1 . The output is taken differentially in order to remove the DC component from v_{op} [4]. [7] shows that the conversion gain of the envelope detector is approximately

$$G_{v,ED} \approx \frac{R_L}{2} g_{m2,1} v_m, \quad (2)$$

where v_m is the magnitude of the voltage at v_x and $g_{m2,1}$ is the second order linearity of M_1 .

Equation 2 shows that G_v is proportional to v_m . Indeed, Fig. 3a confirms that, for $v_m \leq 100$ mV, G_v is proportional to v_m . Equation 2 was obtained by approximating the drain current (i_{ds}) by a two-dimensional Taylor series. The approximation becomes less accurate as v_m increases in magnitude [8]. As v_m exceeds 100 mV, G_v is reduced as the Taylor series approximation becomes less accurate.

Ou and Ferreira have shown that $g_{m2,1}$ increases with the g_m/I_D of M_1 [7]. Indeed, Fig. 3b shows that $i_{ds,2nl}$, which represents the second order distortion of i_{ds} , is increased as g_m/I_D of M_1 is increased. The conversion gain can therefore be increased by increasing the g_m/I_D of M_1 at the expense of reducing the transit frequency of M_1 , and hence the frequency range of the envelope detector.

In order to allow the envelope detector to operate at RF frequencies, L_1 is minimized in order to increase f_T (Fig. 3c). The minimum L_1 is ultimately limited by a combination of bias current, the increasing current density (Fig. 3d) as L_1 is reduced, and the minimum width permitted in a design kit [7].

$G_{v,ED}$ is proportional to R_L and should be maximized in order to maximize the conversion gain. Section III-B describes the design of an active inductor load to increase R_L without using passive resistors.

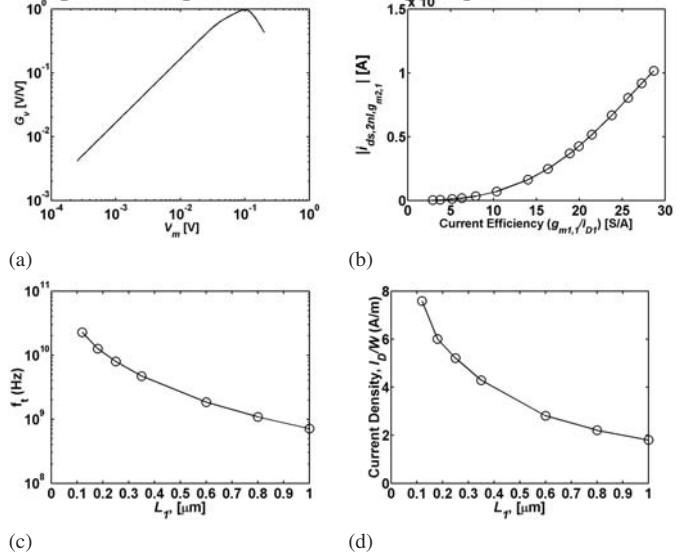


Fig. 3. (a) Conversion gain as a function of v_m . (b) Contribution of $g_{m2,1}$ to $i_{ds,2nl}$. $i_{ds,2nl}$ represents the second order distortion of i_{ds} . (c) f_T as a function of L_1 . (d) current density plotted as a function of L_1 . $g_m/I_D = 20$ S/A. $L_1=250$ nm, $V_{DS}=0.6$ V and $V_{SB}=0.0$ V.

III. DESIGN

A. Input Matching

The input matching circuit is designed to provide adequate return loss (S_{11}) and maximal $G_{v,match}$. C_C is a coupling capacitor. R_B allows the DC voltage at v_x to be defined and is maximized in order to maximize $G_{v,match}$. L is a high quality off-chip inductor chosen to resonate at 915 MHz. Though not shown, the wirebond parasitics and the package parasitics associated with an open-cavity ceramic package are critical and are included in the design of the input matching network. C_2 is a series capacitor introduced to rotate the impedance along constance resistance circle in the counter-clockwise direction on the impedance Smith chart. C_1 is a shunt capacitance introduced in order to rotate the admittance along the constance conductance circle in the clockwise direction on the admittance Smith chart. C_v is a varactor which allows the resonant frequency to be tuned via a tuning voltage. Figure 4a shows that a voltage gain ($G_{v,match}$) of 17.5 V/V (24.8 dB) can be obtained without consuming power. Figure 4b shows a return loss less than -20 dB at 915 MHz.

Compared to [1], which uses inductive degeneration to implement the input matching network with a quality factor of 4.2 and increases the conversion gain by Q^2 or 17.64 V/V, the input matching network described in Fig. 1 achieves a comparable passive voltage gain without using an on-chip inductor, even though it requires the use of an off-chip inductor.

B. Active Inductor Load

It is desirable to maximize R_L in order to maximize $G_{v,ED}$. [1] and [6] used resistive feedback to increase the output resistance. Large pseudo-resistors of values equal to 80 M Ω and 100 M Ω were implemented ([1] and [6], respectively). The aspect (W_1/L_1) ratio of M_1 plays an important role in determining transconductance of M_1 , the conversion gain, and the location of the pole and the zero in the output resistance

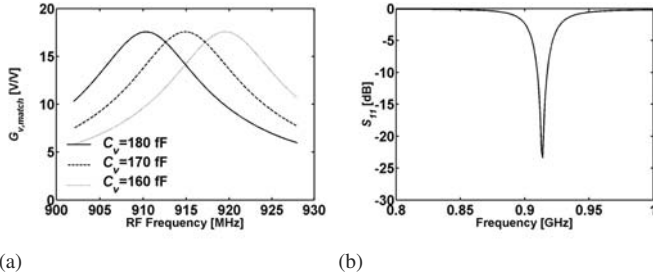


Fig. 4. (a) $G_{v,match}$ as a function of varactor capacitance. (b) Return loss of the input matching circuit in Fig. 1.

[6], as well as the suppression of the low-frequency flicker noise [1].

In contrast to [1] and [6], the design of the active inductor load in Fig. 1 is decoupled from that of M_1 , the transistor responsible for the nonlinear operation of the envelope detector. It can be shown via small signal analysis that the input impedance of the active inductive load in Fig. 5a is

$$Z_{in} = \frac{1}{g_{ma}} \frac{1 + s/\omega_z}{1 + s/\omega_p} \quad (3)$$

where $1/g_{ma}$ represents the resistance at DC. ω_z is $1/(R_1C_1)$ and $\omega_p = g_{ma}/C_1$. g_{ma} is determined by the sizing of M_a and is independent of the g_m/I_D of M_1 , which controls the second order nonlinearity of M_1 .

In order to create an approximately 40 dB increase in conversion gain, ω_p/ω_z is chosen to be 100. R_1 and C_1 are chosen by assuming that the Manchester coded baseband has a bit rate of $f_{bitrate} = 200$ kb/s, and that the lowest frequency component is $f_{bitrate}/4$, the highest frequency component is $3f_{bitrate}/2$ [5], and f_p is chosen to be $f_{bitrate}/20$. R_a is replaced with M_b biased in the triode region in order to provide tunability and conserve area.

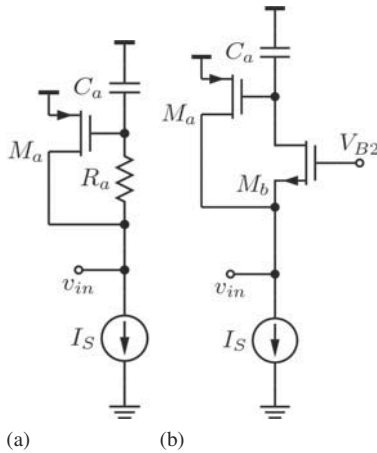


Fig. 5. (a) Implementation of an active inductive load. (b) R_a replaced with M_b biased in the triode region.

IV. SIMULATION RESULTS

Figure 6 shows the conversion gain (G_v) including the passive gain as a function of the output frequencies. The amplitude of v_{in} is 1 mV. V_{B2} is 0.9 V. G_v is approximately 80

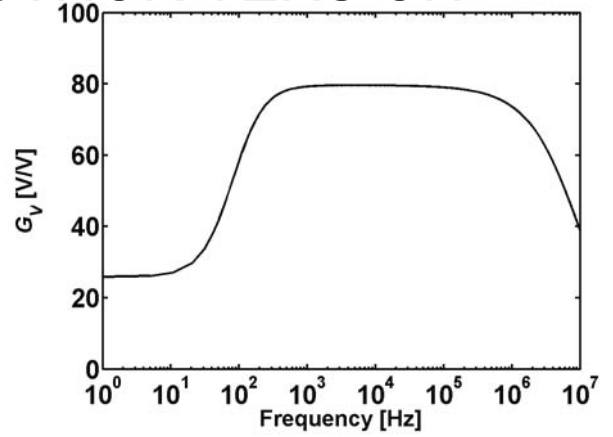


Fig. 6. Simulated G_v as a function of the output frequencies.

V/V between 50 kHz and 300 kHz, the lowest frequency component and the highest frequency component of the Manchester baseband signal.

Figure 7 shows the simulated conversion gain as a function of $V_{in,m}$. The carrier frequency is 915 MHz. The conversion gain is evaluated at 200 kHz at v_{out} . The conversion gain (G_v) with input matching and active inductive load is compared with $G_{v,ED}$ reported in [7]. At $v_{in,m} = 1$ mV, $G_{v,ED}$ is 0.033 V/V (-29.6 dB) and G_v is 78.4 V/V (37.8 dB) with input matching and active inductive load. Compared to [7], the proposed design improves the conversion gain by approximately 67.4 dB. Even though the nonlinearity is increased as a result of increased G_v , nonlinear G_v is less of a concern for envelope detector first architecture where the input voltage is generally small.

The noise factor (NF_{ED}) of the envelope detector can be calculated as

$$NF_{ED} = 1 + \frac{N_{o,ED}}{N_s G_v^2} \quad (4)$$

where $N_{o,ED}$ is the output noise of the envelope detector, N_s

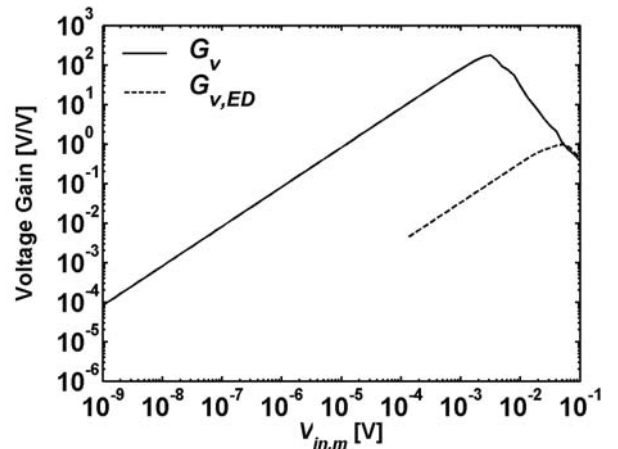


Fig. 7. Simulated voltage gain as a function of the input amplitude. G_v is the conversion gain with the input matching and the active inductor load. $G_{v,ED}$ is the conversion gain without the input matching and the active inductor load.

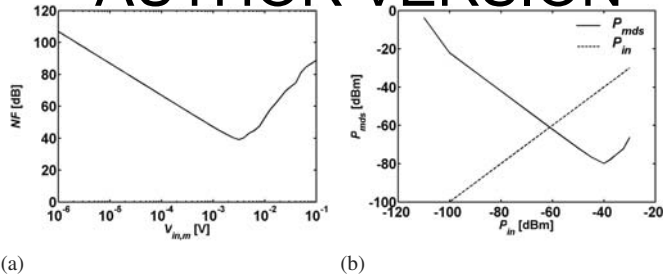


Fig. 8. (a) Noise figure of the envelope detector in Fig. 1.(b) Using simulated $P_{m,ds}$ and P_{in} to determine the envelope detector sensitivity.

is the noise of the source resistance. NF_{ED} is a function of $V_{in,m}$ since G_v is a function of $V_{in,m}$. Figure 8a confirms that the noise figure at 200 kHz is degraded as $V_{in,m}$ is reduced.

The minimal detectable signal $P_{m,ds}$ is a function of NF_{ED} .

$$P_{m,ds} = NF_{ED} + 10 \log_{10} B - 174 + SNR_{min}, \quad (5)$$

where B is the envelope detector bandwidth, SNR_{min} is the minimum signal-to-noise ratio required for reliable detection. SNR_{min} is 12 dB for a Bit Error Rate (BER) of 0.001 for OOK demodulation [1]. [1] shows that by plotting $P_{m,ds}$ and P_{in} , the sensitivity of the envelope detector can be determined by determining the input power at which $P_{m,ds}$ intersects with P_{in} as shown in Fig. 8b. With a total DC bias current of 2 μ A and a supply voltage of 1.2 V, the sensitivity for the 915 MHz envelope detector is -60 dBm.

A Monte Carlo simulation is run in order to better understand the robustness of the design. A total of 1000 simulations are run. G_v is determined from each simulation and recorded. Figure 9 shows the occurrences as a function of G_v . The average of G_{v5} is 76.2 V/V. The standard of deviation is 20.6 V/V.

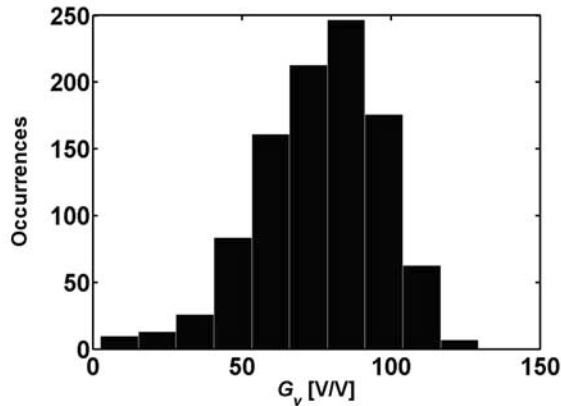


Fig. 9. Occurrences as a function of G_v .

Table I shows a comparison between envelope detectors with comparable data rates in the GHz range. Table I shows that the envelope detector in Figure 1 achieves a sensitivity of -60 dBm while consuming power comparable to that of previously reported envelope detectors ([1] and [5]). [9] reported a 22 μ W envelope detector with a data rate of 2 Mb/s and a sensitivity of -60 dBm. Even though power consumption is

generally reduced as the data rate is reduced, the exact power consumption at 100 kb/s of data rate cannot be determined from [9] and is included for completeness.

TABLE I. PERFORMANCE COMPARISON.

	this work	[1]	[9]	[9]	[5]
Carrier Frequency	915 MHz	2.4 GHz	2.4 GHz	2.4 GHz	2.45 GHz
Process	130 nm	180 nm	65 nm	65 nm	130 nm
Supply	1.2 V	0.8 V	1.0 V	1.0 V	1.0 V
Power	2.4 μ W	2.4 μ W	22.0 μ W	N/A	1.0 μ W
ED Sensitivity	-60 dBm	-50 dBm	-60 dBm	-65 dBm	-47 dBm
Data Rate	200 kb/s	200 kb/s	2 Mb/s	100 kb/s	200 kb/s

V. CONCLUSION

The design of an envelope detector which uses an input matching circuit and active inductive loads to improve its conversion gain is discussed in this paper. With a total DC bias current of 2 μ A and a supply voltage of 1.2 V, the 915 MHz envelope detector achieves a conversion gain of 37.8 dB and a sensitivity of -60 dBm at 200 kb/s of data rate in a 0.13 μ m CMOS.

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