Electro-thermal Model of a Silicon Carbide Power MOSFET

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Abstract. This paper proposes an electro thermal model for power silicon carbide (SiC) MOSFET based on the EKV MOSFET structure. The thermal dissipation is modeled as an RC Network. The model is developed for the SiC MOSFET C2M0025120D CREE (1200V, 90A) and integrated in the Psim, Saber and Pspice simulation software libraries for prototyping. The simulation curves are compared with the manufacturers' data-sheet.

Keywords: SiC MOSFET, Electro-thermal Model, Psim, Saber, Pspice Model

1 Introduction

The use of a silicon carbide (SiC) for industrial manufacturing power components such as the MOSFET makes it possible to have high performance which satisfy advanced application problems (time response, environmental stresses, heating, power loss reduced). These constraints affect the electrical behavior of the electronic components by the coupling between the electrical and the thermal behaviors. In high power applications, Silicon (Si) circuits are more and more replaced by SiC MOSFET devices [1]. A first serie of such devices has been proposed by CREE, like the SiC MOSFET C2M0025120D (1200V, 90A) [2]. Simulations are very important in electric systems design. Therefore a good suitable simulation models is required in order to show the faisability of the complex systems [3, 4].

In this paper, we propose an electro-thermal model based on the EKV MOSFET scheme [5, 6] for a SiC MOSFET C2M0025120D (1200V, 90A) proposed by CREE. The model is implemented in Psim, Saber and Pspice softwares to allow easy development of applications. For validation, the simulation curves are compared to the manufacturers' experimental data (curves of data sheets). The results show that the proposed model is more precise compared to the literature existing models.

2 SiC MOSFET Electrothermal Model

2.1 Nomenclature

V_S, V_G and V_D	Source, Gate and Drain Voltages
L_D	Drain inductance
L_G	Gate inductance
L_S	Source inductance
R_G	Gate Resistance
C_{GS}	Gate-Source Capacitor
C_{DS}	Drain-Source Capacitor
C_{GD}	Gate-Drain Capacitor
R_{DSon}	On state MOSFET resistance
V_p	Pinch voltage
U_T	Thermodynamic voltage
g_m	MOSFET Transconductance
K_s	Slope Factor of drain source current variation
λ	Parameter for channel length modulation
α and n	Parameters of the triode region
V_{th}	Transistor gate Threshold Voltage
T_c	Case temperature
P_P	Power loss dissipated
T_j	MOSFET Jonction temperature
F	The MOSFET commutation frequency
Δt	MOSFET commutation period

2.2 Electric Model

The electrical model of a SiC MOSFET ($25m\Omega$,$1200V$ and $90A$) proposed here is based on the EKV's one. The power losses are analysed to estimate and take into account their effect as shown in the equivalent scheme of Fig. 1. V_S, V_G et V_D are respectively the Source, Gate and Drain voltages. It includes 3 parasitic inductances (connected in series with the transistor electrodes L_G, L_D, L_S) to describe the behaviour at high frequencies and the commutation losses. The resistance R_G estimates the gate losses. These inductances and the resistances are used to estimate the power losses during the switching [7–9]. The different variables and parameters (V_{DS}, I_{DS}, R_{dson},...) of the model vary also in function of the junction temperature [10].

In this model, we used parameters from the datasheet and the others from an optimization (comparison) that was performed by Saber, Psim and PSpice. Fig. 1 shows the EKV deduced scheme for a SiC MOFET developed under the softwares. The EKV model is based on mathematical expressions which accounts for a MOSFET operation in three regions. It is composed of two current sources G1 and G2. For interpolation between these regions of operation, a linear combination of logarithmic functions is used by EKV.

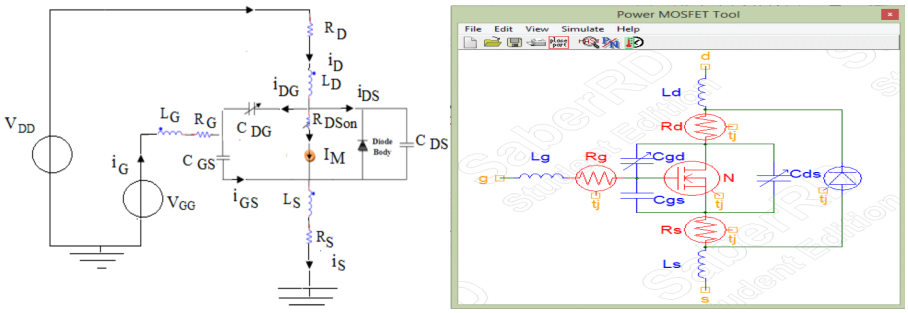


Fig. 1. Electric model of the SiC MOSFET (C2M0080120D) in Saber Software

The specific current is $I_{s_0} = 2.U_{th}^2.K_s.g_m$. The Drain-Source current (I_{DS}), in the EKV MOSFET model [7, 8], is defined by equation 4, as the difference beetwen the direct I_{G1} (2) and the reverse one I_{G2} (3) [6].

$$I_M = I_{G1}(V_p - V_S) - I_{G2}(V_p - V_D) \tag{1}$$

$$I_{G1} = I_s.g_m.\left[Ln(1 + exp\frac{V_p - V_s}{2V_{DS}})\right]^2 \tag{2}$$

$$I_{G2} = I_s.ft.\left[Ln(1 - exp\frac{V_p - V_D}{2})\right]^2 \tag{3}$$

$$I_M = 2\lambda U_{th}^2 K_s g_m((L_n(1 + e^{\frac{V_p - V_s}{2V_{DS}}}))^2 - ft(L_n(1 - e^{\frac{V_p - V_D}{2}}))) \tag{4}$$

where g_m is the transconductance, K_s is the slope factor, $V_p = \frac{(V_G - U_{th})}{K_s}$ the pinch voltage with U_{th} the thermodynamic reference voltage and ft the internal thermal voltage. This model of Fig. (1) can then be used for simulation and prototyping of any application using this SiC MOSFET into softwares like Saber, Pspice, Psim (see section 3) or Matlab/Simulink (see [11]). The electric equivalent scheme can be completed by electric equations to allow any kind of its numerical simulation.

In a second step, we can consider and include, to this model, the parameters temperature dependance. The accuracy of the proposed model will be enhanced by modeling of the influence of temperature on electrical parameters.

The variation of the junction temperature, leads to parameters variation which can be described as follows, where $\vartheta = -8.5mV/°K$. The variations included in the previous model show that the model is Non Linear and Time Varying (NLTV).

$$\begin{aligned} V_{GS(th)}(T_J) &= V_{GS(th)}(300°C) + \vartheta.(T_j - 300°C) \\ g_m(T_j) &= g_{m(300°C)}(\tfrac{T_j}{300})^{-1.5} \\ R_{DSON}(T_j) &= R_{DSON(300°C)}(1 + \tfrac{\alpha}{100})^{(T_{j-300})} \end{aligned} \tag{5}$$

It remains now to describe the temperature variations by a dynamic model which takes into account the MOSFET operation and convert the power losses in heating the component. Thermal dynamic behaviour is obtained using the heat equation and the finite element method.

2.3 Thermal Model

The electro- thermal coupling between the electrical parts and the thermal parts is produced by the power losses P_P dissipated during normal operation. This power can be estimated by the following equations [8, 9]:

$$P_P = R_{DSon}(T).i_{DS}^2 + (0.25.\Delta t.F.V_{DS}.i_{DS}) \tag{6}$$

We have used the Finite Element Method (FEM) based on an RC Cauer network. As also used in Pspice simulation, we have considered 14 cells of (R, C) equivalent components (Fig.(2) [9]. It gives a very good global approximation of the thermal behaviour going from the MOSFET junction temperature T_j to the ambiant air temperature T_a (assumed to 25°C), through the case (T_c) (package and the thermal dissipation radiator, T_r) (see Fig.(2)).

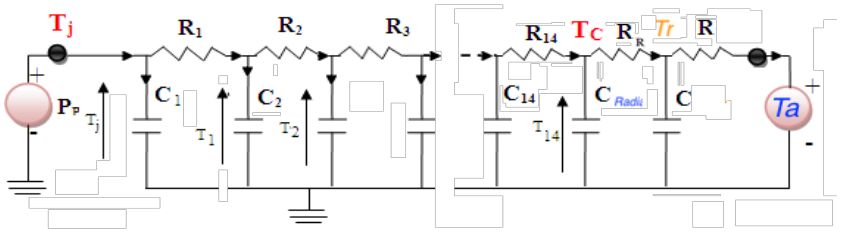


Fig. 2. Thermal model of SiC MOSFET

The RC layers describing the heat flow has as input power loss to be dissipated as an equivalent current source and as second output the ambiant temperature T_a represented by voltage source (see Fig. 2). The ouptut of interest is of course the junction temperature T_j. A $V_a = 25V$ continuous voltage source correspond to the ambiant air temperature $T_a = 25°C$. The flow of the dissipated power losses is represented by an input current source (P_P). The junction temperature T_j is imposed trough the thermal impedance Z_{TH} between the MOSFET junction and the ambiant air and the dissipated power losses (P_P) by the heat transfer equation $Z_{TH} = \sum_{i=1}^{14} R_i * (1 - exp\frac{-t}{R_i C_i})$

$$T_j = T_a + P_P * Z_{TH} \tag{7}$$

The thermal MOSFET behaviour, if we consider the thermal state vetor $X_T = [T_j,\ T_1, ..., T_{14},\ T_r]^T$ can be expressed as

$$\begin{cases} T_1 = T_j - R_1\left(P_P - C_1\frac{dT_J}{dt}\right) \\ T_2 = T_1 - R_2\left(P_P - C_1\frac{dT_J}{dt} - C_2\frac{dT_1}{dt}\right) \\ T_3 = T_2 - R_3\left(P_P - C_1\frac{dT_J}{dt} - C_2\frac{dT_1}{dt} - C_3\frac{dT_2}{dt}\right) \\ T_4 = T_3 - R_4\left(P_P - C_1\frac{dT_J}{dt} - C_2\frac{dT_1}{dt} - C_3\frac{dT_2}{dt} - C_4\frac{dT_3}{dt}\right) \\ : : : : : : : : : : : : : : : : : : \\ T_N = T_{N-1} - R_N\left(P_P - C_1\frac{dT_J}{dt} - C_2\frac{dT_1}{dt} - ... - C_N\frac{dT_{N-1}}{dt}\right) \\ T_r = T_{N+1} = T_N - R_R\left(P_P - C_1\frac{dT_J}{dt} - ... - C_N\frac{dT_N}{dt}\right) \\ T_a = T_r - R\left(P_P - C_1\frac{dT_J}{dt} - ... - C_{N+1}\frac{dT_{N+1}}{dt} - C\frac{dT_r}{dt}\right) \end{cases} \tag{8}$$

3 Simulations Tests and Model Validation

The developed model has been implemented in Saber, Pspice and Psim softwares and compared to the experimental curves presented by the SiC MOSFET data sheet for its validation.

3.1 Saber Simulation Model

The proposed model is then implemented under Saber software (see Fig. 1). The use of Power MOSFET Tool and the Diode Tool proposed in Saber allow us to extract the SiC MOSFET parameters and get curves using fitting to optimize the estimation errors. The verification of the output characteristic $I_{DS} = f(V_{GS})$ with the Saber optimized simulation model, for $T_j = 25°C$ and $T_j = 150°C$ as proposed and developed in this work, is shown in Fig. 3.

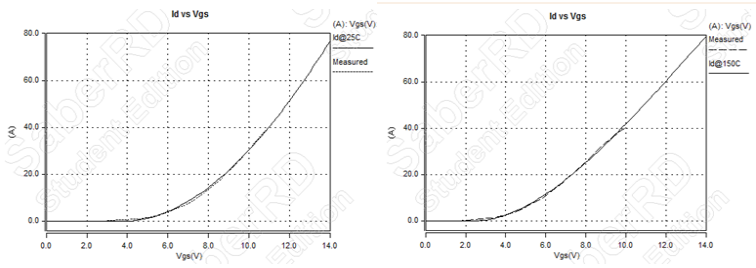


Fig. 3. I_D current versus V_{ds}

The Fig. 3 compares the variation of the current I_{DS} as a function of the voltage V_{GS} for a voltage $V_{DS} = 20V$ and a junction temperature of 25 °C (left curve) and 150°C (right) to the curves got from the datasheet (dotted line).

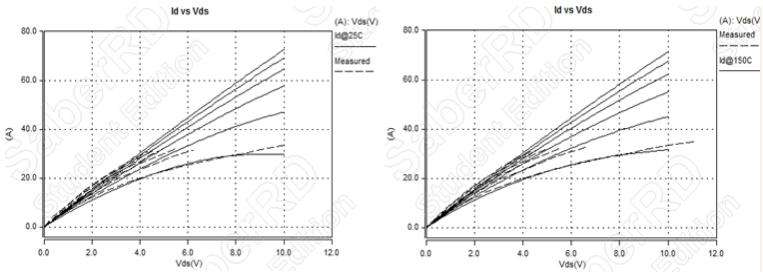


Fig. 4. Id current in function of V_{DS} for different V_{GS} values

The Fig. 4 compares the variations of the current I_{DS} versus V_{DS} for different V_{GS} values and the same junction temperature of 25 °C (left curve) and 150°C (right) to the curves got from the datasheet (dotted line). Among this experiment we got respectively for 25°C and 150°C, a threshold voltage $V_{th} = 3.808V$ and $V_{th} = 2.313V$, Drain resistance $R_d = 0.1\Omega$ and $R_d = 0.0942\Omega$, Source resistance $R_s = 0.01033\Omega$ and $R_s = 0.0173\Omega$ and Gate resistance $R_g = 4.6\Omega$ and $R_g = 4.6\Omega$ (respectively).

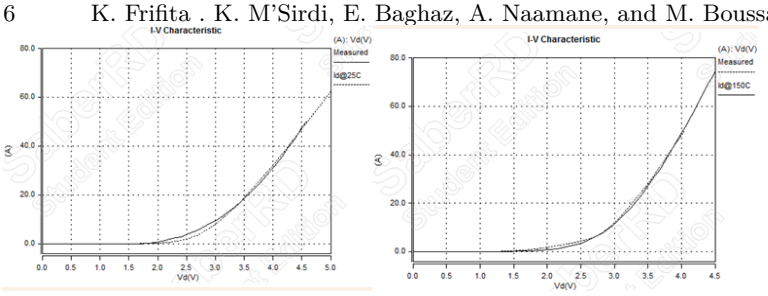


Fig. 5. I-V Charasteristic for $T_j = 25°C$ and $T_j = 150°C$

The current versus output voltage (I-V) characteristics of the integrated diode has also been compared, using Diode Tools of Saber software. Results are represented in Fig. 5. The capacitance curves of datasheet have also been fitted to get the MOSFET model parameters. For two V_{DS} values V1 and V2 we got the parameters values summarized in Fig. 1.

Parameters	Significance	Values
Crrs0	Max Reverse transfert Capacitance	780pF
COSS0	Maximal output capacitance	1350pF
Ciss0	Maximal input capacitance	1775pF
V1	$V_DS = V_1$	1V
V2	$V_DS = V_2$	16,3V
Crss1	Reverse capacitance at VDS =V1	247pF
COss1	Output capcitance at VDS = V1	767,5pF
Crss2	Reverse capacitance at VDS =V2	25,2pF
COSS2	Output capacitance at VDS = V2	363,1pF

Table 1. MOSFET estimated Parameters

A comparison of the Gate charge, Gate threshold voltage, ON-state resistance and transconductance are given in Table 6. We then got :
- A very good agreement between the simulations represented by continuous lines and those of datasheet represented by a points,
- For gate voltages V_{GS} lower than 3.8V, the MOSFET is switched OFF because the condition V_{GS} is not greater than or equal to that transistor threshold V_{th}. Beyond 3.8V, the MOSFET starts to operate and the current I_{DS} gradually increases.

3.2 PSpice simulation Model Validation

Several simulation results obtained, using the model implemented under the Pspice software, were compared with those of the datasheet of the CREE's

Table 2-1 Verification result of the Saber model of SPW20N60C3 MOSFET.

	Data sheet	Model simulation result	Error
Gate charge plateau voltage	5.5 (V)	5.21 (V)	5.3%
Q_{gs}	11 (nC)	10 (nC)	9.1%
Q_{gd}	33 (nC)	34 (nC)	3.0%
Q_g	87 (nC)	85 (nC)	2.3%
Threshold voltage	2.1 (V) minimum 3.0 (V) typical 3.9 (V) maximum	3.1 (V)	
On-state resistance	0.16 (ohm)	0.14 (ohm)	12.5%
Transconductance	17.5 (S)	18.8 (S)	7.4%

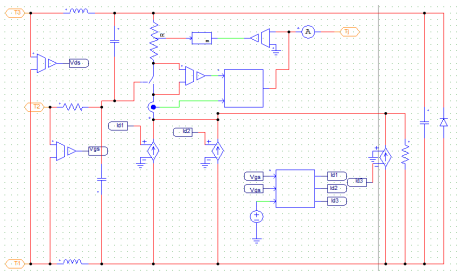
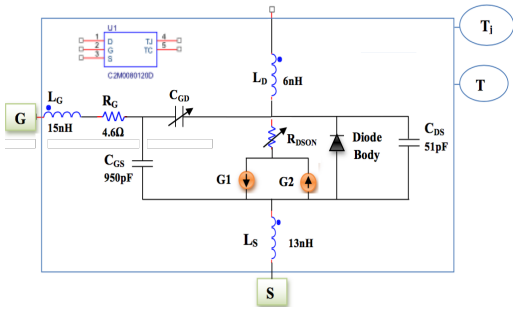


Fig. 6. Comparative results and the Psim model

MOSFET [9]. The model scheme is given in Fig. 7 with the parameters estimated (under Pspice tests) from datasheet. We can note that the resistances R_d and R_s are small and have been neglected.



Parameters	Values
L_D	$6nH$
L_G	$15nH$
L_S	$9nH$
R_G	$4,6\Omega$
C_{GS}	$950pF$
C_{DS}	$51,93pF$
C_{GD}	$161,7pF$

MOSFET Characteristic

Fig. 7. Pspice Sic MOSFET C2M0080120D and Parameters

The Fig. (8) below show good behaviour of the electrothermal model proposed in this work. Fig. 8 represents the variation of the Drain-Source current (I_{DS}) as a function of the voltage at the output of the SiCMOSFET (V_{DS}) for different Grid-Source voltage values (V_{GS}) and a temperature of 25°C. It appears that there is a very good agreement between the simulation results, represented by lines, and those of datasheet, represented by poinctual bars.

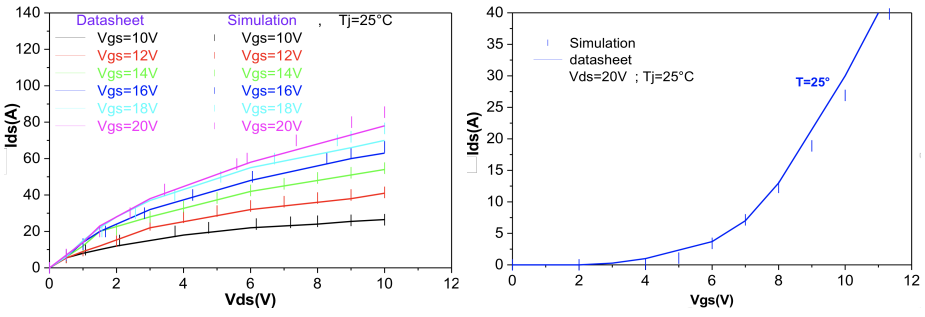


Fig. 8. Variation of I_{DS} current versus V_{DS} for different values of V_{GS} and Drain-Source current Ids versus V_{GS}

Fig. 8 the variation of the current I_{DS} as a function of the voltage V_{GS} for a voltage $V_{DS} = 20V$ and a temperature of 25 ° C. We can note a very good agreement between the simulation results represented by continuous lines and those of detasheet represented by dotted bars. For voltages $V_{GS} < 4V$, the MOSFET is not controlled because the condition $V_{GS} < V_{th}$, the treshold condition is not verified. Beyond 4V, the transistor start to operate and the current I_{DS} gradually increases. Fig. 9 show the thermal effect on the Drain-Source resistance (R_{DSon}) compared to the datasheet characteristic, for $I_{DS} = 50A$ and $V_{GS} = 20V$. It appears that the electro thermal model developed in this work has a high accuracy and is close to actual operating (datasheet) up to very high temperatures (150°C).

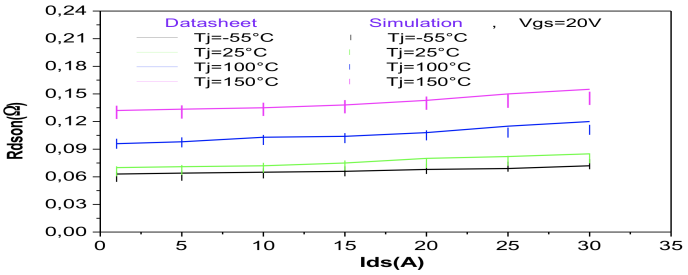


Fig. 9. R_{DSon} Variations in function of the junction temperature

In summary, the electric model developed, under Pspice, during this work has considerable precision. This allows us subsequently to use this simulation model in the power electronics to clearly show these performance and advantages over silicon transistors. Although the CREE model fairly accurately represents the evolution of R_{DSon} in function of the junction temperature, it has some discrepancy with the datasheet. However, with our simulation model, it is easy to see a better superposition between the two curves by adjusting the coefficients mentioned in Table 1.

3.3 Psim simulation Model Validation

The proposed model is implemented in Psim software as described by the Fig. (6). The improvements in the simulation model need additional adjustments of the device characteristics and computation parameters such as variable simulation step size which is used for the convergence rapidity. For our SiC MOSFET, we use the parameters that have been extracted from the data sheet (see table 7). The Drain and Source resistances have been neglected. The Fig. 10 shows the variation of I_{DS} in function of the drain-source voltage V_{DS}. It compares the Drain-Source current (I_{DS}) versus the MOSFET output voltage (V_{DS}) for several Gate-Source voltages (V_{GS}) under a temperature of 25°C. The simulated characteristics are then compared to the data sheet values and curves. Simulation results (continuous lines) are in good agreement with the data sheet values (dots).

The Fig. 10 shows the variation of I_{DS} in function of the Gate-Source voltage V_{GS} for the junction temperatures of 25°C and 150°V. We can note that for

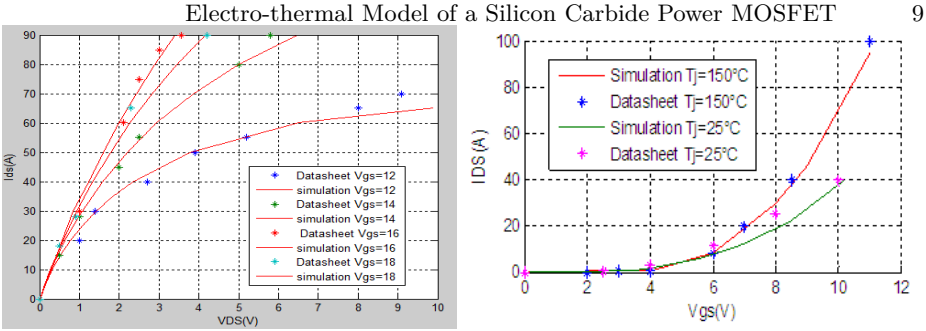


Fig. 10. I_{DS} versus V_{DS} for different V_{GS} values and I_{DS} versus V_{GS} for T_j 25°C and 150°C

V_{GS} values less than 4V, the MOSFET is not controlled because the threshold voltage V_{th} is not reached. When the MOSFET start operation $V_{GS} > V_{th} > 4V$, and then the current $\mathrm{I_{DS}}$ increases gradually with V_{GS}. The results are in good agreement.

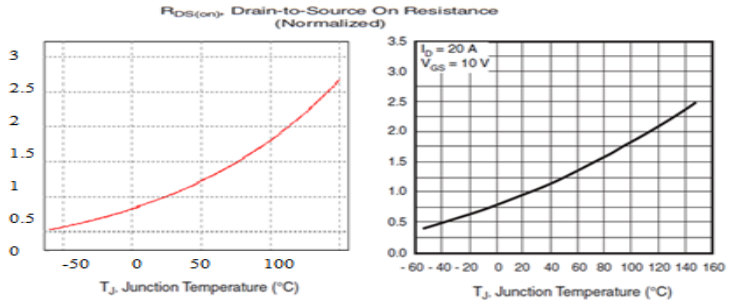


Fig. 11. Variation of R_{DSon} versus the temperature $\mathrm{T_j}$

The Fig. 11 shows the simulated and the actual Drain-Source resistance (R_{DSon}) in function of the temperature variation T_j, for a current equal to $I_{DS} = 50A$ and voltage $\mathrm{V_{GS}}$=20V. The obtained curves are very close in a wide temperature range (up to T=150°C). We observe that the result obtained is similar to the datasheet, particularly in the interval $[0°C, 150°C]$.

4 Conclusion

A new model of SiC Power MOSFET is proposed in this paper. This model is implemented successfully under Psim, Pspice and Saber softwares and then have been tested and optimized for numerical circuit design and simulation. The Characteristics of the MOSFET simulation models (on-state resistance, threshold voltage, and transconductance, etc...) has been compared to actual characteristics given by manufacturer's data sheet in Psim, PSpice and Saber.

The proposed electrothermal model is very accurate and able to describe the dynamic behavior of the SiC MOSFET with a very good precision. Owing to our last results, it is shown that the electrothermal model developed on Psim, Pspice

an Saber has a high accuracy and is close to the optimum operating conditions presented in the datasheet. This simulation model of SiC power MOSFET is easy to use in numerical design and prototyping of electric circuits and simulations. The future work of our staff will be on nonlinear and robust control of a power circuit including the SiC MOSFETs.

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